# Pixel analog part design in TIIMM for STRONG project

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# Contents

# STRONG - Expectations and status

## The TIIMM

The TIIMM ( Tracking and Ions Identifications with Minimal Material budget ) project in STRONG aims to create a new class of instrument combining precision tracking and energy loss measurement in conditions where minimizing the crossed material is mandatory.

## TIIMM expectations and status

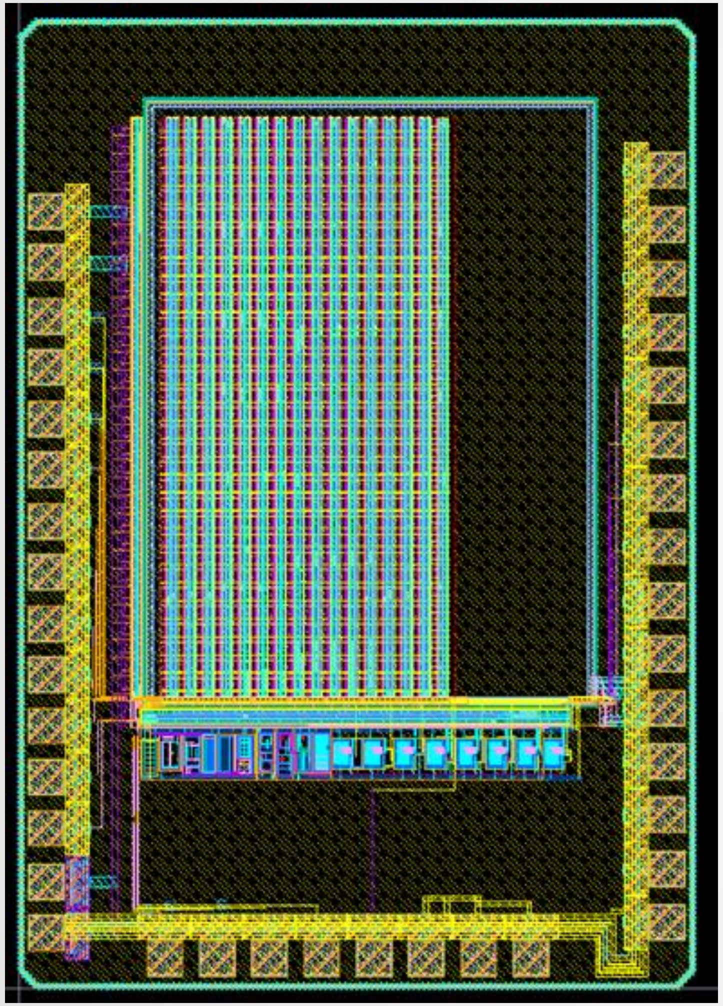
- 1st prototype (TIIMM-1) in late 2020
- 2nd prototype (TIIMM-2) in 2021-2022
- Both are small size prototypes
- Status: preliminary prototype (TIIMM-0) submitted with MIMOSIS-1.

# STRONG - Requirements preliminary

- **Requirements for hadron physics**
  - Particles to be detected: protons to Oxygen ions (200-400 MeV/u) and consider proton close to 1 GeV
  - Spatial resolution 5 to 10 µm
  - Hit rate few $kHz/cm^2$ (in any case < $MHz/cm^2$)
  - Sensor surface area few $cm^2$ (2x2 or 1x3 probably OK)
  - Power dissipation compatible with air cooling < 200 $mW/cm^2$

- **Sensor specifications**
  - Signal charge assuming 25 µm sensitive thickness: 500 $e^-$ to 500 000 $e^-$ (1-1000 dynamic ← to be confirmed)
  - Digitization over 4 to 6 bits (4 will be probably not enough due to dynamic…)
  - Pixel pitch 20 to 40 µm (the smaller, probably the better)
  - Frame rate 1-10 kHz ↔ integration time 100 to 1000 µs (if $T_{int}$ ~ µs possible, better)

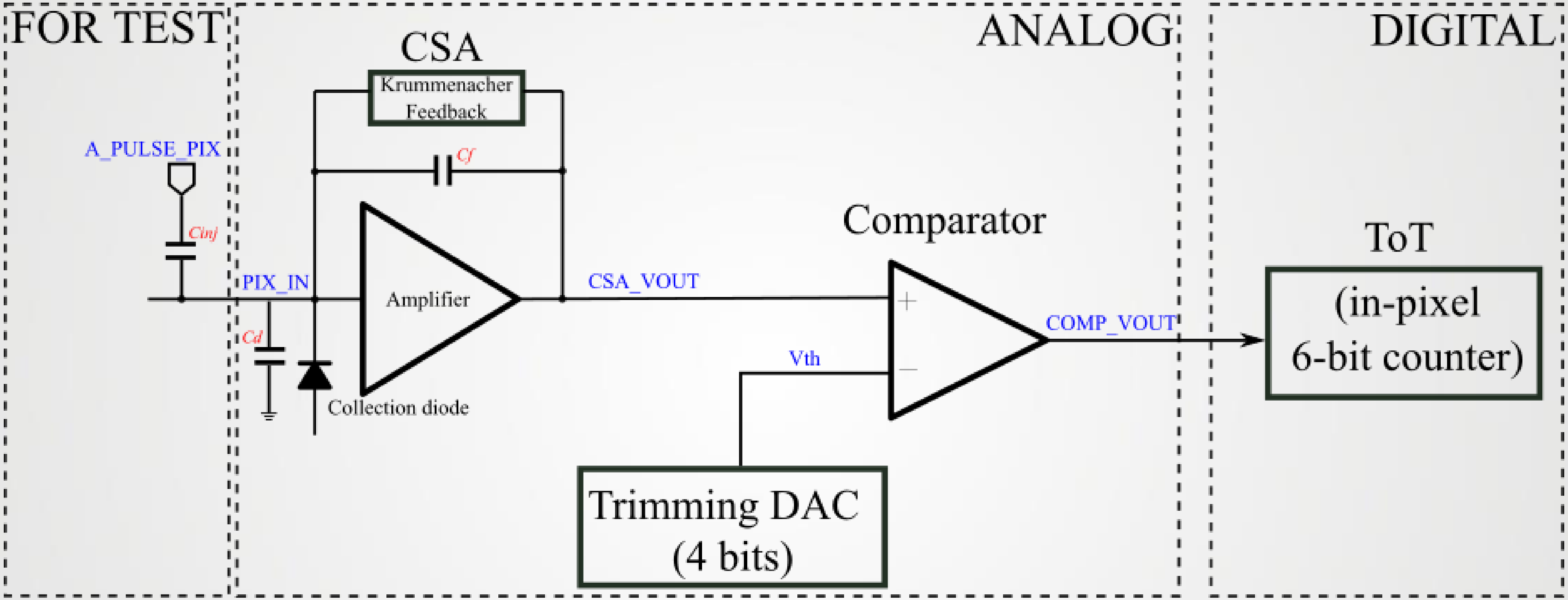
# TIIMM-0 - General description



TIIMM0 sensor layout

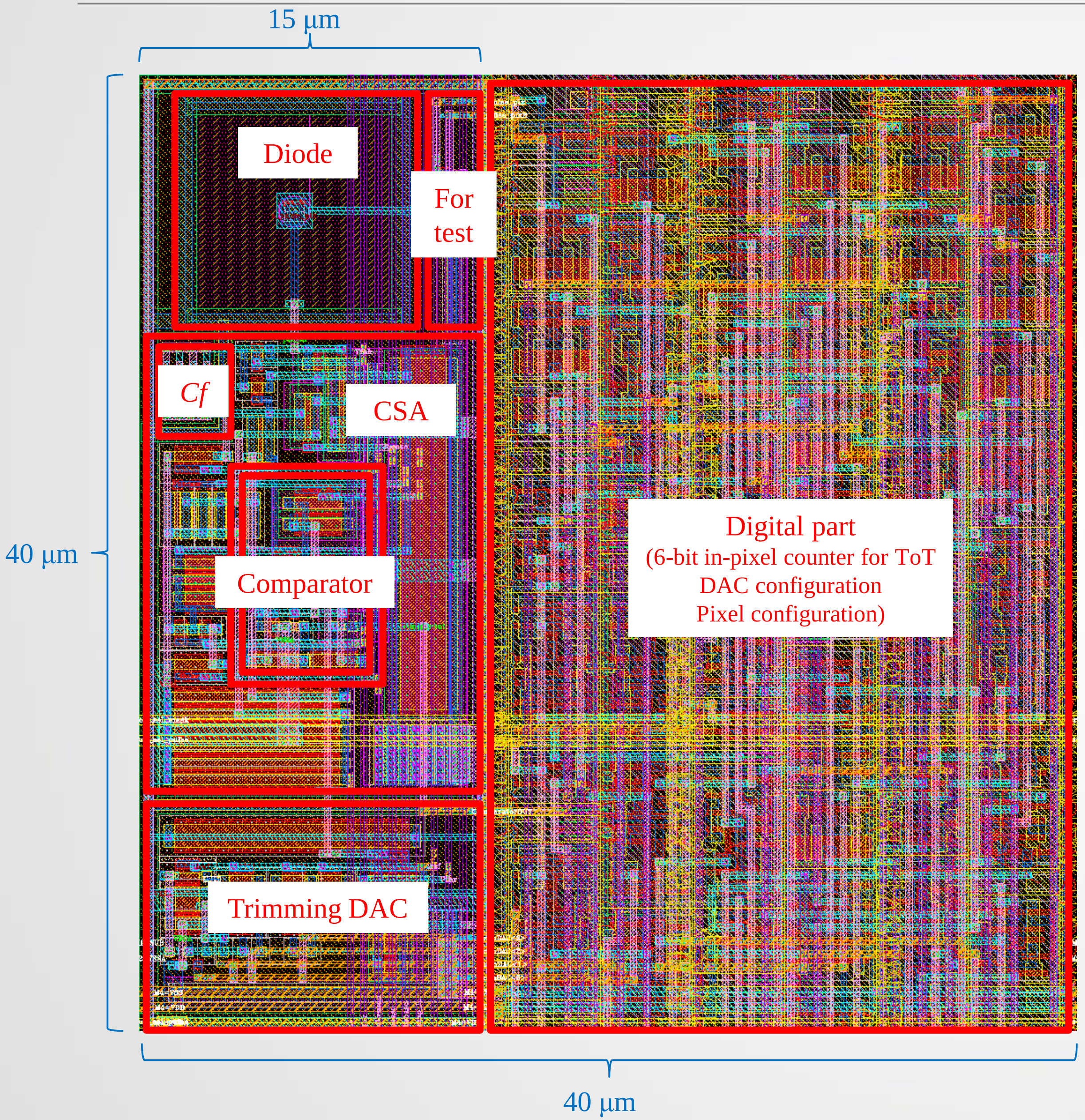
- **CMOS Monolithic Active Pixel Sensor**
- **Design in TowerJazz 180 nm process**
- **Submitted in March, 2020**
- **Chip area: 2.2 mm * 1.5 mm**
- **Matrix: 32 (rows) * 16 (columns)**
  *(the last column has the analog output for test)*
- **Pixel pitch: 40 µm**
- **Position and energy measurements**

# TIIMM-0 - Pixel structure




- **TOT (6 bits)** – 6 bits register in pixel
- **Trimming DAC (4 bits) -** for threshold adjustment
- **Possibility to mask pixels**

# TIIMM-0 - Pixel layout design

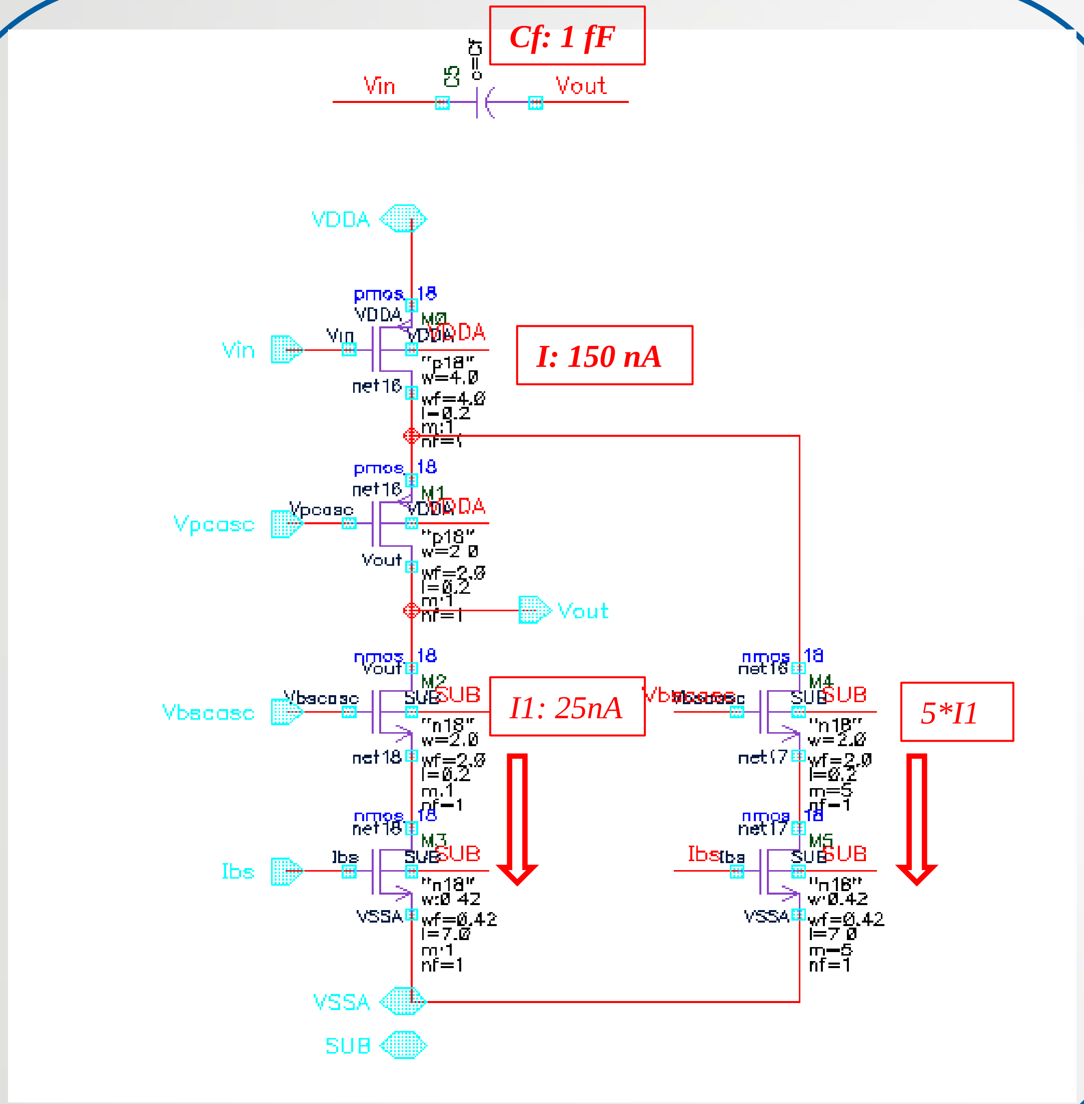



**Pixel size: 40 µm * 40 µm**

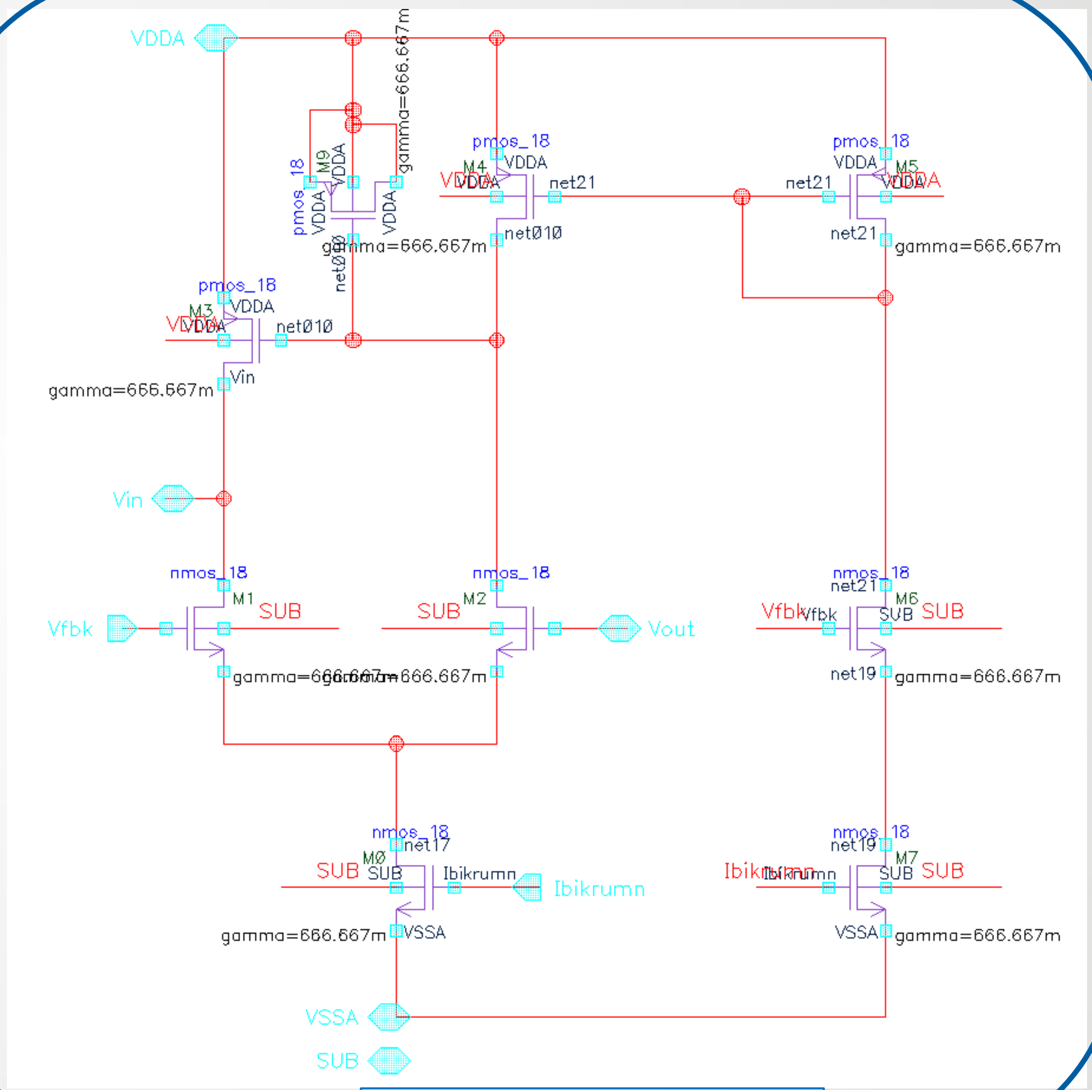
**Analog part: 40 µm * 15 µm**

**Digital part: 40 µm * 25 µm**

# TIIMM-0 - CSA with Krummenacher feedback

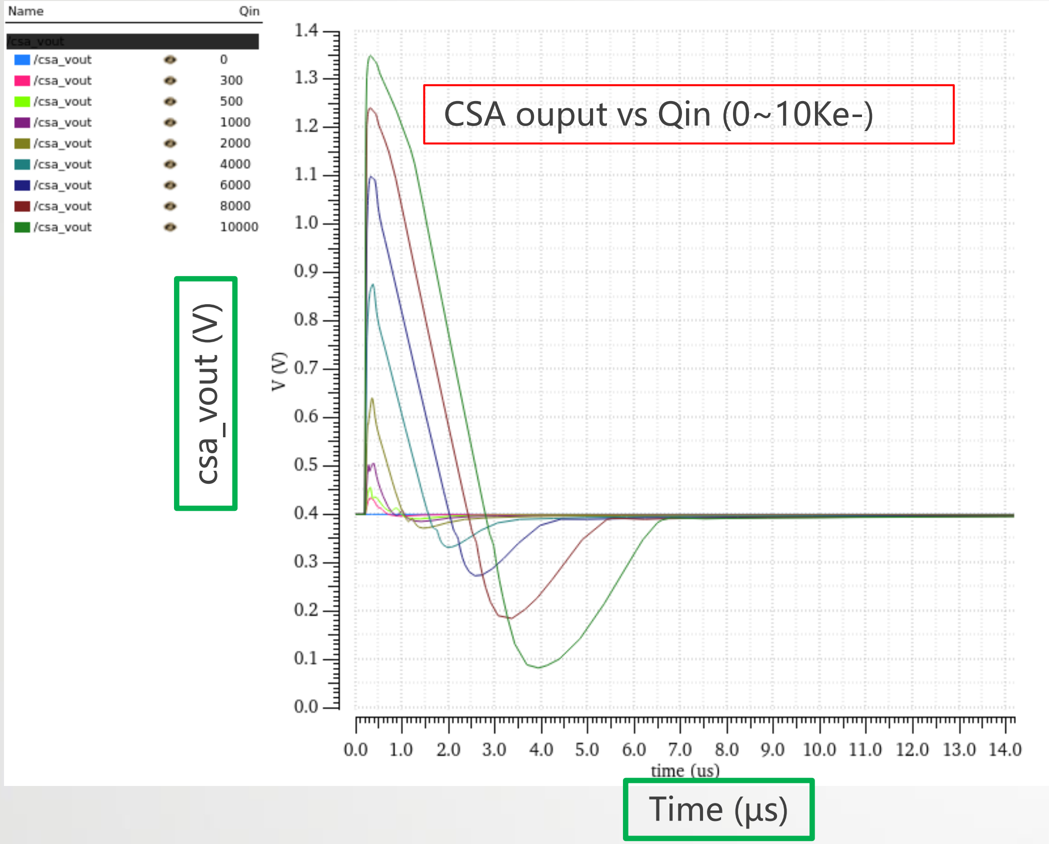


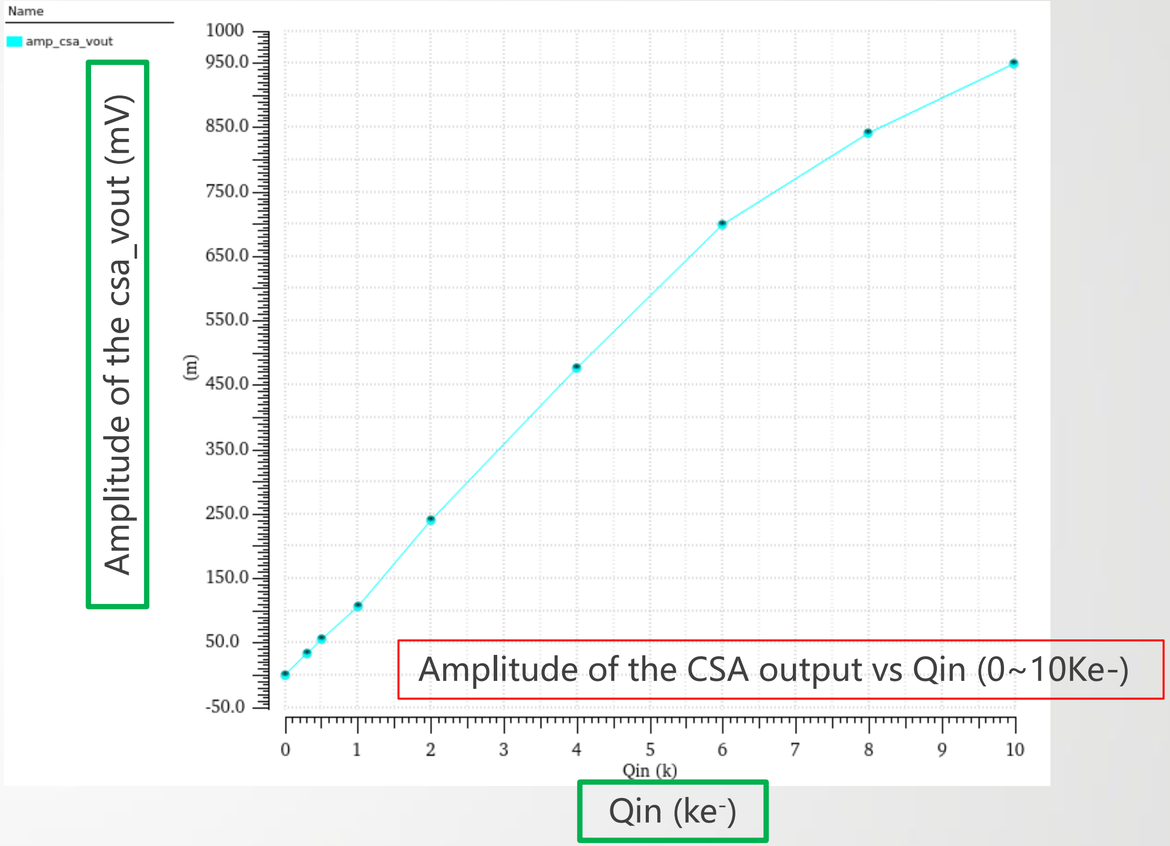

Amplifier




Krummenacher Feedback

# TIIMM-0 - Simulation performance of CSA



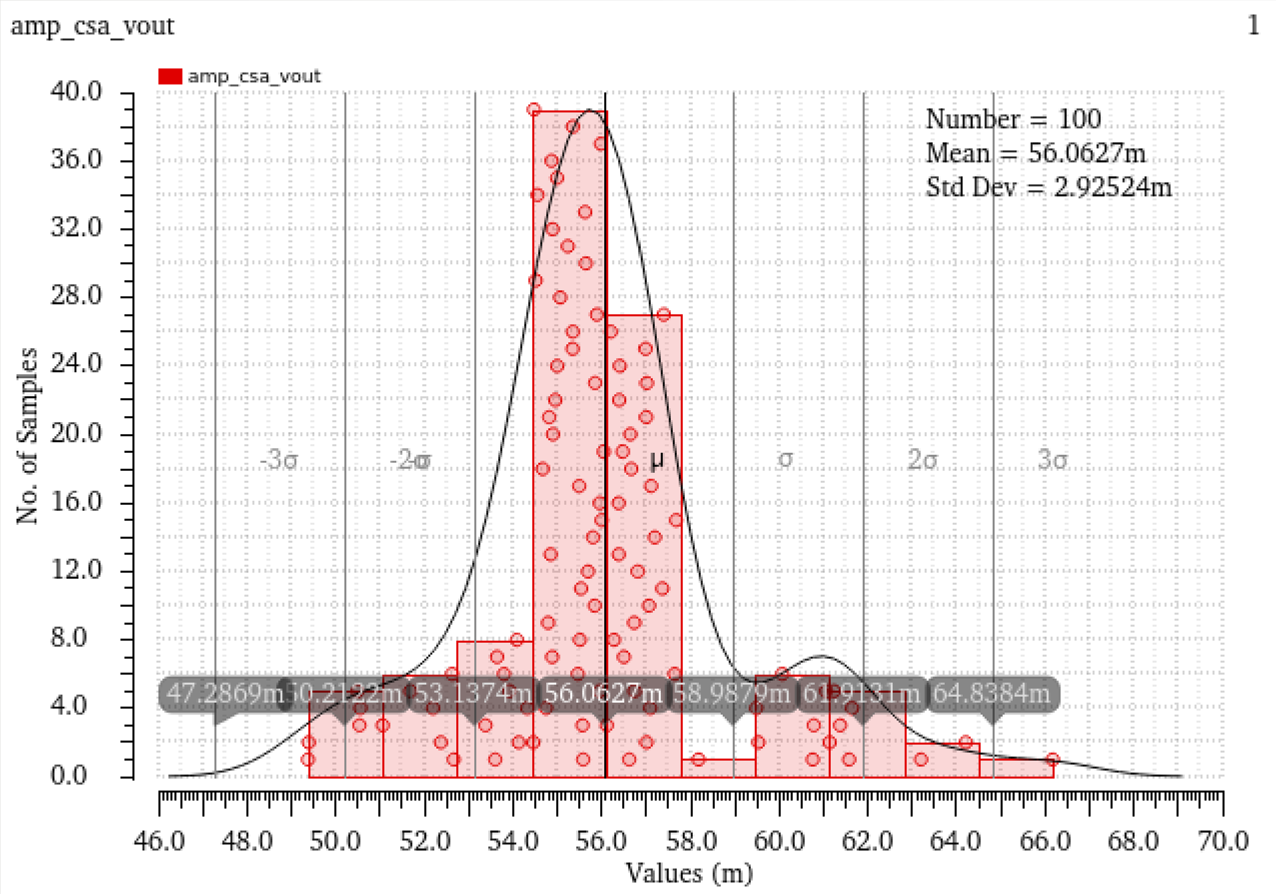




- Cf = 1fF, Cd = 2 fF
- Gain about 120 mv/ke-, ENC = 42 e -
- There is a overshot problem in the CSA design.

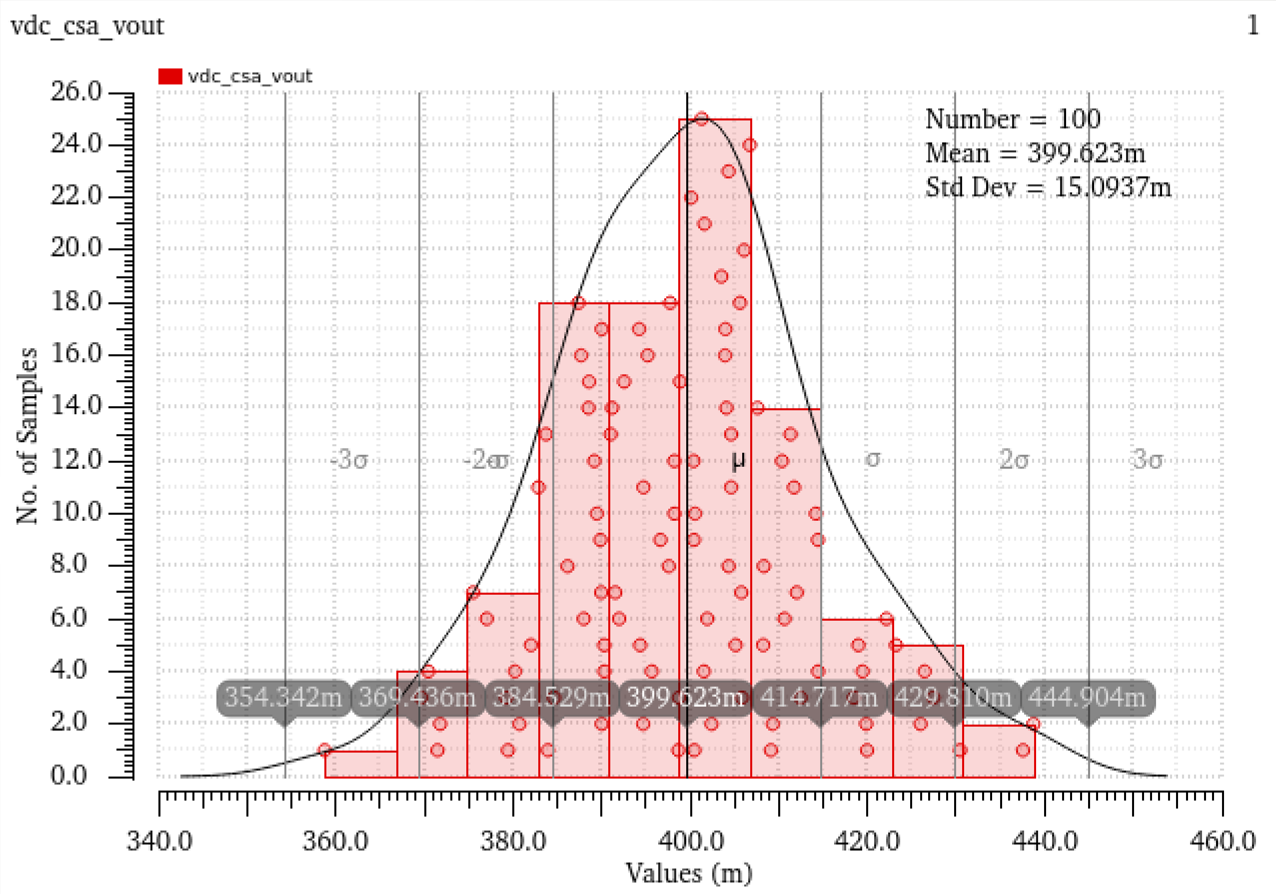
# TIIMM-0 - Performance of CSA (corner simulation)

| Qin=500 e- | NOM 27℃ | FAST 0℃ | SLOW 85℃ |
|---|---|---|---|
| CSA Power[nA] | 146.8 | 150.2 | 149.9 |
| ENC[e-] | 41.98 | 39.99 | 43.93 |
| Amplitude of the CSA output[mV] | 55.89 | 55.68 | 60.09 |
| Baseline of the CSA output[mV] | 399.7 | 399.8 | 399.3 |

# TIIMM-0 – Performance of the CSA (MC simulation|Mismatch)




Monte Carlo simulation, spread of the amplitude of the CSA output (Qin=500 e-)



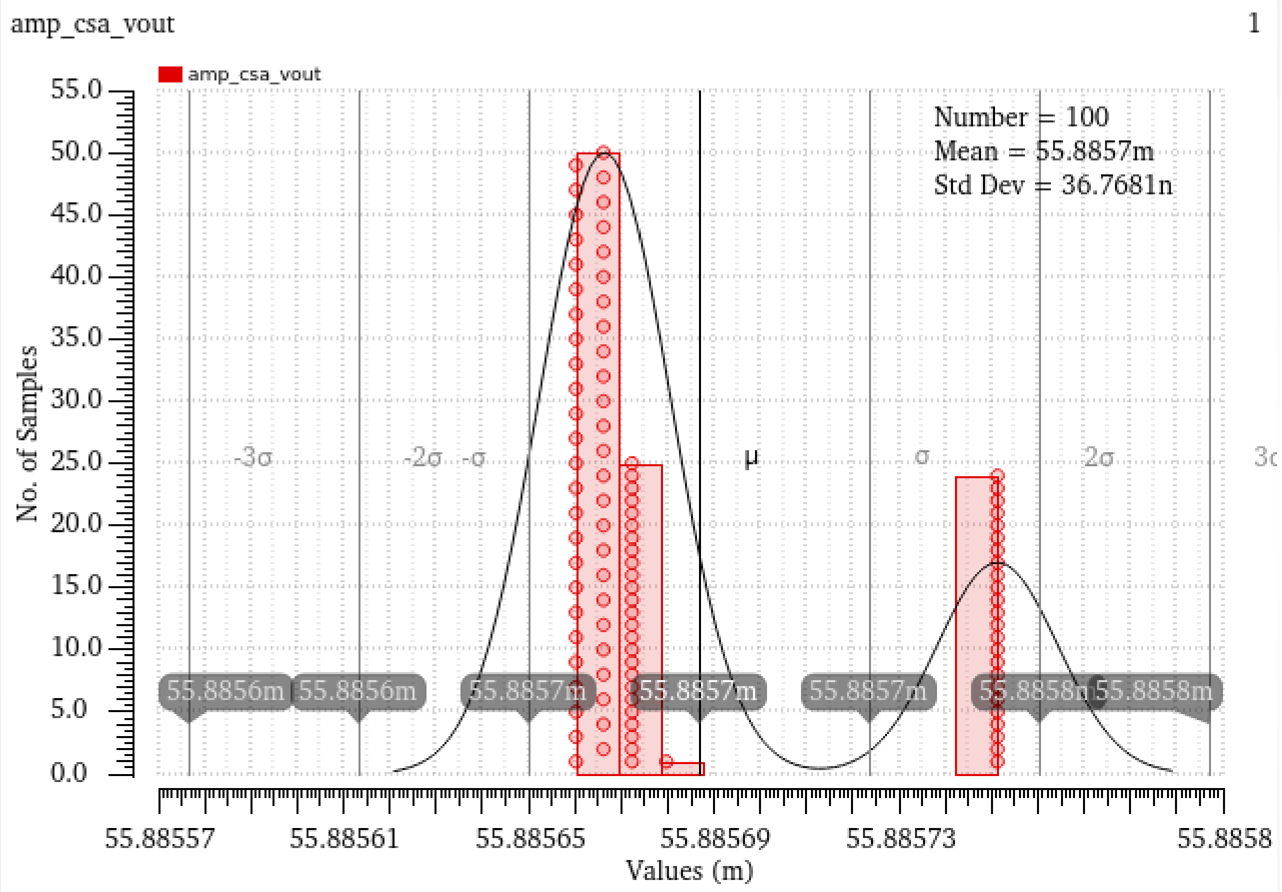

Monte Carlo simulation, CSA output baseline offset

- Offset spread of the CSA

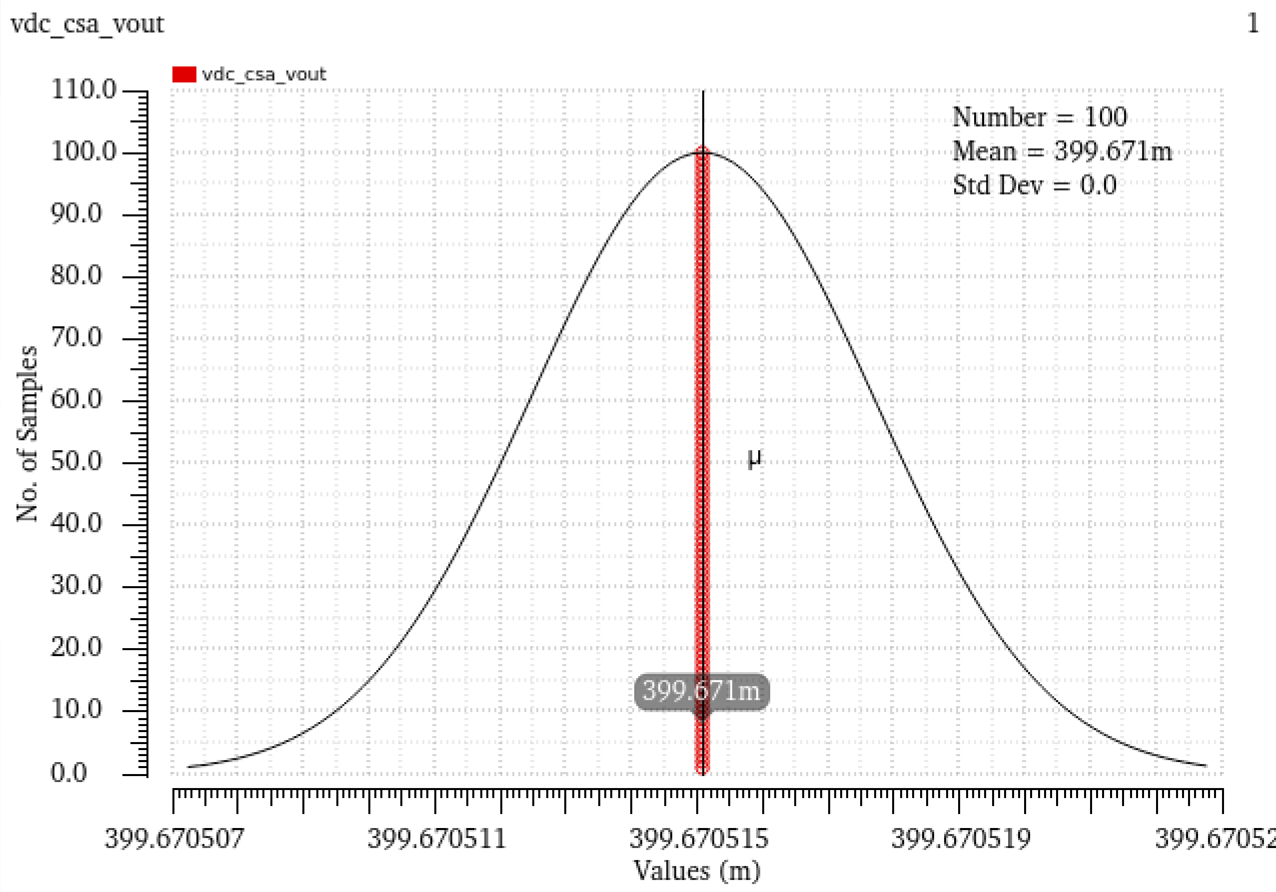
  Sigma: 15.09 mV

  Range: 359 mV ~ 440 mV

# TIIMM-0 – Performance of the CSA (MC simulation|Process)



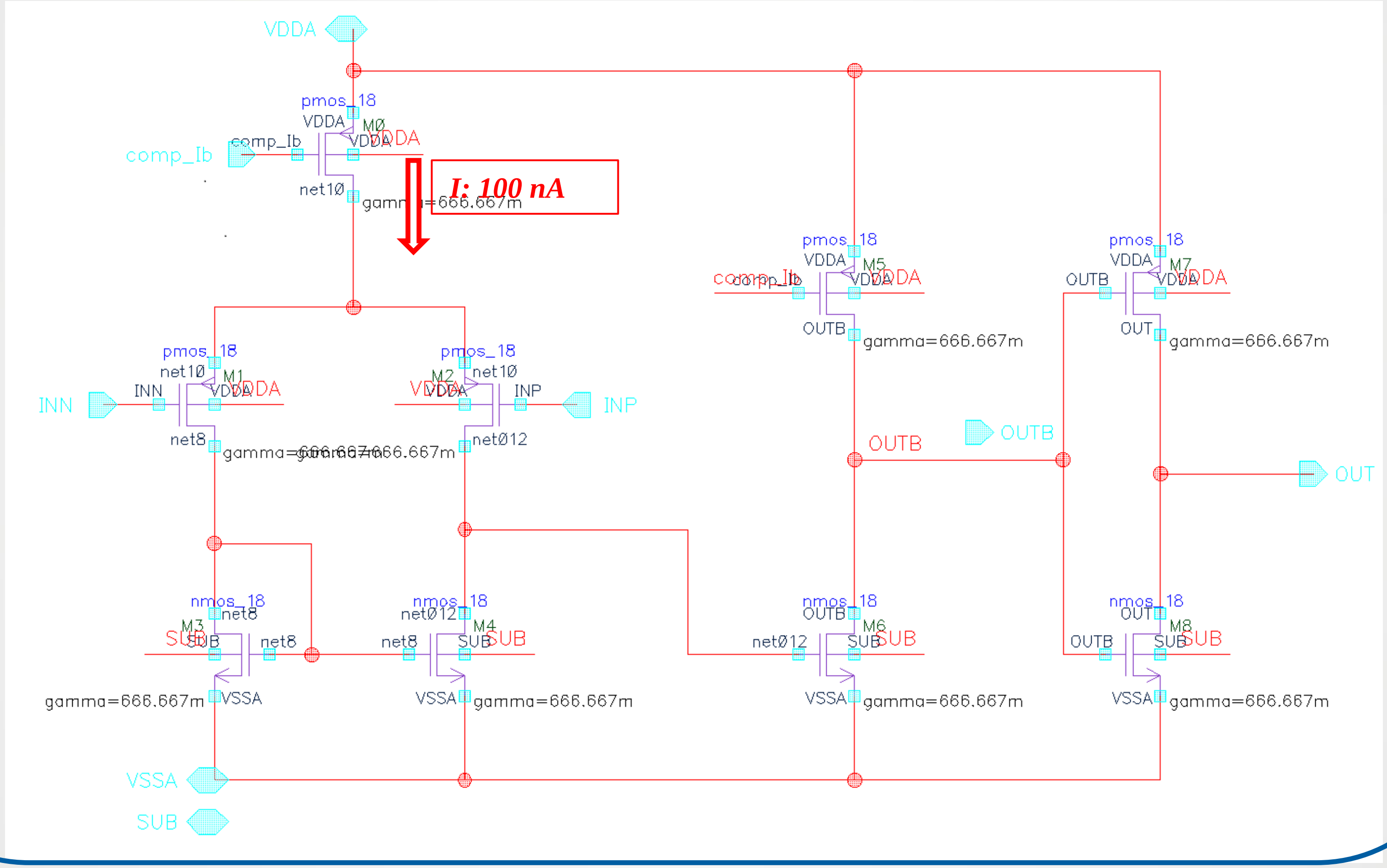

Monte Carlo simulation, spread of the amplitude of the CSA output (Qin=500 e-)




Monte Carlo simulation, CSA output baseline offset

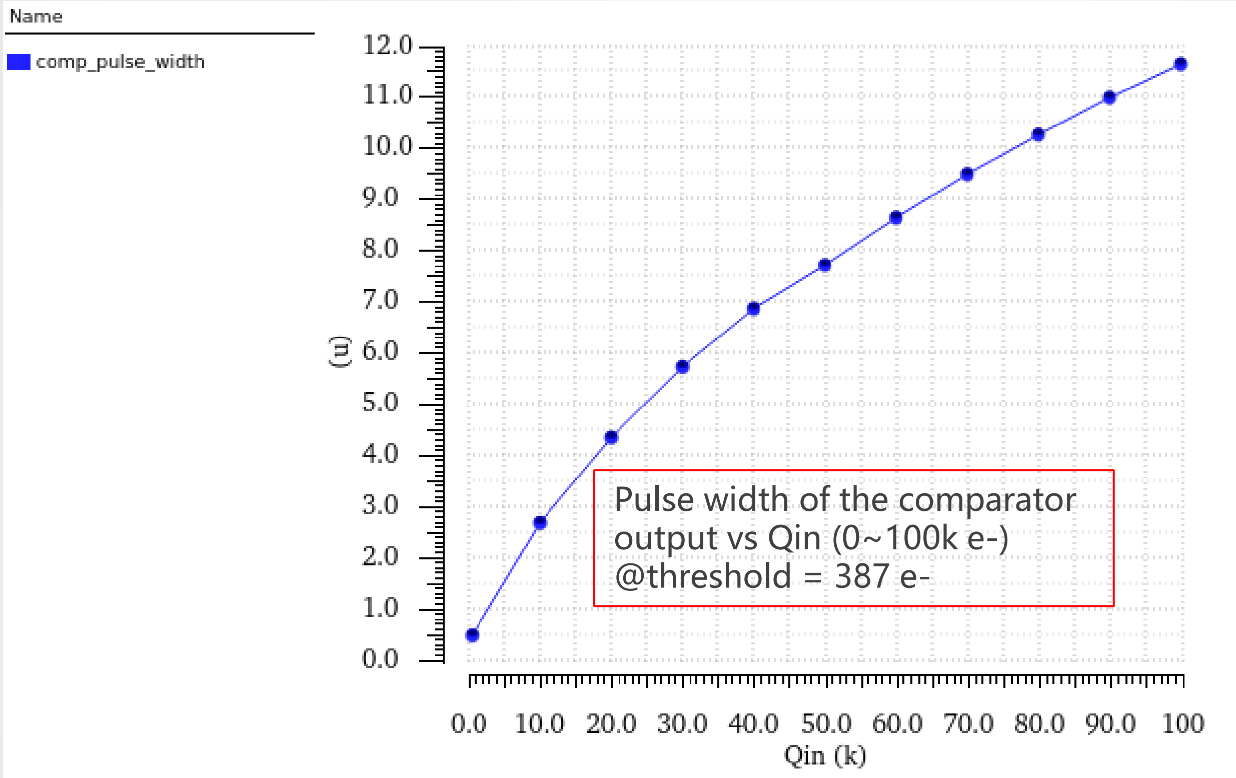
- Offset spread of the CSA baseline
  Sigma: 0 mV

# TIIMM-0 - Comparator



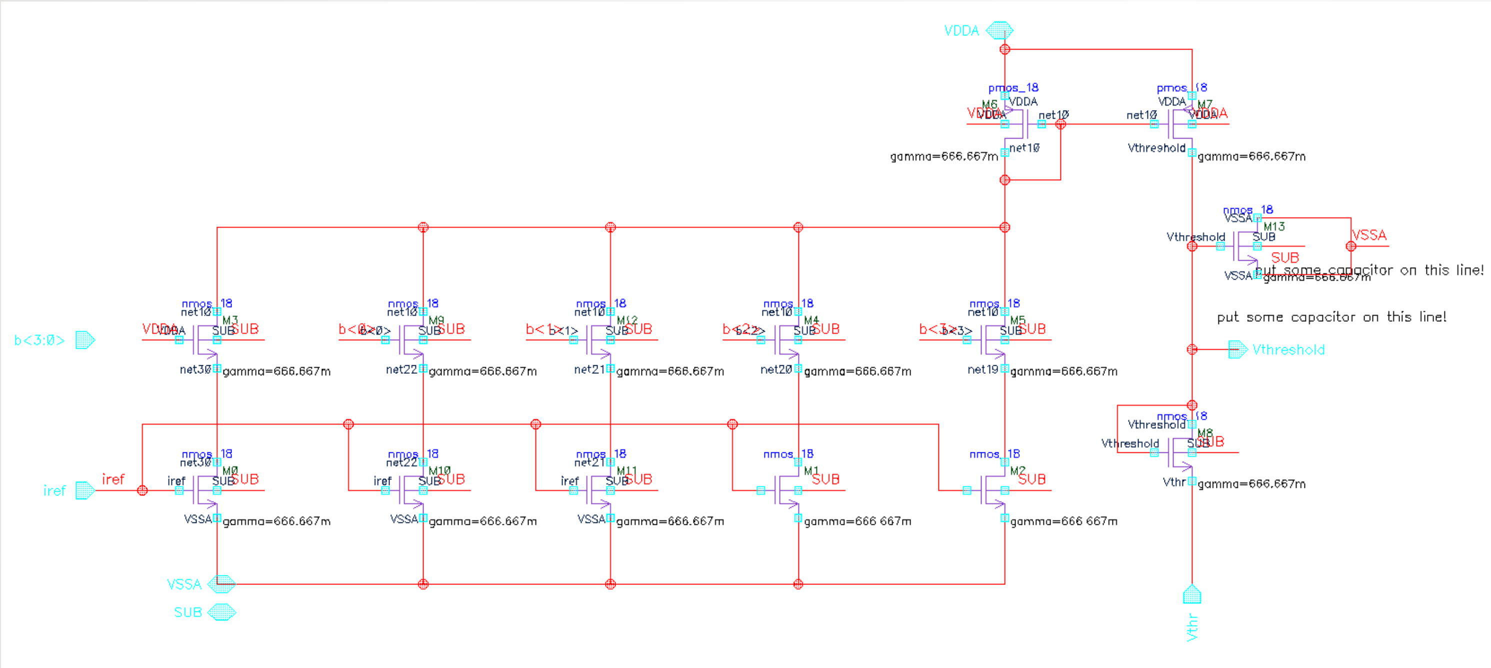

- The comparator is designed with a two stage amplifier and an inverter to form the digital signal.

# TIIMM-0 - Pulse width vs Qin (0~100Ke-)




- The pulse width (0.5 µs~12 µs) increase with the Qin(from 0 to 100 Ke-).
- Threshold=387 e-.
- ToT output is not linear (at least at low Qin) → calibration needed.

# TIIMM-0 – Trimming DAC

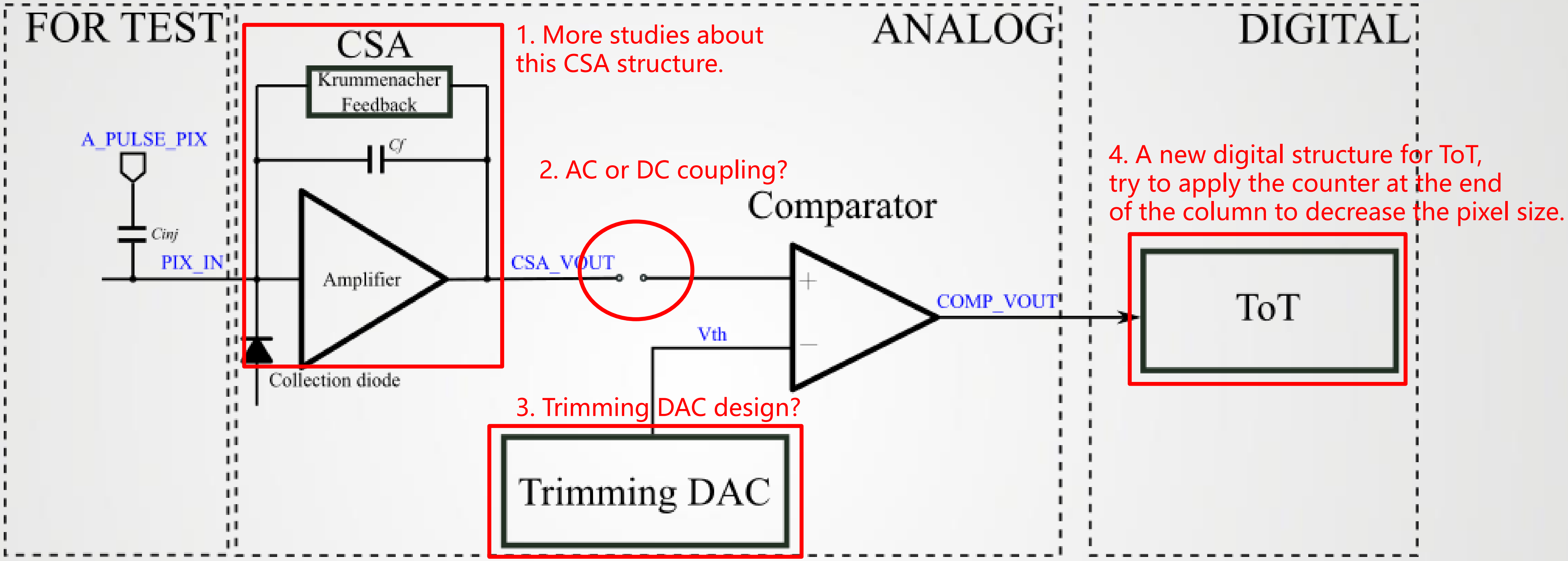



- The Trimming DAC provides the adjustable threshold for the Comparator to treat with the problem of the offset of the CSA
- 4 bits
- Range: 331 mV ~ 473.8 mV (cover the offset of the CSA)

# TIIMM-0 – Analysis

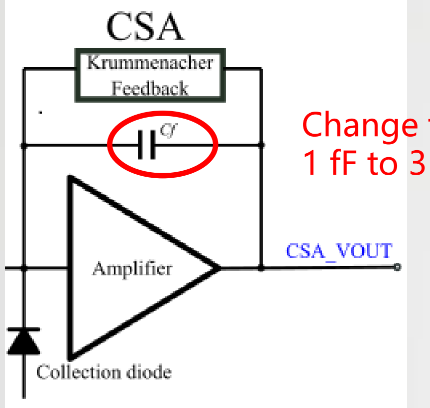
- ENC = 42 e- → is that good enough for our project?
- ToT output is non-linear → require calibration.
- Resolution on Qin varies non-linearity with Qin → input to physics simulation for cross check.
- In this design, the trimming DAC can cover the offset range of the CSA. But it only has 4 bits. Its performance needs to be verified by chip test.

# TIIMM-1 - Pixel structure

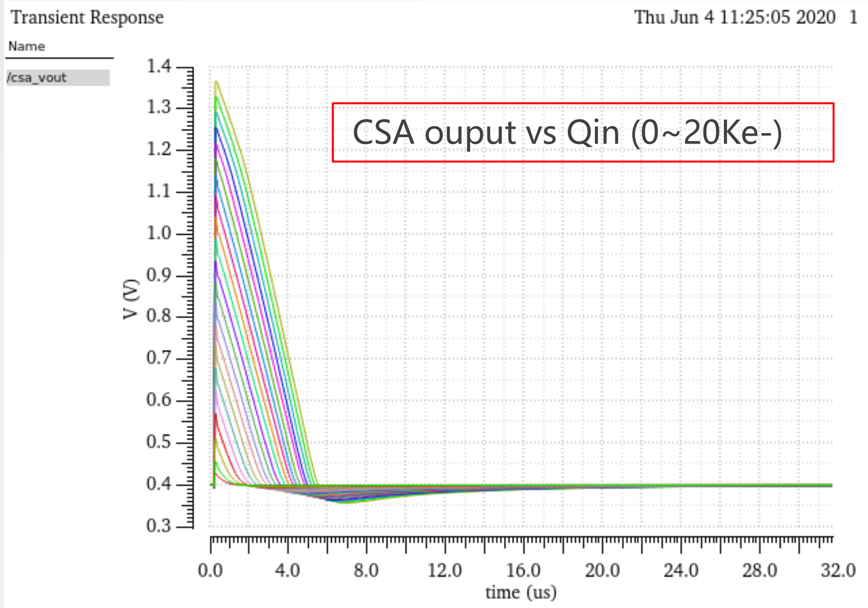


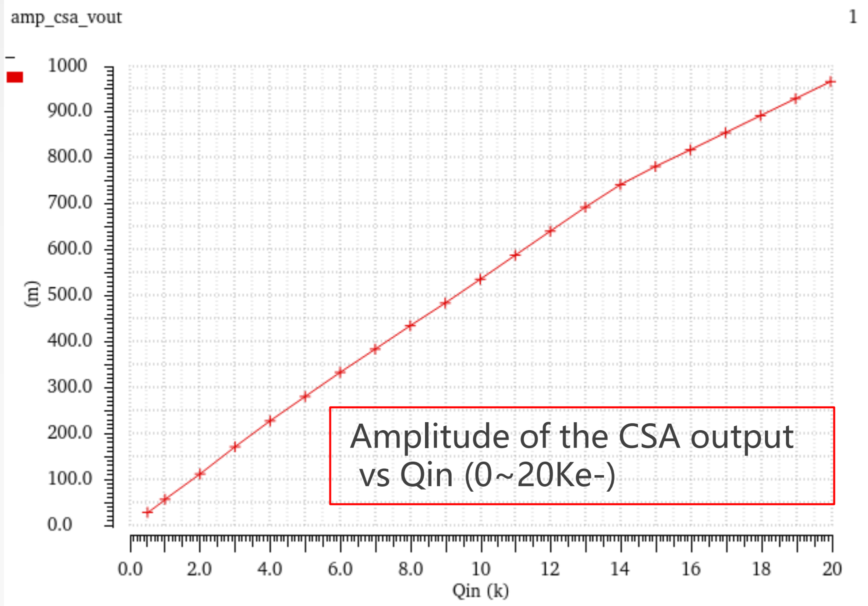

- In this design, we want to apply this new architecture of amplifier. This amplifier structure can get higher gain which can reduce the ENC.
- Due to the spread of the CSA output baseline is large, and it is common in pixel sensor. We are considering about using AC coupling between CSA and comparator or a trimming DAC with better performance to reduce the threshold dispersion.

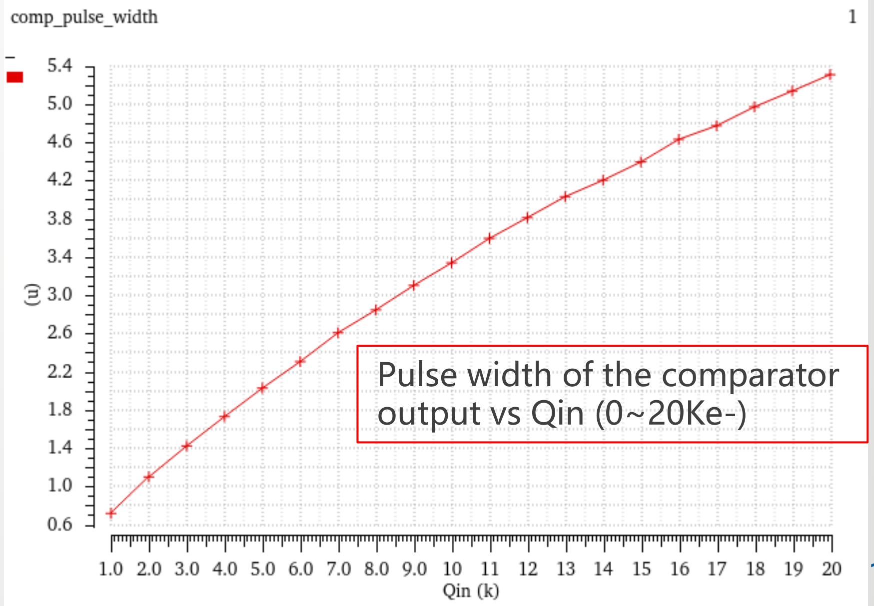
# TIIMM-1 - CSA with Krummenacher feedback




Change from 1 fF to 3 fF



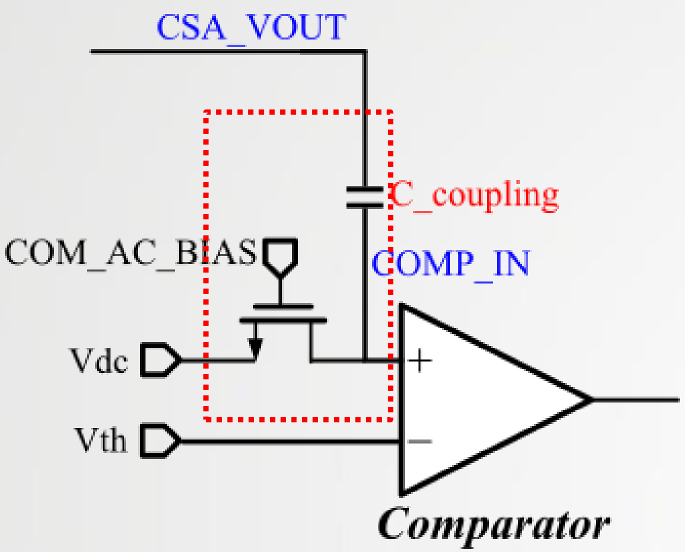



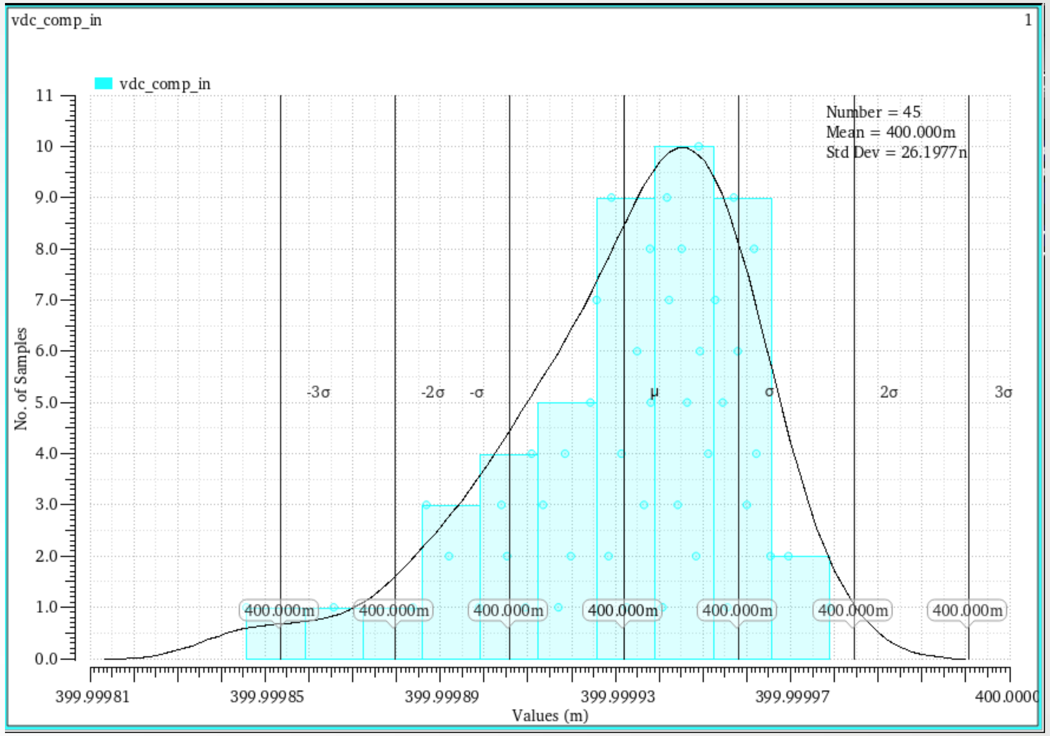




- Cf=3 fF(In TIIMM-0, it is set as 1fF)
- ENC=52 e-.
- At charge range: 0~20k e-

1) The overshot problem of the CSA output improved a lot.
2) The pulse width of the comparator shows a better linearity performance.

# TIIMM-1 - AC coupling




- Add capacitor between CSA and comparator to realize AC coupling (consuming an area for capacitor) . And the DC-level will be provided by a reference voltage Vdc through a NMOS transistor. The simulation shows that the spread of the COMP_IN after the capacitor is σ = 26 nV.
- But the comparator will still bring offset even though we use AC-coupling to eliminate the pixel-to-pixel baseline spread (threshold offset). Thus we still need a trimming DAC afterwards to reduce the offset of the comparator. AC-coupling + Triming DAC (simple one, only used to reduce the offset of the comparator)
- Or DC-coupling + Triming DAC (high performance)

# TIIMM-1 - Trimming DAC (reference paper)

- A multi-level offset trimming DAC
  - 7-bit trim DAC for tuning $I_{DAC}$ current
  - Two different ways to control the tuning range (bit br or bit bb)
  - Addition of an extra offset at the input from outSH_ref line (bits bosf<0:1>)
- Performance
  - Pixel-to-pixel baseline level spread before correction is about σ =17 mV rms. It is reduced to σ =1.524 mV rms(using only 7-bit trim DACs)

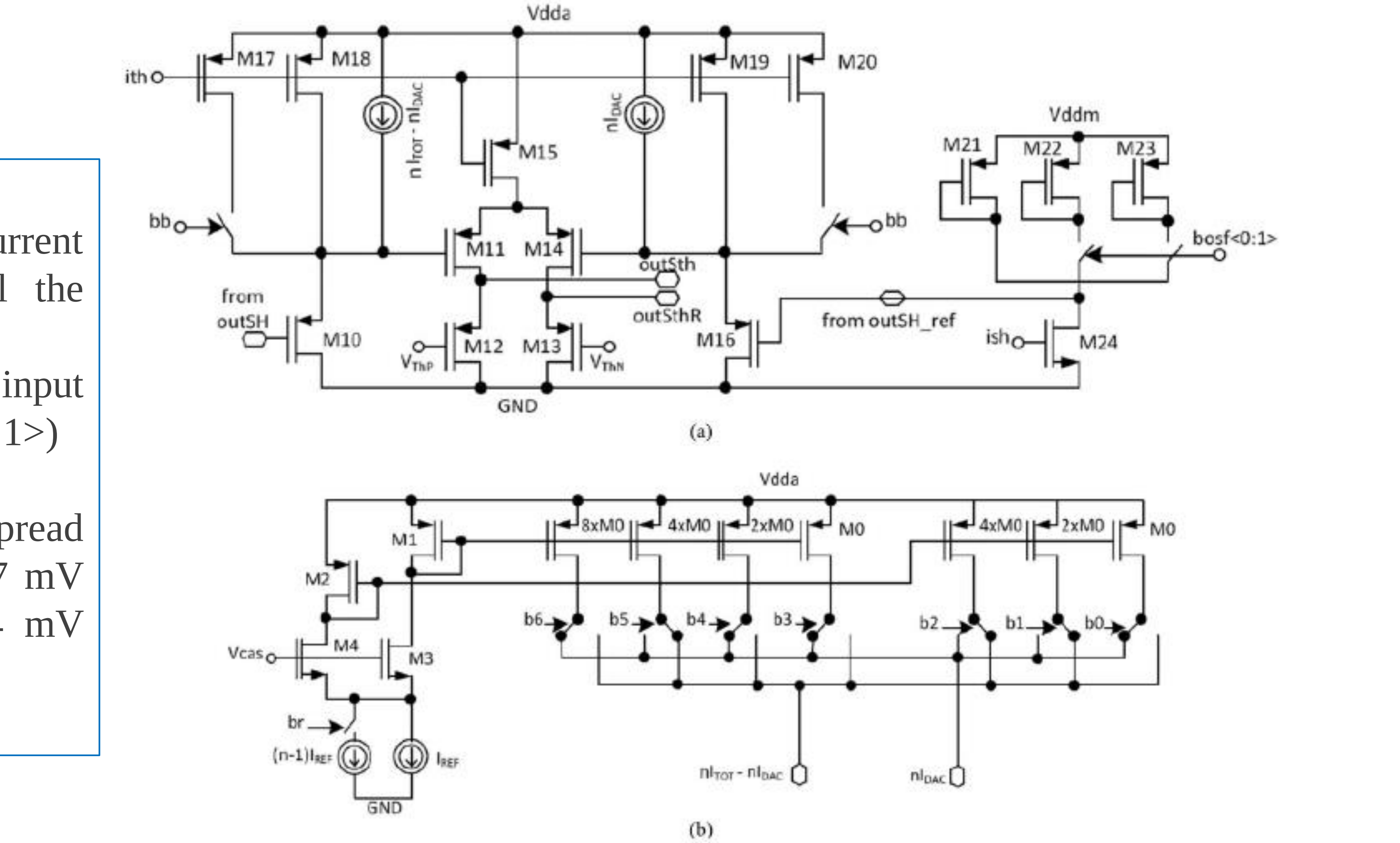
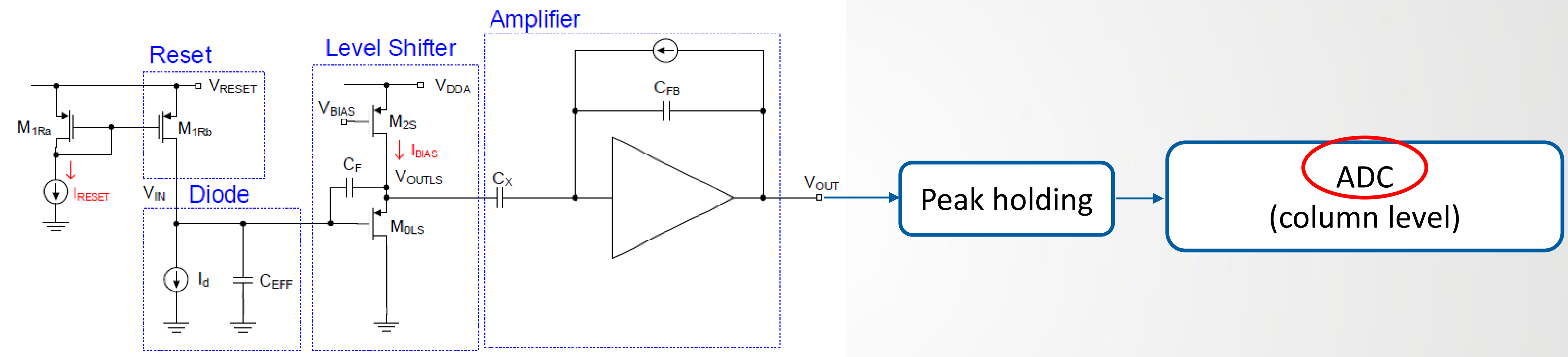


Fig. 7. (a) Circuit for applying the threshold voltage and offset correction–trim DAC is represented by two current sources, (b) simplified scheme of trim DAC (M0 transistor dimensions are $W_0/L_0 = 0.3\ \mu m/2\ \mu m$).

*IEEE Transactions on Nuclear Science, Volume 63, Issue 2, April 2016, doi: 10.1109/TNS.2016.2527834*

# New pixel architecture with ADC

$$V_{OUT} = \frac{Q_{DET} C_X}{C_{EFF} C_{FB}}$$




- For the next prototype, if we will try the column ADC structure?
  - Need peaking holding circuit in pixel.
  - Reduce the area (In ToT structure, the register for ToT in the pixel consumes a large area)
  - Column level, can get higher bits.
  - The output amplitude of the Amplifier has better linearity vs input charge.
  - The dynamic range is bound to be smaller with the ADC structure (unless we can switch the capacitance)

# Conclusion

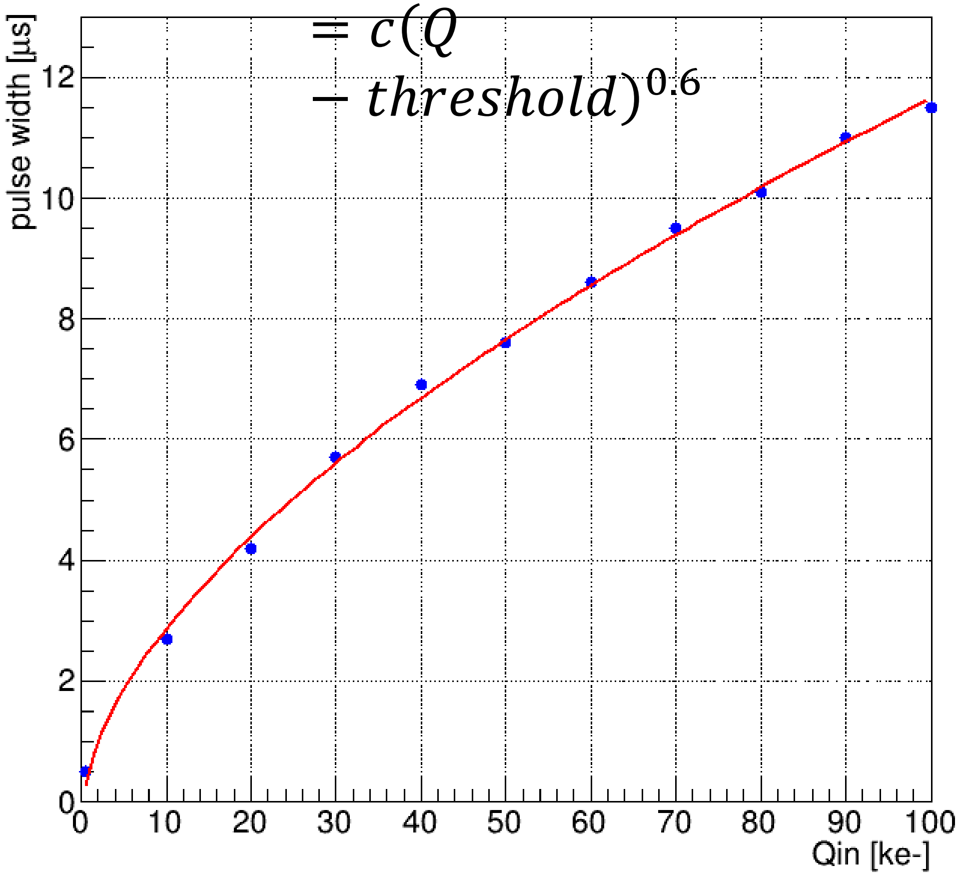
- The TIIMM-0 design has been summarized. The chip contains 32 rows and 16 columns with a pixel pitch of 40 μm. A 6-bit ToT architecture has been applied for energy measurement.
- The ENC of the TIIMM-0 is 42 $e^-$.
- The 4-bit Trimming DAC in TIIMM-0 provides the adjustable threshold for the Comparator to treat with the problem of the offset of the CSA. And the performance need to be verified through the chip test.
- In TIIMM-1, more studies about the amplifier were carried out.
- AC-coupling scheme between the CSA and comparator was proposed.
- A multi-level trimming DAC to solve the offset problem with calibration was presented (reference).
- ADC solution seems more complex, not considered for the time being.

*The end*

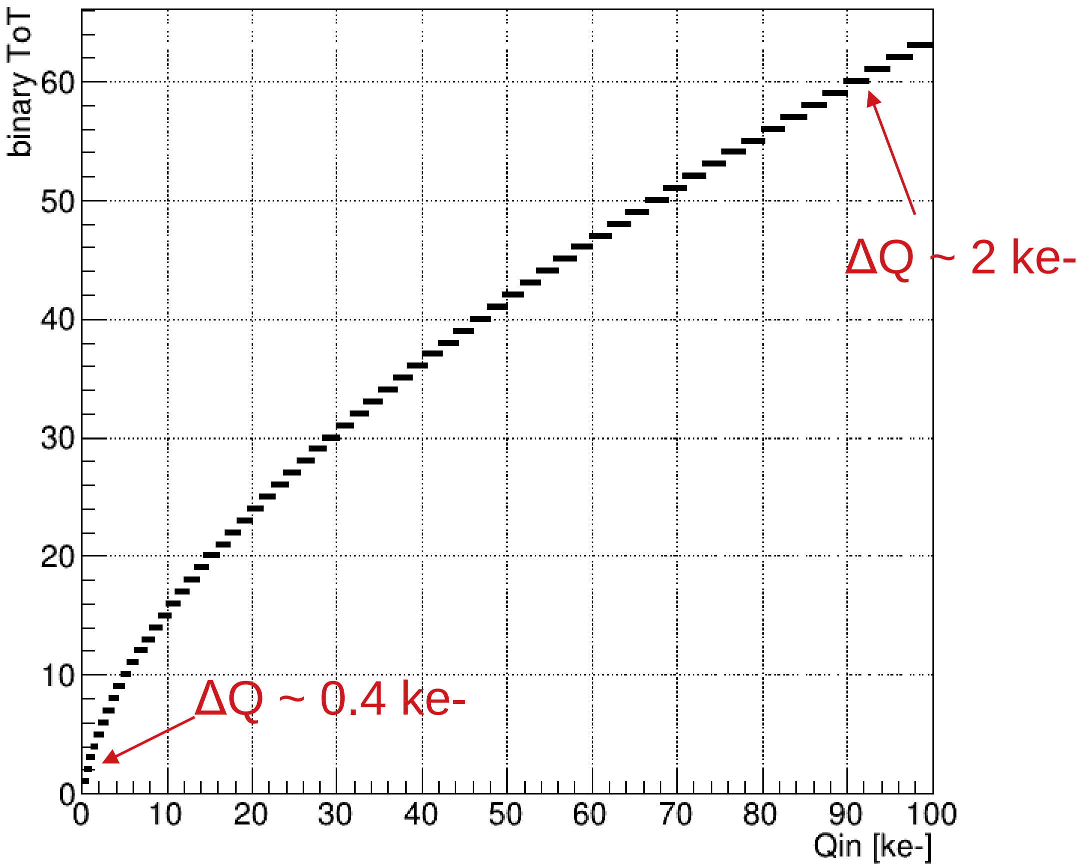
Thanks!

# Predicting ToT values (TIIMM-0 proto)

$$width = c(Q - threshold)^{0.6}$$




6 bits conversion (bin width ~ 0.19 µs




ΔQ = increase in Q to increment ToT by 1 digit