Update on pixel bus and pixel module interfaces

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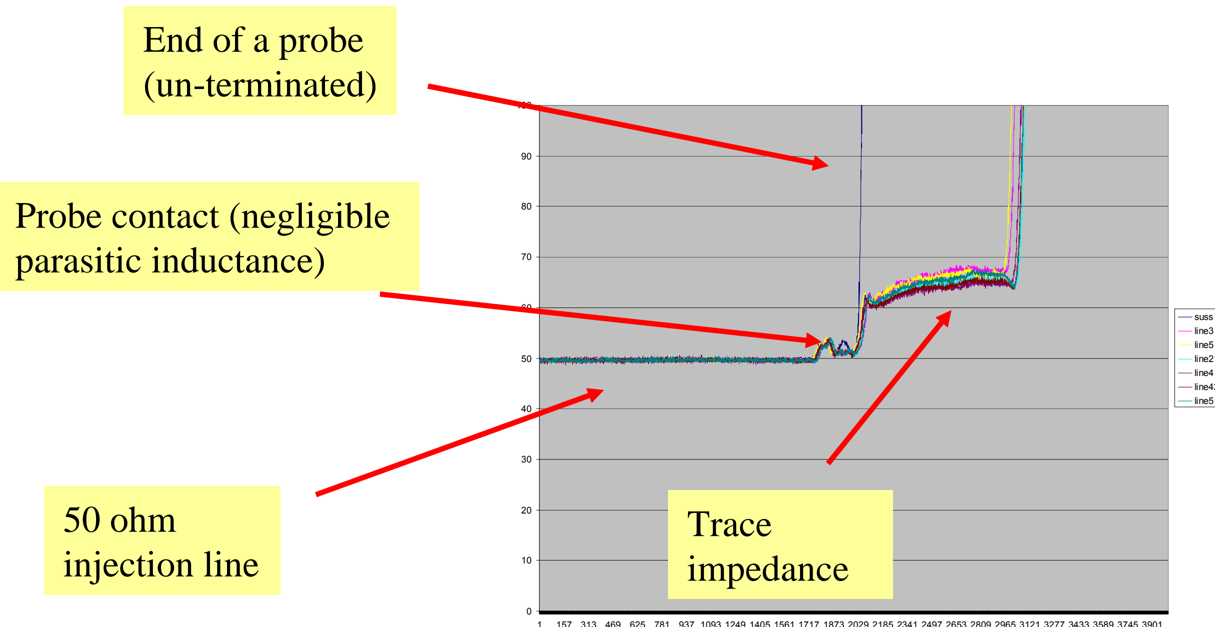
On behalf of INFN Milano and Università degli Studi di Milano

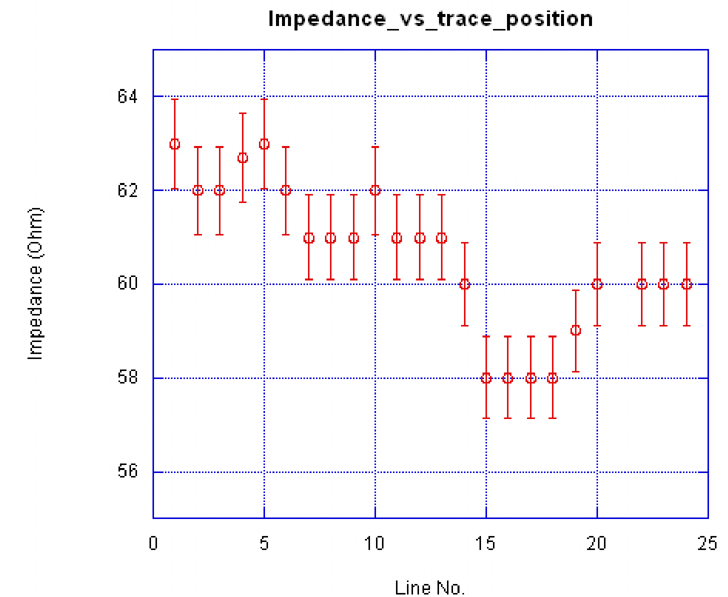
Index

- Bus design
  - Understanding “prototype bus” construction
    - Discrepancies from expected performances
    - Analysis undertaken
  - Design review of the “3-chip BUS” with CERN PCB shop and suggestions
  - Status of BUS redesign
    - Production issues
- HDI and transition card
  - Prototype HDI design using an FPGA
  - Next steps

Understanding "prototype bus" construction

- **Three main concerns:**
- Bus designed for 50 Ohm Impedance
- Measured impedance is > 60 Ohm
- Impedance changes between identical lines
- Measured NEXT crosstalk (~ 10%) much higher than simulated (3%)

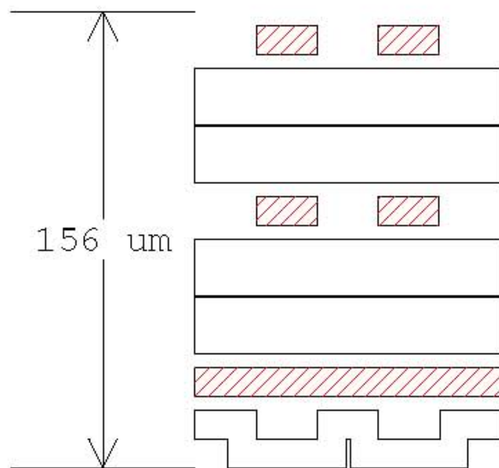




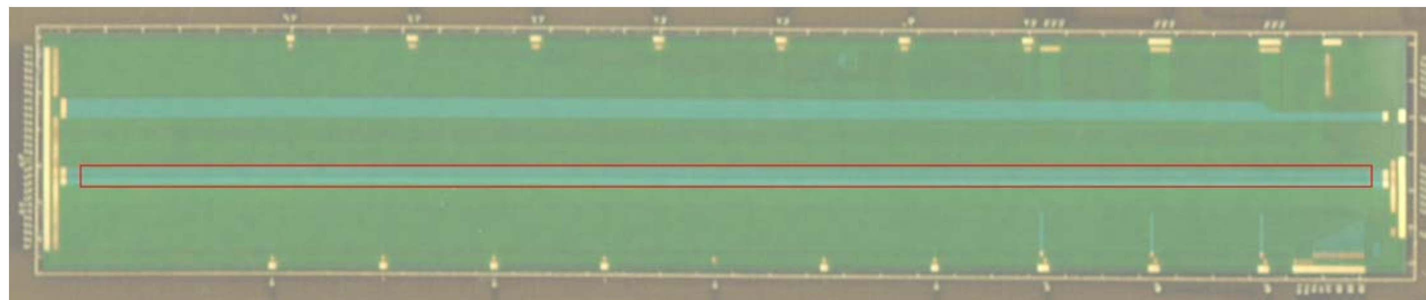
Understanding "prototype bus" construction

- **Stack-up by design**

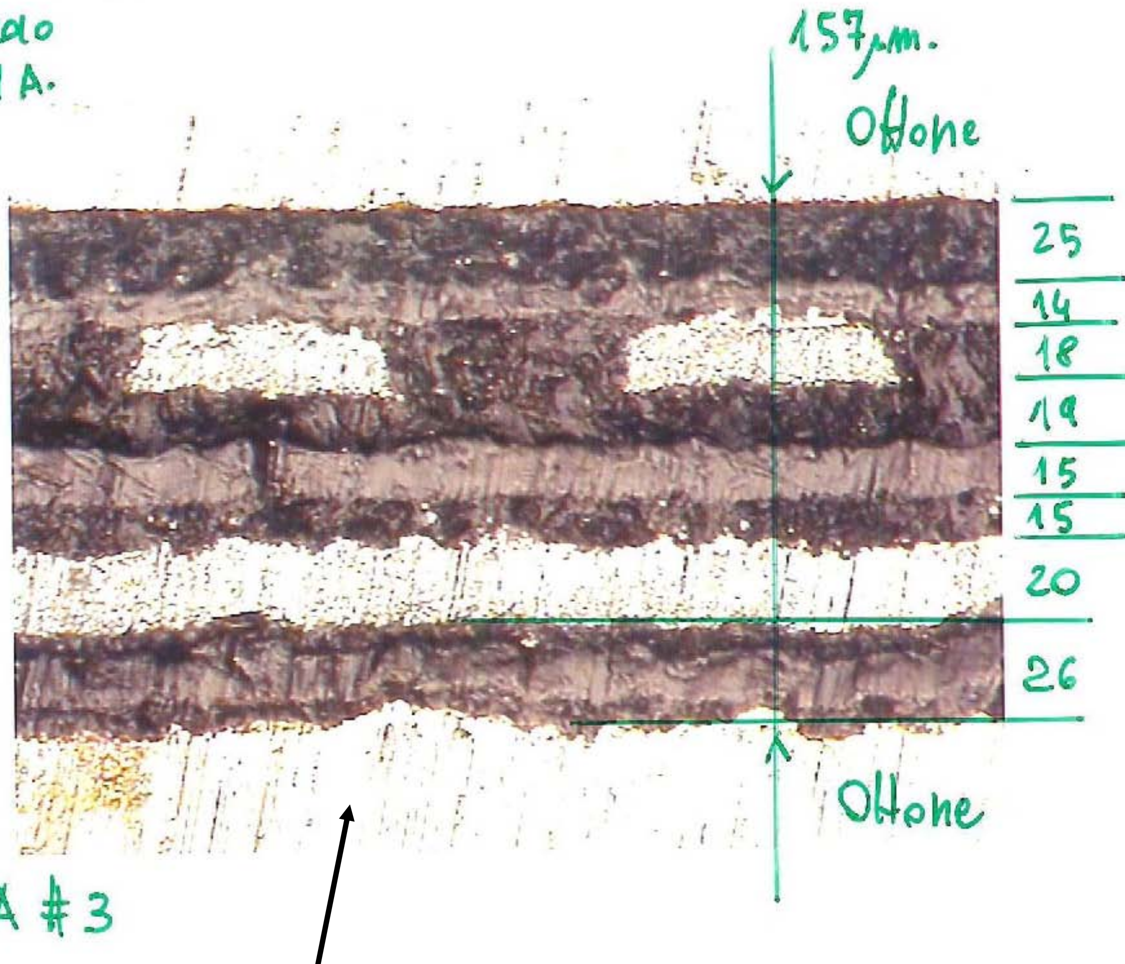
Number of layers: 8
Total thickness = 156 um



NN	Layer Name	Type	Usage	Thickness um	Er
1	TOP-LAYER	Metal	Signal	13	<Auto>
2	Polyimide	Dielectric	Substrate	15	3.5
3	Glue	Dielectric	Substrate	5	4.5
4	INNER-LAYER	Metal	Signal	13	<Auto>
5	Polyimide	Dielectric	Substrate	40	3.5
6	Glue	Dielectric	Substrate	5	4.5
7	GROUND-PLANE	Metal	Plane	50	<Auto>
8	Polyimide	Dielectric	Solder Mask	15	3.5



Analysis of the stack-up



Thanks to F. Bosi and INFN Pisa

- **From CERN estimate**

Layer 1 :soldermask (30um, Dk: 4.5)
Layer 2 : kapton 12.5um
Layer 3 : aluminium 13um (inner layer)
Layer 4 : glue 15um
Layer 5 : kapton 12.5um
Layer 6 : glue 15um
Layer 7 : aluminium 25um (GND plane)
Layer 8 : glue 5um + kapton 12.5um

} !

(only one signal layer is shown)

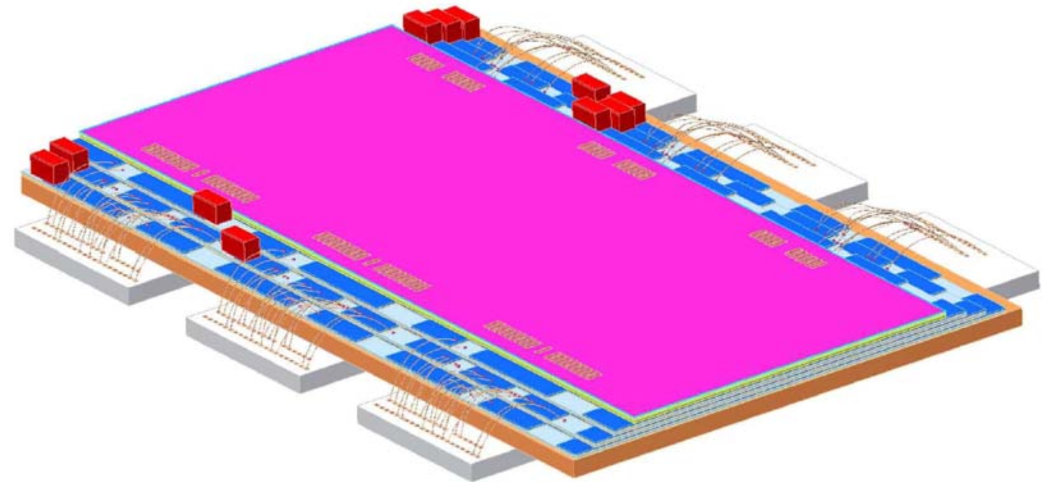
What we understood so far

- **Impedance**
  - Impedance is obtained by increasing glue thickness and NOT by thicker kapton layers
    - ***E***r is different for glue and kapton, dielectric thickness is more → Z moves toward the right value, not exact value yet !!
    - Layer thickness must be carefully measured during stack-up
      - » It will be good practice to measure thickness at each step in production
      - » The kapton layer is always the same (nominal thickness is 12. 5 um)
  - Aluminum signal lines are slightly thicker than expected
  - Trace widht is ~ 75 um, but with some “undercut” due to etching. Trace width could be not uniform → it will explain impedance variation from line to line.
  - Power planes are “polished” before depositing the glue → the effective thickness must be considered for power drop calculation. Thicker planes (50 um or more) can be used but not available at all time.
- **Crosstalk**
  - Not yet understood the extra crosstalk → solder mask properly considered ?
  - We need more cut-out of the bus to evaluate the top metal layer
    - Thanks to Pisa help we will have the info soon

Bus for a 3-chip assembly

Layout of a BUS for up to 3 modules

- using front-end IC "FE 32x128" (expected in the summer)
- Bus widht: 8.7 mm
- Signal trace layer widht: 75 μm
- Bus length ~ 6.5 cm



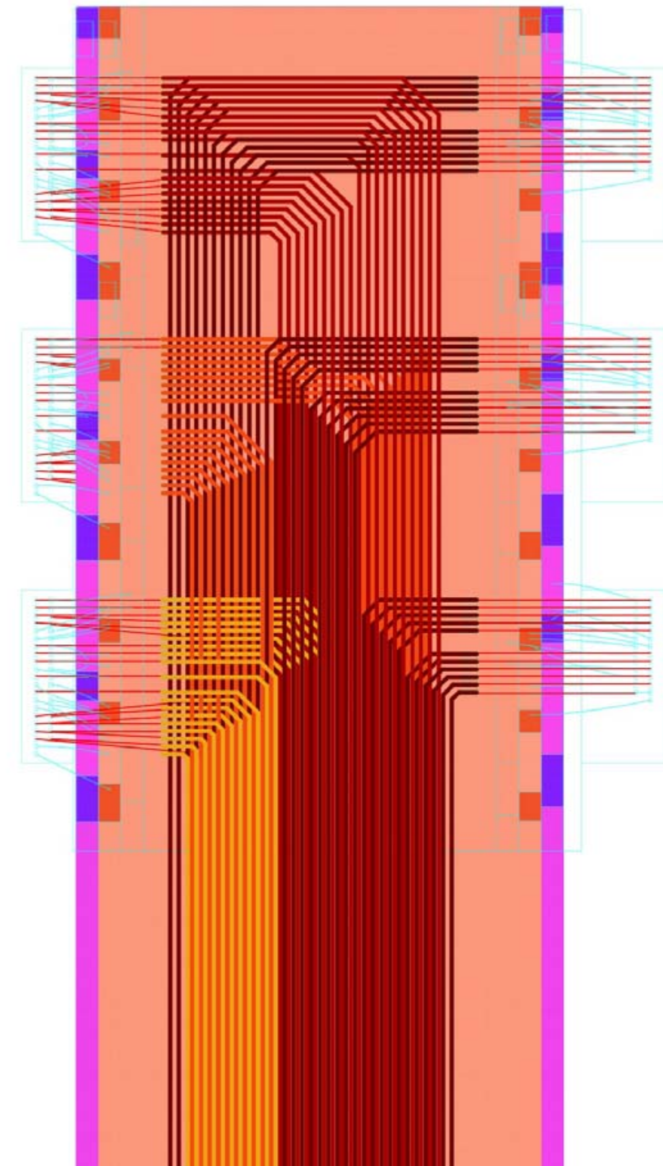
Issues discussed with CERN:

- "Area opening" of 300x500 μm possible on power planes to allow decoupling (cap mounting). Openings will be gold-nickel plated
- Bonding pads will be aluminum. Avoid bimetallic junctions to increase reliability
- Use mesh instead of full layer for power and ground planes → better for X_0

Bus for a 3-chip assembly

Other important design guidelines:

- Each chip will have its own signal data layer
  - 3 chips → 3 layers
  - Same impedance on each data layer (~ 50 Ω, 75 Ω under study)
- Two signal layers are striplines (to decrase crosstalk) the other lines are microstrip (to study two options)
- **To decrease layout complexity no vias will be used**
- 3 power planes + 3 ground planes
  - 2 digital power/ground kept separated to avoid possible interferences
- Data bus layout have been designed to reduce inter-bus capacitive values
- Upgrade to 6 chips will scale accordingly
  - Same number of layers



Signal layers for the 3-chip BUS

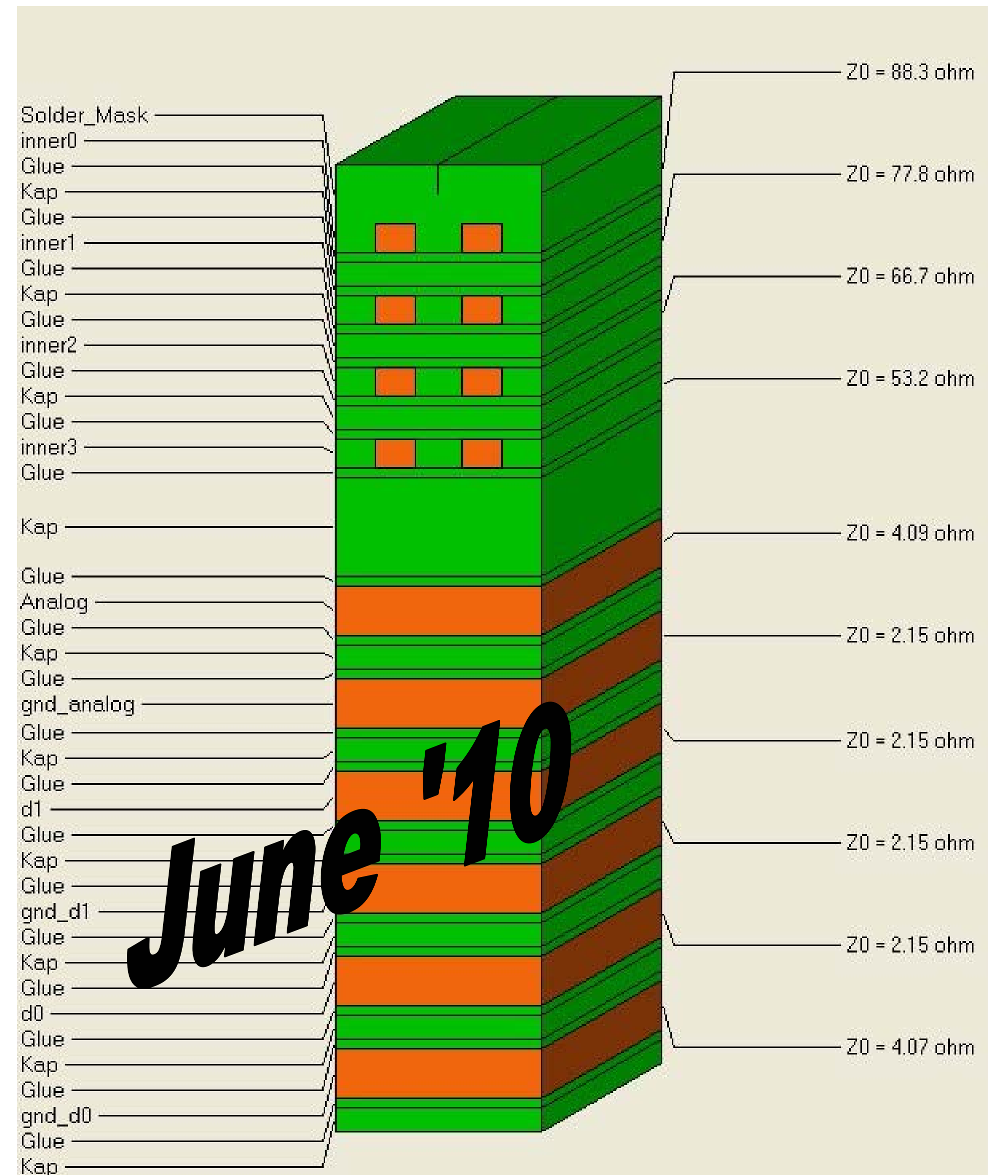
Panasonics high density connectors

Layer 1

Layer 2

Layer 3

Stack-up modification (50 Ω)



1&2
SIGNALS-1
Glue
Kapton
Glue
AVDD
Glue
Kapton
Glue
AGND
Glue
Kapton
Glue
SIGNALS-2
Glue
Kapton
Glue
DVDD_CORE
Glue
Kapton
Glue
DGND_CORE
Glue
Kapton
Glue
SIGNALS-3
Glue
Kapton
Glue
DVDD_MAT
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Glue
DGND_MAT
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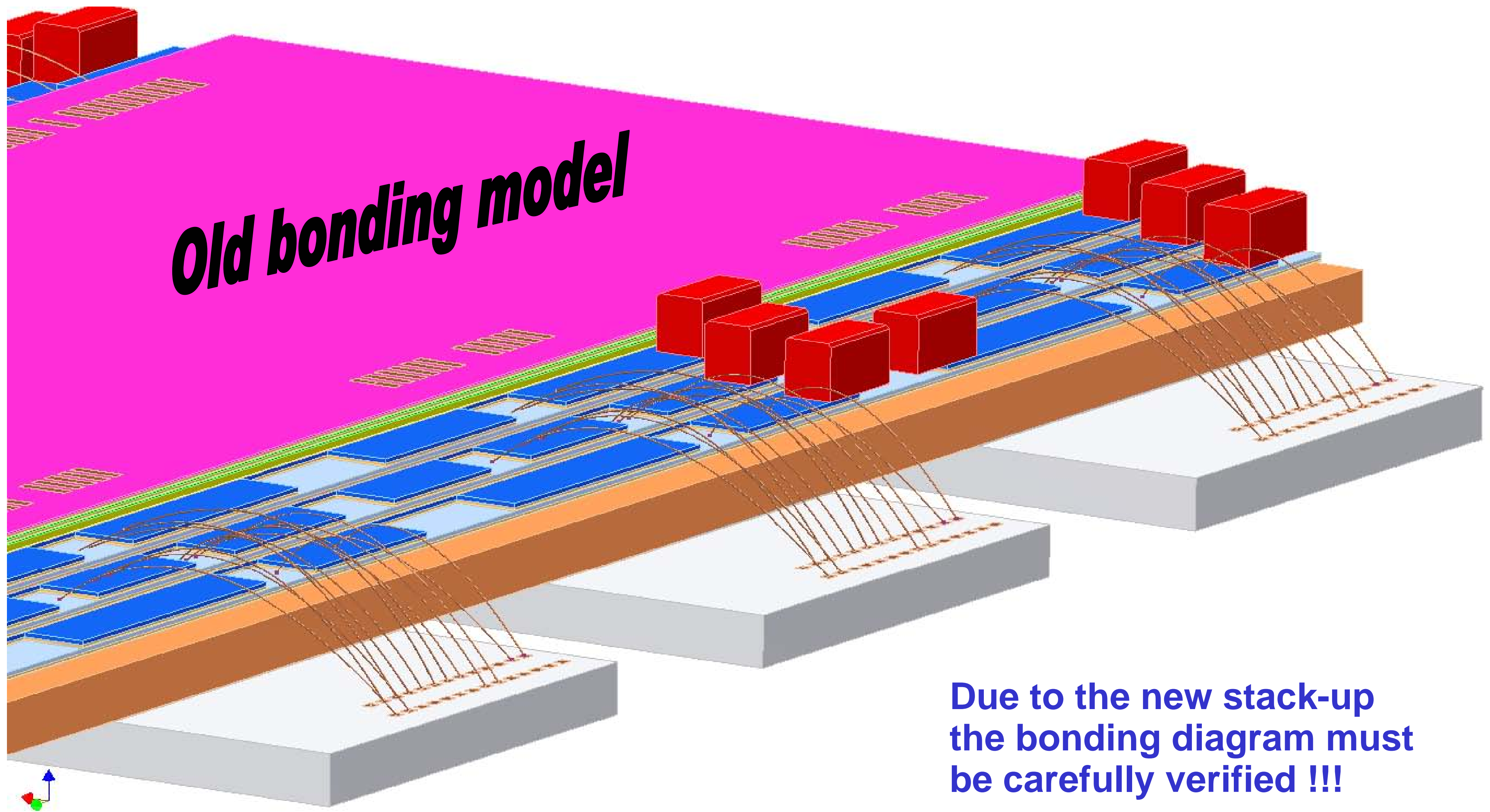
25 um
5 um
12 um

New version

New situation

- Overall thickness increases
  - Due to striplines → overall thickness ~ 800 um
  - Minimal glue thickness (5 um) used only between planes
  - Mesh plane structure (70/30 full/empty) compensate material on average
- Avoiding vias
  - Each layer is prepared and tested independently
  - Stack-up assembled at the last moment → no vacuum deposition
  - No minimum quantity
    - Consider to submit two design versions for comparison
- Redesign status
  - Simulation of new layout will be completed by mid October
  - Bonding layout should be reviewed
    - Bonding pads are not on the uppermost layers anymore
- Production schedule
  - Design/s submitted October → BUS back by end of March ‘11

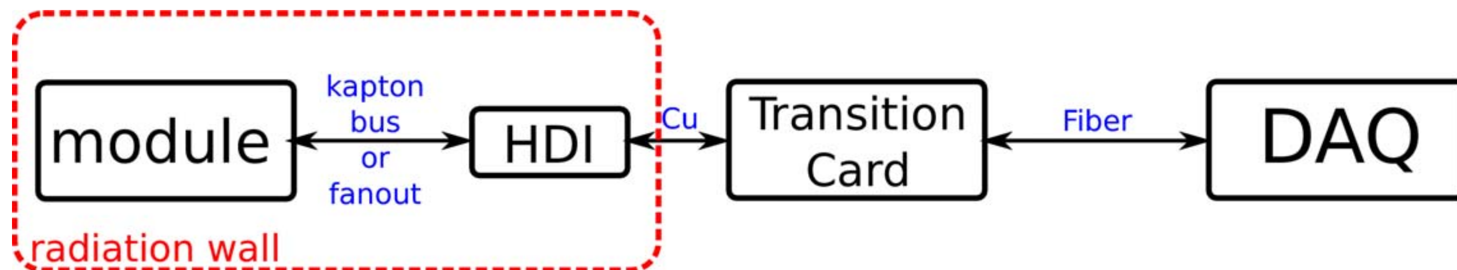
3D Model of the assembly



superB

HDI, transition card development

- Transfer data from **layer0** front-end electronics to DAQ
  - to collect data and program FSSR2 (baseline) or MAPS (upgrade)
  - to store data for 20 μs by means of buffers (hypothesis)
  - to increase robustness using ECC codes and radiation hardening by design ASICs
  - to transfer data at high frequencies (up to 5 Gbps)
  - to re-use similar approach for others layers (with less contraints)

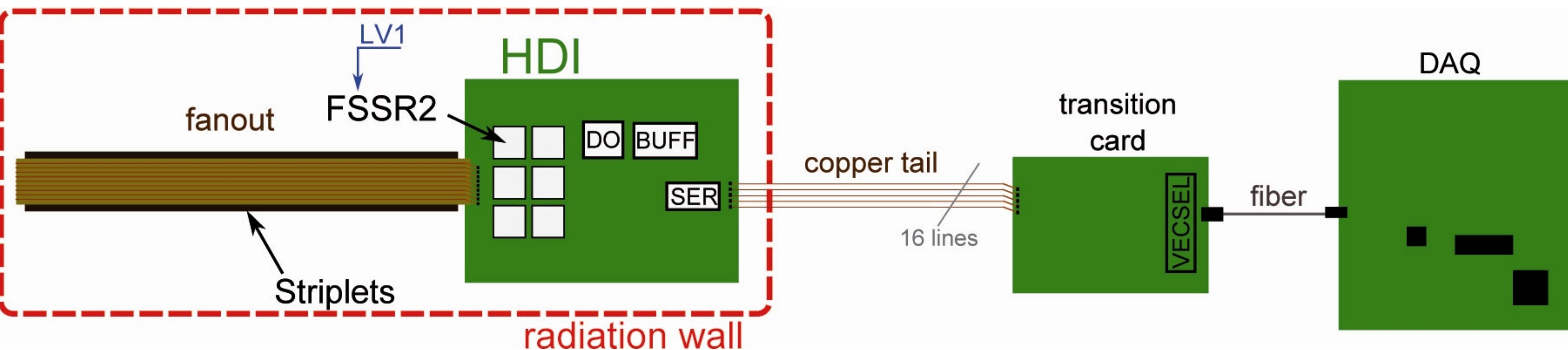


Present Understanding

- At high occupancy **(layer 0)**, FSSR2s are not able to collect data properly
- A triggered solution needs to be implemented in the FSSR2 chips
- For this reason our test/development strategy has moved to a data push-out solution

Main strategy

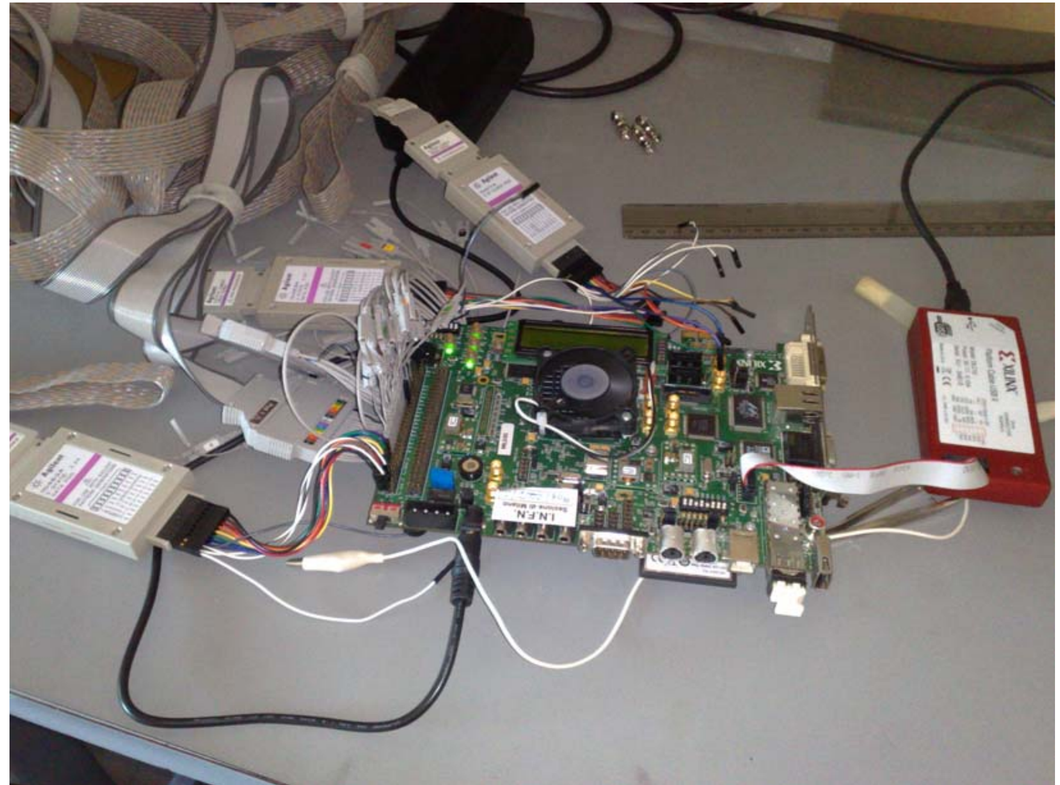
- Usage of a rad-hard IC containing data organizer, buffers, and serializer



HDI size ≈ 1.0 TH x 14.8 W x 70 L mm
Copper tail size ≈ 500 L mm → (≈ 16 lines)
PIX/MAPS: Kapton/aluminum bus size ≈ 0.3 TH x 20 W x 45 L mm → (≈ 100 lines)

HDI prototype

- We have developed a first prototype using a Virtex 5 FPGA
  - Prototype contains:
    - Differential receivers
    - De-serializer
    - Data organizer

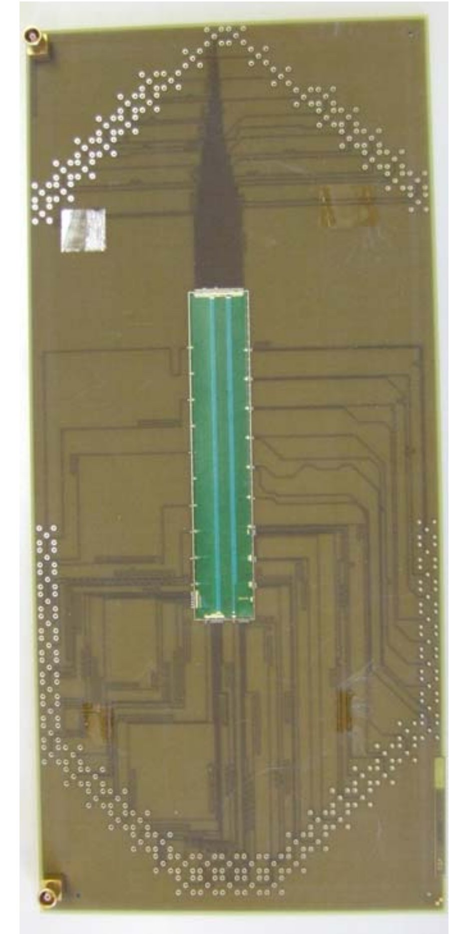


Test of the FPGA prototype

- Extensive tests demonstrate that the Virtex 5 FPGA **prototype works as expected**
  - A C++ program generates data as an FSSR2 will do and data stream is loaded in a Logic State Analyzer (LSA)
  - Such data are then emulated by means of the pattern generator of the LSA
  - The prototype can accept 1,2,6 differential input line
  - The prototype is able to lock on the sync word
  - Data are handled (deserialized, buffered) by the FPGA before sending them back to the LSA for comparison

Next Steps

- **Study data transmission using the prototype BUS**
  - Data sent from the LSA pattern generator through to the FPGA via the BUS lines (differentiall and not)
  - Signal integrity measurements and comparison with simulation
  - Multiple line inejction to study crosstalk and jitter



- **Rad hard Serializer (LOC) 16:1, 5 GBps**
  - ITER export limitation solved
  - Dallas chip expected in the coming weeks
  - LOC will be used instead of FPGA rocketIO