PID meeting

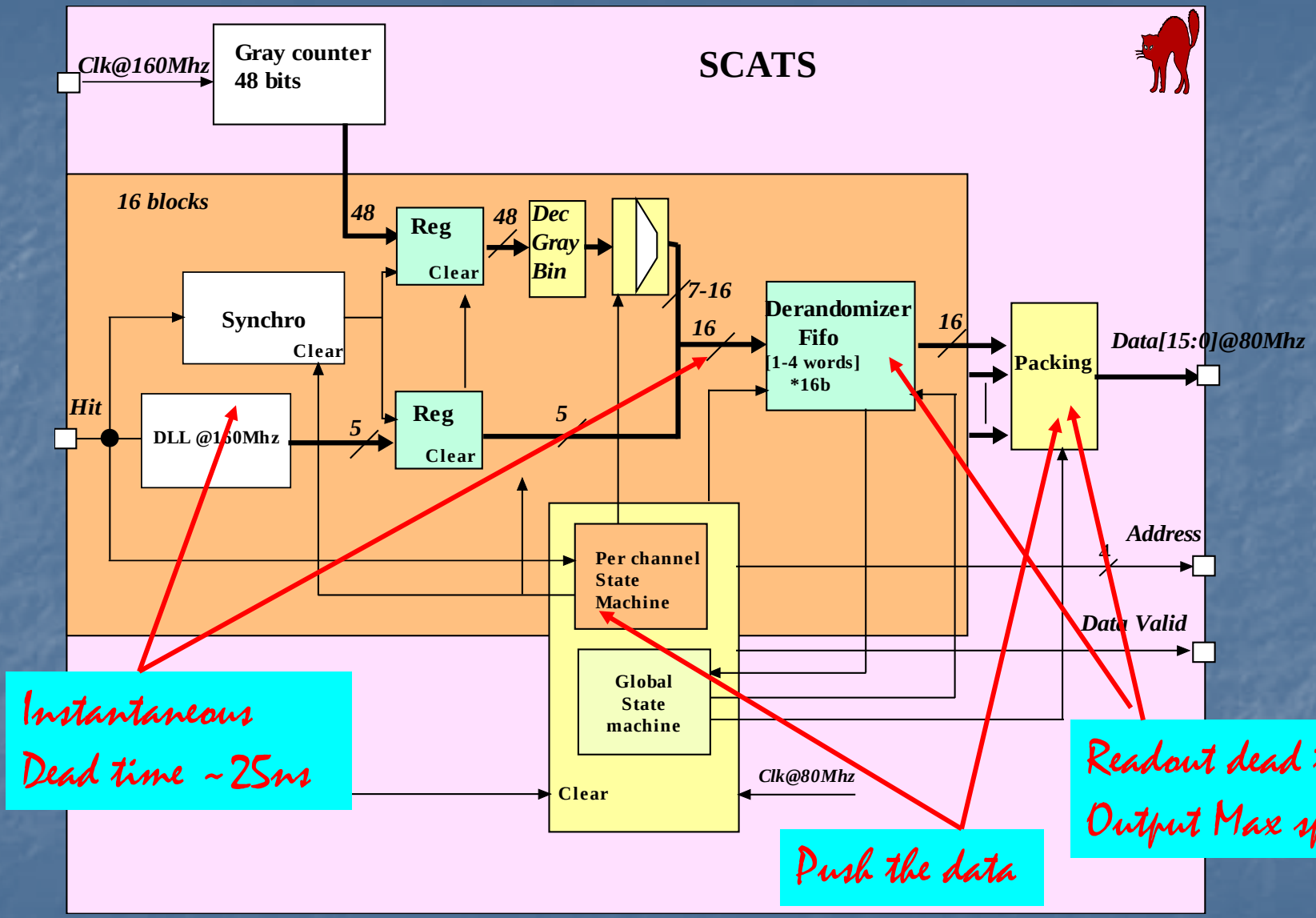
SCATS

Status on front end design

Preliminary simulation of the readout part

Next steps

SCATS


SCATS
Clk@160Mhz
Gray counter
48 bits
16 blocks
48
Reg
Clear
48
Dec
Gray
Bin
7-16
16
Derandomizer
Fifo
[1-4 words]
*16b
16
Packing
Data[15:0]@80Mhz
Synchro
Clear
Hit
DLL @160Mhz
5
Reg
Clear
5
Per channel
State
Machine
Address
4
Data Valid
Global
State
machine
Clk@80Mhz
Clear
Instantaneous
Dead time ~25ns
Push the data
Readout dead time
Output Max speed ~20 M

Performances

Already measured : Resolution , Linearity ... => SNATS matches our requirements.

Expected :

Dead time at the input : 25 ns. Matches the background input max frequency with a a large safety factor

Readout :

Number of data words per event	4	3	2	1
Readout frequency per channel (All channels fired)	1,25 MHz		2,5 MHz	**5 MHz**
Max readout frequency per channel (only one channel fired)	5 MHz		10 MHz	**20 MHz**

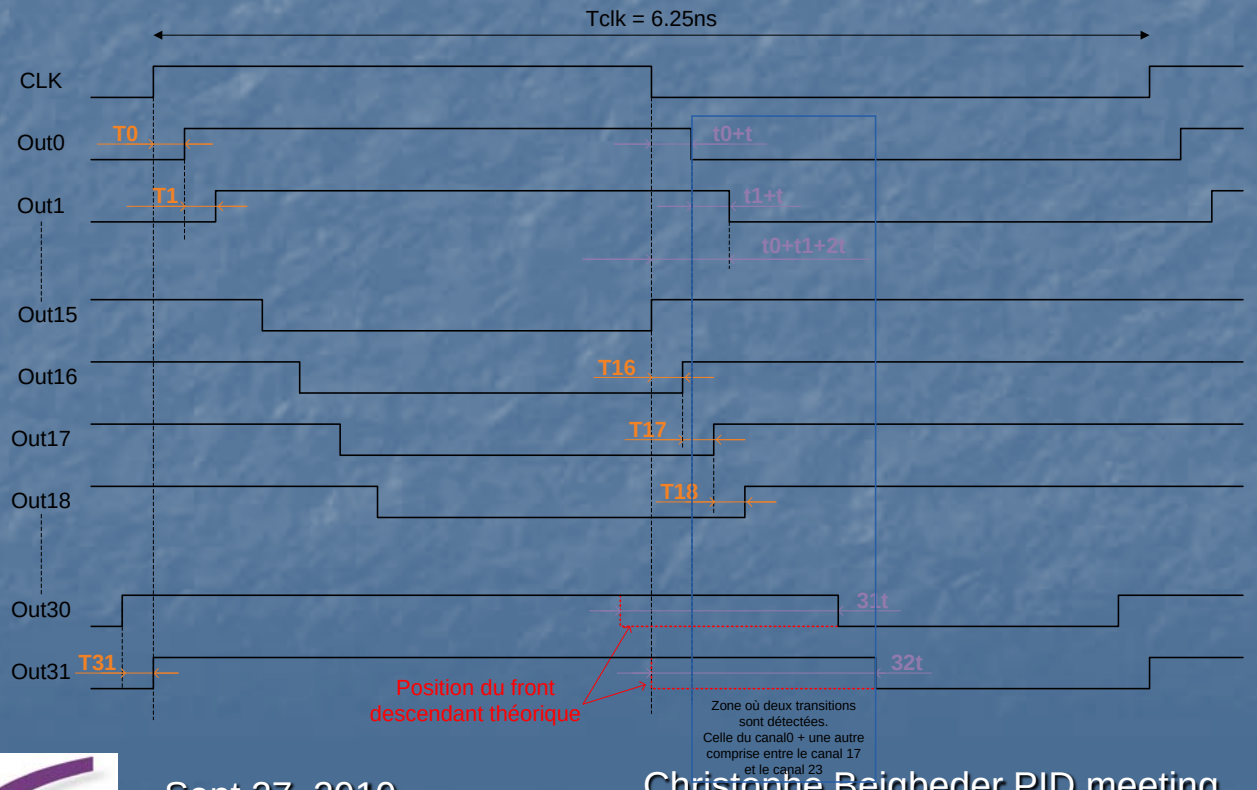
Match the 70ns and 150 KHz Trigger requirements.
The complete chain up to the sector concentrator has to mach the 4 us trigger latency.

Front end Upgrade

Gray encoder : scheme, simulation & layout : done

- Shift by « 1 »
  - ↳ New design of the ouputs

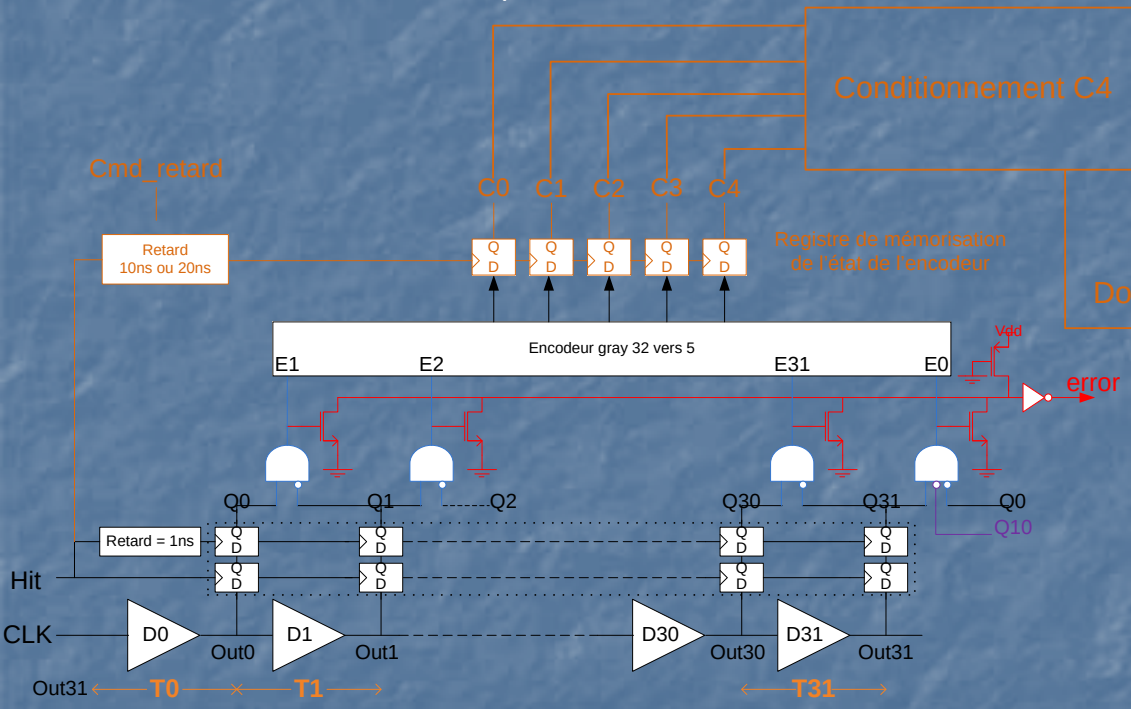
- New design of the canal zero



Front end Upgrade

Matching between DLL & counter (Synchronizer) :

- New conditions implemented
  - If canal 31 with 2 hits coarse ⇨ canal 0
  - If canal 0 with 1 hit coarse ⇨ canal 31



Scheme, simulation & layout : done

Layout to finish

Front end Upgrade

Input channel inhibit :

- Inhibition of the channel input
  - ↳ check the state of the input stage in the Hit synchroniser

Scheme, simulation & layout done

Readout bus for the time registers

- 16 independant channels:
  - ↳16x 16 bit tri state bus (4 commands) to multiplex 4 x 16 bit registers

Schemes done & Layout under design

Front end Upgrade

DLL :

- Problem on the bloc lock control:
  - ↳ sensitivity of the lock of the DLL to the duty cycle

Scheme, simulation & layout done

Test :

- Do we keep the possibility to visualise the charge pump output .
  - ↳ New analog buffer to be designed

nothing done

Front end Upgrade

LVDS receiver :

- Differential input stage (NMOS)
  - ↳ Scheme, simulation & Layout to be done

- Redesign of the hit output buffer :
  - ↳ Buf15 from vendor library corelib3B (existing solution)

- Power supplies has to be separated between hits et clk:
  - ↳ Schemes, simulation & Layout to be done

- Signal input polarity selection :
  - ↳ Schemes, simulation & Layout to be done

Front end Upgrade

others:

- Suppression of the test channel

  Schemes done ; Layout to be done

- More configuration bits needed for setup

  ↳ new setup registers

  Schemes, simulation et Layout to be done

Readout Upgrade

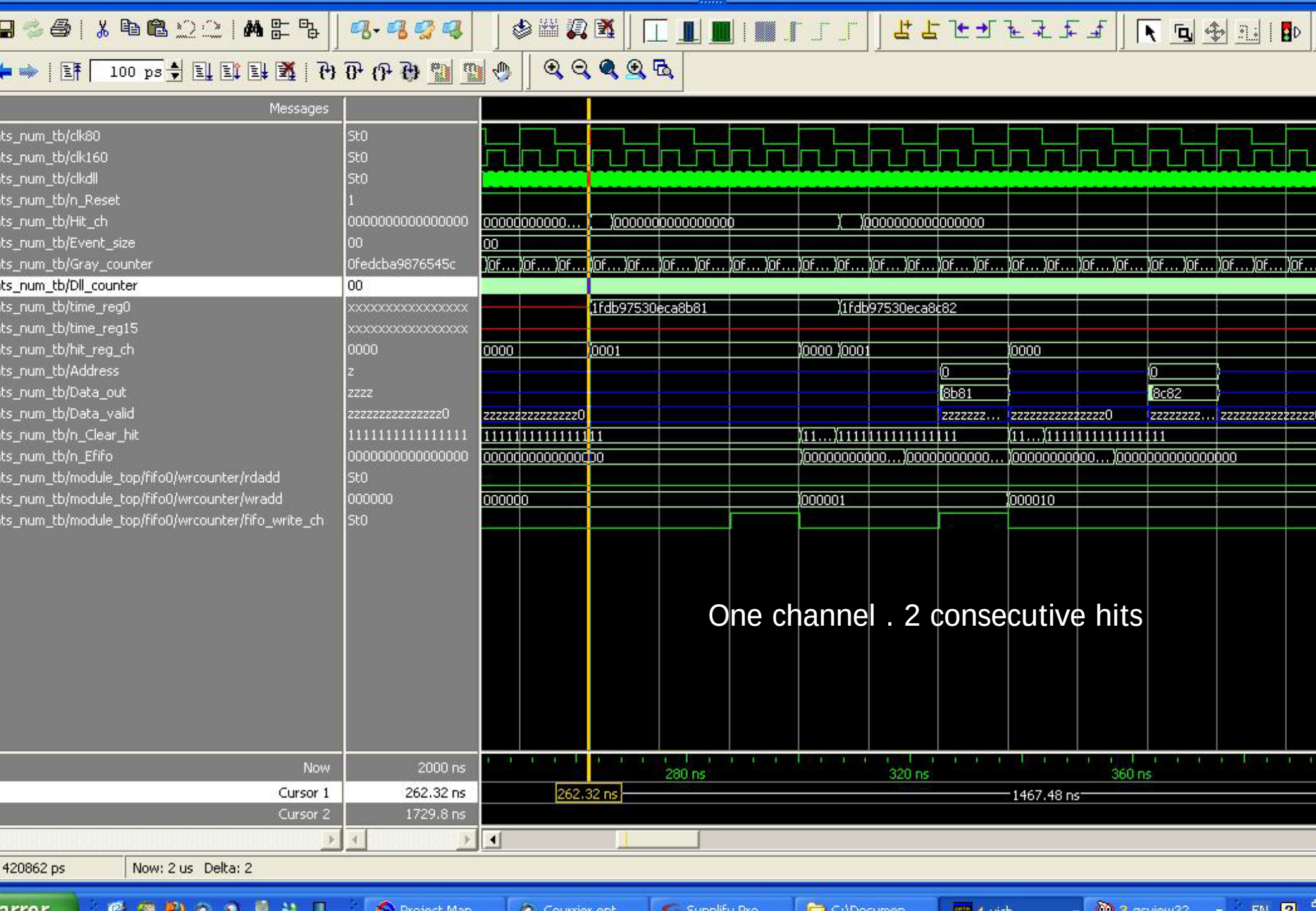
Design of the readout part is done in Verilog

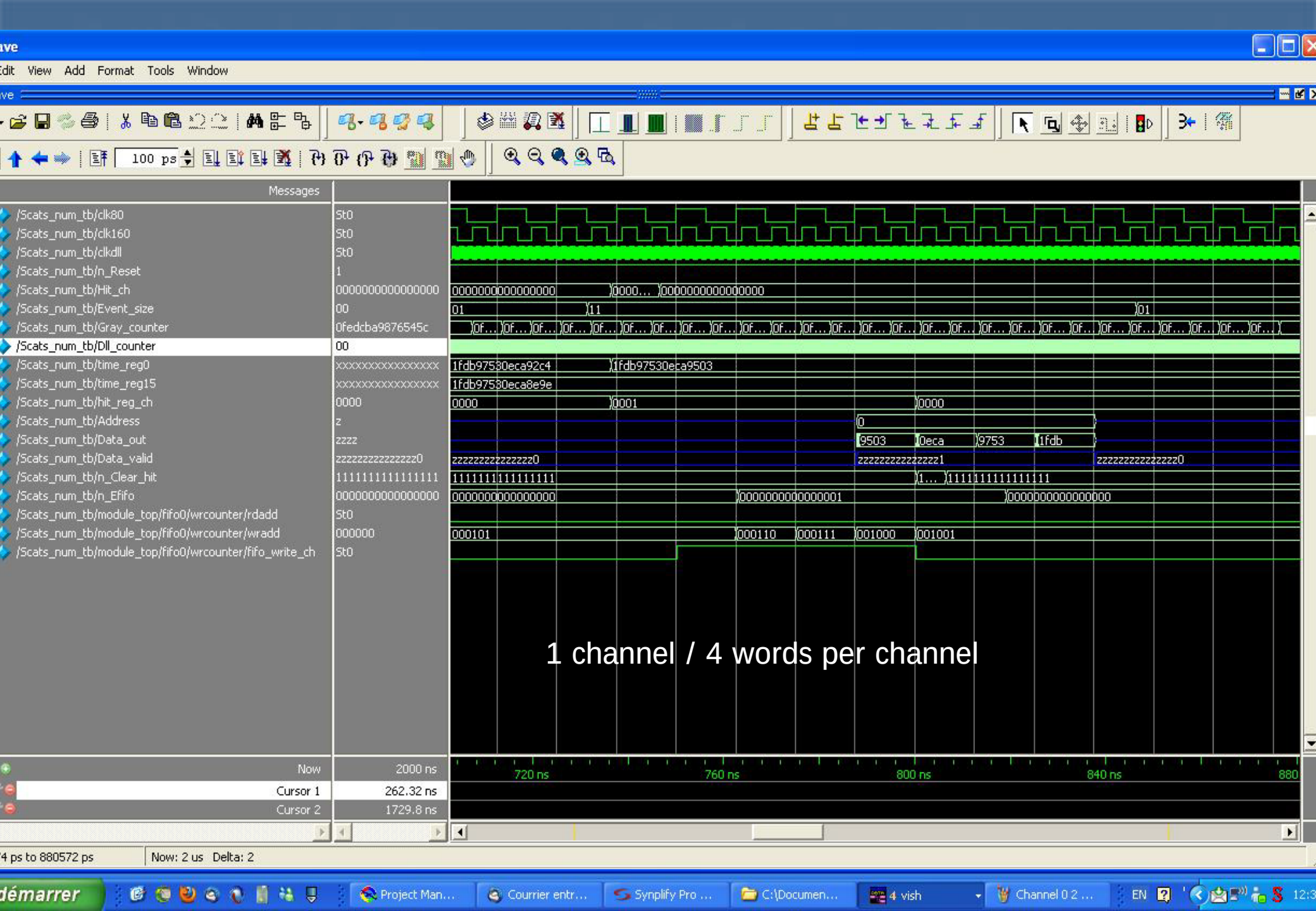
- First step :
  - targeted in a Actel family FPGA in order to have a first post synthese evaluation of the performance .
  - first level simulation

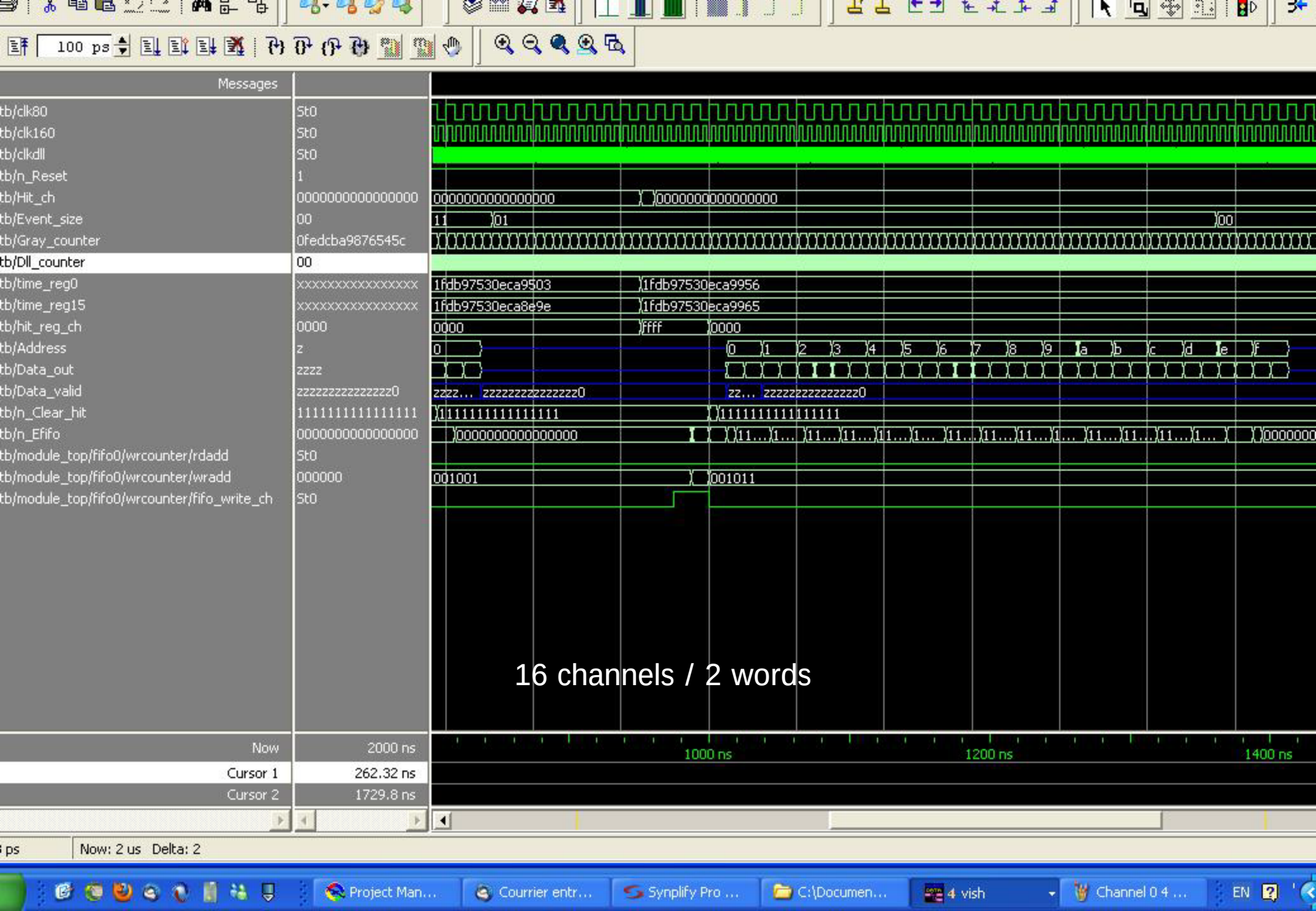
- Ram size : 16 bits x 1 up to 4 words per event x 16 or 32 or … events per channel .

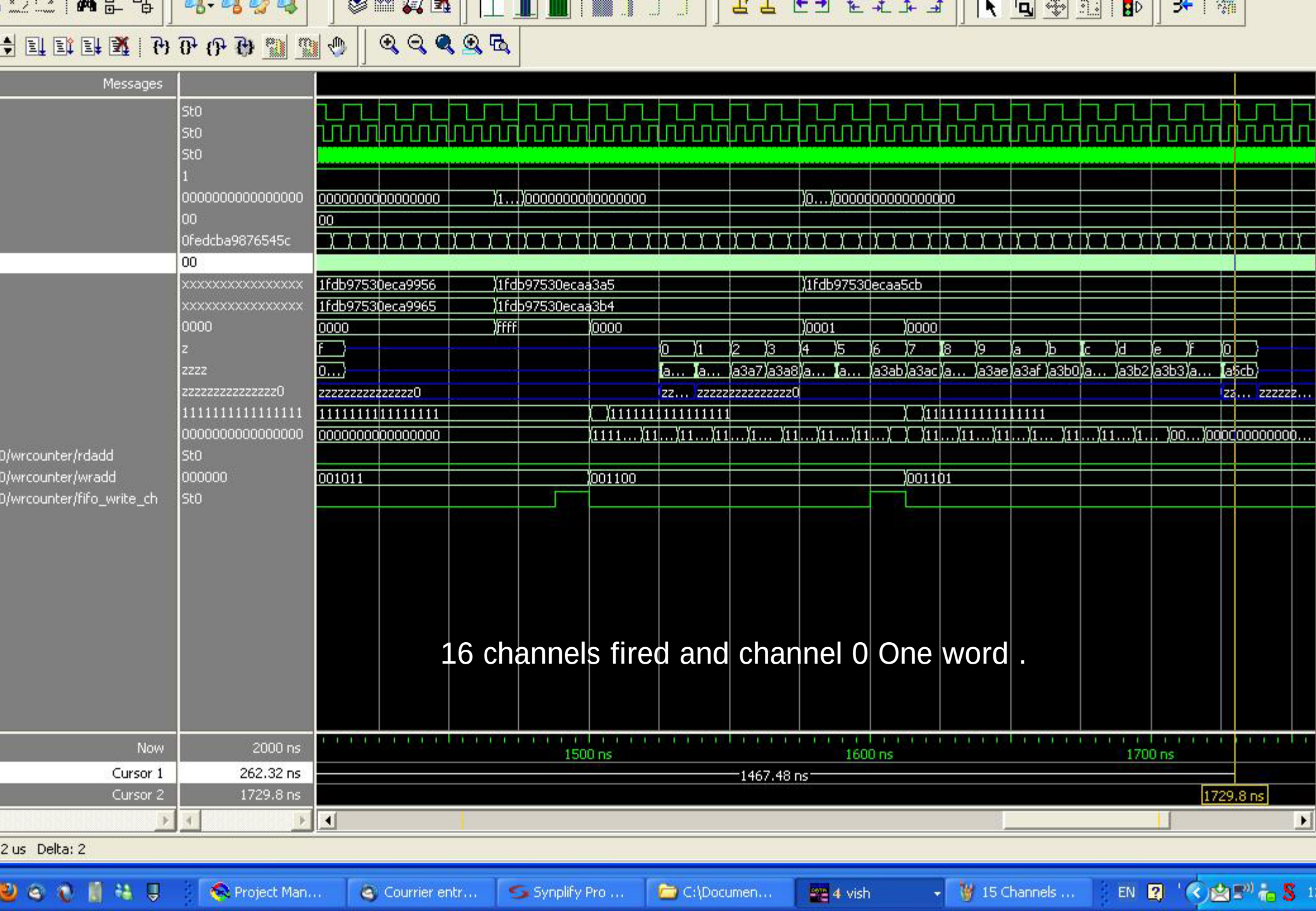
  ➔**The size has to be define very soon** to order the Ram to the vendor and start the design with Cadence design kit.

- Next step:
  - readout behavior simulation with :
    - ➢50 ns input dead time (max expected performance)
    - ➢40 KHz readout frequency per channel
    - ➢80 MHz deasy chain readout scrutation
    - ➢150 KHz input noise with the good distribution law…


Messages
ts_num_tb/clk80
ts_num_tb/clk160
ts_num_tb/clkdll
ts_num_tb/n_Reset
ts_num_tb/Hit_ch
ts_num_tb/Event_size
ts_num_tb/Gray_counter
ts_num_tb/Dll_counter
ts_num_tb/time_reg0
ts_num_tb/time_reg15
ts_num_tb/hit_reg_ch
ts_num_tb/Address
ts_num_tb/Data_out
ts_num_tb/Data_valid
ts_num_tb/n_Clear_hit
ts_num_tb/n_Efifo
ts_num_tb/module_top/fifo0/wrcounter/rdadd
ts_num_tb/module_top/fifo0/wrcounter/wradd
ts_num_tb/module_top/fifo0/wrcounter/fifo_write_ch
St0
1
0000000000000000
00
0fedcba9876545c
xxxxxxxxxxxxxxxx
0000
z
zzzz
zzzzzzzzzzzzzzz0
1111111111111111
000000
1fdb97530eca8b81
1fdb97530eca8c82
8b81
8c82
000001
000010
One channel . 2 consecutive hits
Now
2000 ns
Cursor 1
262.32 ns
Cursor 2
1729.8 ns
280 ns
320 ns
360 ns
1467.48 ns
420862 ps
Now: 2 us Delta: 2


Edit View Add Format Tools Window
100 ps
Messages
/Scats_num_tb/clk80
/Scats_num_tb/clk160
/Scats_num_tb/clkdll
/Scats_num_tb/n_Reset
/Scats_num_tb/Hit_ch
/Scats_num_tb/Event_size
/Scats_num_tb/Gray_counter
/Scats_num_tb/Dll_counter
/Scats_num_tb/time_reg0
/Scats_num_tb/time_reg15
/Scats_num_tb/hit_reg_ch
/Scats_num_tb/Address
/Scats_num_tb/Data_out
/Scats_num_tb/Data_valid
/Scats_num_tb/n_Clear_hit
/Scats_num_tb/n_Efifo
/Scats_num_tb/module_top/fifo0/wrcounter/rdadd
/Scats_num_tb/module_top/fifo0/wrcounter/wradd
/Scats_num_tb/module_top/fifo0/wrcounter/fifo_write_ch
1 channel / 4 words per channel
Now
Cursor 1
Cursor 2
2000 ns
262.32 ns
1729.8 ns
720 ns
760 ns
800 ns
840 ns
880
Now: 2 us Delta: 2
démarrer
Project Man...
Courrier entr...
Synplify Pro ...
C:\Documen...
4 vish
Channel 0 2 ...
EN


Messages
tb/clk80
tb/clk160
tb/clkdll
tb/n_Reset
tb/Hit_ch
tb/Event_size
tb/Gray_counter
tb/Dll_counter
tb/time_reg0
tb/time_reg15
tb/hit_reg_ch
tb/Address
tb/Data_out
tb/Data_valid
tb/n_Clear_hit
tb/n_Efifo
tb/module_top/fifo0/wrcounter/rdadd
tb/module_top/fifo0/wrcounter/wradd
tb/module_top/fifo0/wrcounter/fifo_write_ch
16 channels / 2 words
Now
2000 ns
Cursor 1
262.32 ns
Cursor 2
1729.8 ns
1000 ns
1200 ns
1400 ns
Now: 2 us Delta: 2


Messages
St0
St0
St0
1
0000000000000000
00
0fedcba9876545c
00
xxxxxxxxxxxxxxxx
xxxxxxxxxxxxxxxx
0000
z
zzzz
zzzzzzzzzzzzzzz0
1111111111111111
0000000000000000
0/wrcounter/rdadd
0/wrcounter/wradd
0/wrcounter/fifo_write_ch
St0
000000
St0
1fdb97530eca9956
1fdb97530eca9965
0000
ffff
0001
1fdb97530ecaa3a5
1fdb97530ecaa3b4
1fdb97530ecaa5cb
001011
001100
001101
16 channels fired and channel 0 One word .
Now
2000 ns
Cursor 1
262.32 ns
Cursor 2
1729.8 ns
1500 ns
1600 ns
1700 ns
1467.48 ns
1729.8 ns
2 us Delta: 2
Project Man...
Courrier entr...
Synplify Pro ...
C:\Documen...
4 vish
15 Channels ...
EN

Next steps

- Complete simulation tests.

  - Comportemental behavior model (Verilog, C. VHDL)
    - Readout part in Actel FPGA for 16 channels
  - Gate level simulation of one complete channel (fine + coarse TDC + readout)

- Ram implementation:
  - ensure size compatibility between Ram & FE channel heights

- Error bit in the first word

- New output buffer for data bus to the FPGA

- Integration of a 2nd gray counter (SEU)

- Output fifo bypass in test mode

Milestones

- Submission:

  - Shared wafer in a dedicated run (with IRFFU): very end of Dec. 2010

  or

  - MPW run: beginning of Dec. 2010

- 1rst prototype: around 3 months later.