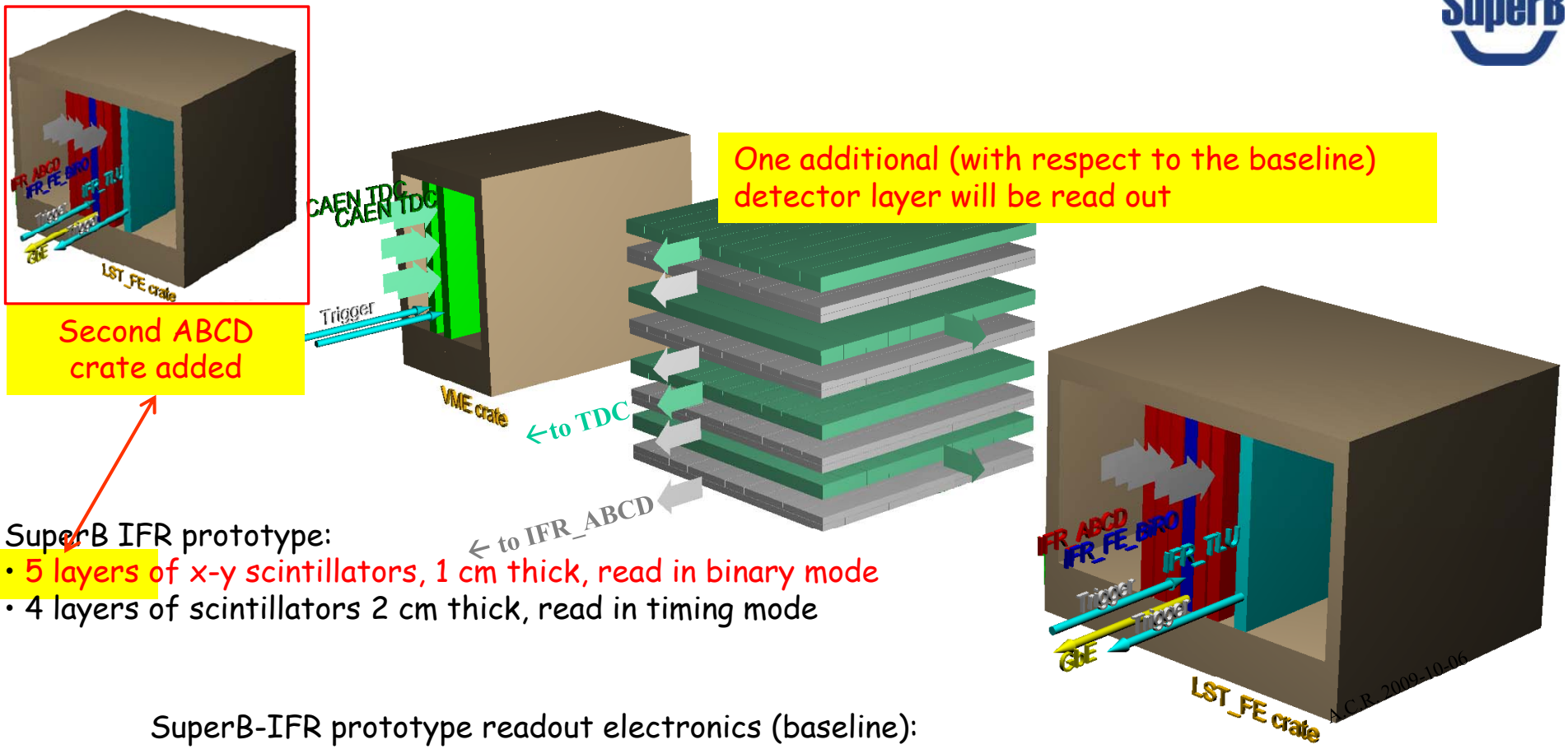
SuperB IFR electronics: update on prototype electronics and IFR_DAQ

Overview

- update on the development of the IFR prototype electronics and DAQ system

SuperB IFR electronics : update on prototype electronics and DAQ



SuperB IFR prototype:

- 5 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

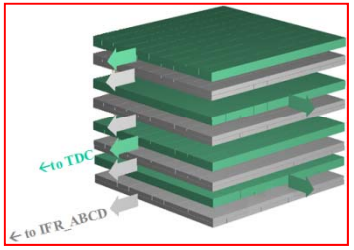
SuperB-IFR prototype readout electronics (baseline):

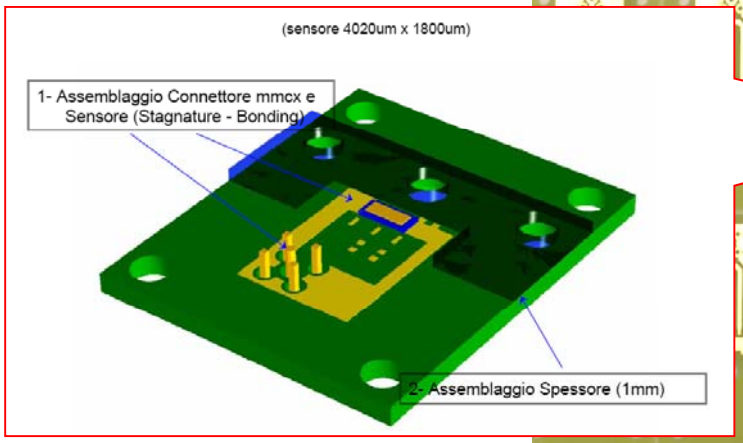
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing:
  it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

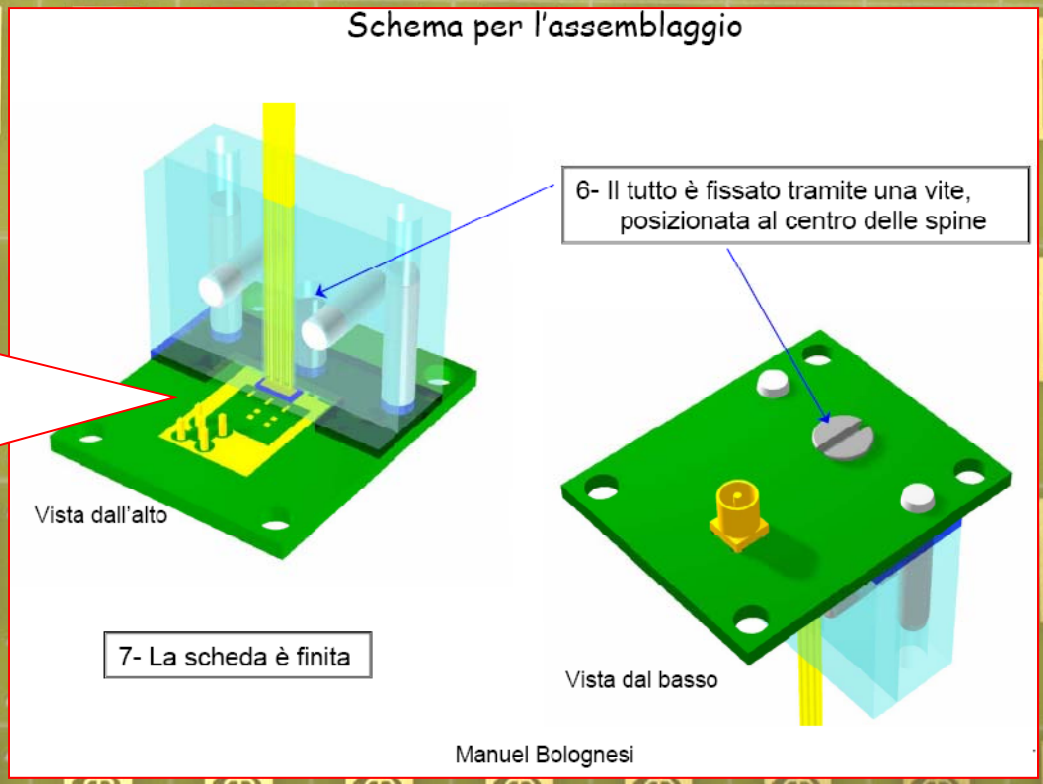
IFR_FE_BiRO + IFR_TLU are now a single module

SuperB IFR electronics : update on prototype electronics and DAQ

SiPM carrier PCB





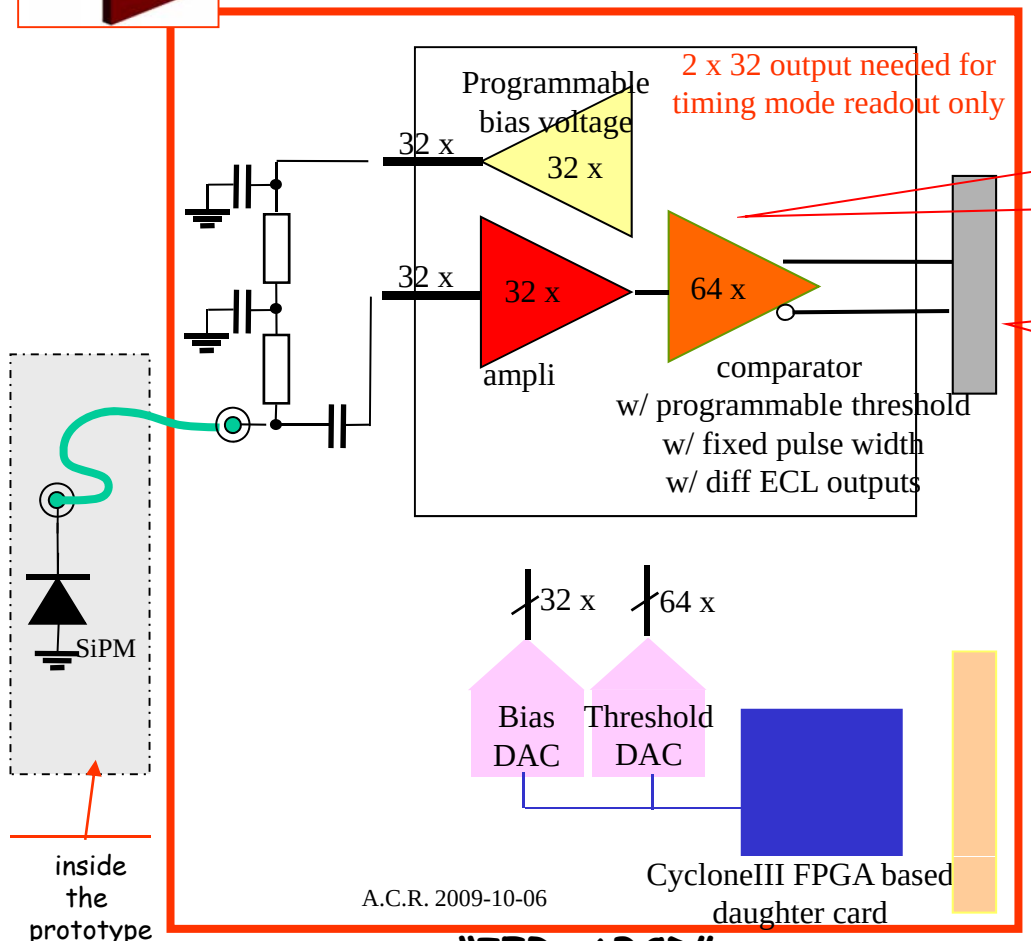


SiPM carrier PCB with NiAu plating for bonding: fits all three type of sensors being manufactured by FBK-Trento.
Sensor die gluing position is determined by a countermask.

Status:
- all parts needed have been delivered
- SiPM bonding is ongoing at INFN-Perugia thanks to Dr. Giovanni Ambrosi and Dr. Maria Ionica
- bonded SiPM already delivered to INFN-Ferrara are being characterized

SuperB IFR electronics : update on prototype electronics and DAQ

dimensions: VME 6U x 220mm



Outline of the **"IFR_ABCD"** card

(**A**mplifier, **B**ias, **C**omparator,**D**ataProcessing)

"IFR_ABCD" card features:

- ampli: two stage w/discrete components: BGA2748 + BGA2716
- discri: ADCMP563BRQ (ECL out, dual)

For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

- DAC: LTC2625CGN#PBF (I^2C, 12bit, octal)
- FPGA: Cyclone III ALTERA EP3C25Q240C8

"IFR_ABCD" needed for prototype readout :

1 for each of 4 BiRO planes (readout at only one end of scintillator) +

1 for each of 4 planes read with TDCs (readout at both ends of scintillator)

TOTAL "IFR_ABCD" cards: 8

TOTAL "IFR_ABCD" cards produced: 12

(to enable the reading of a 9th prototype layer + spares)

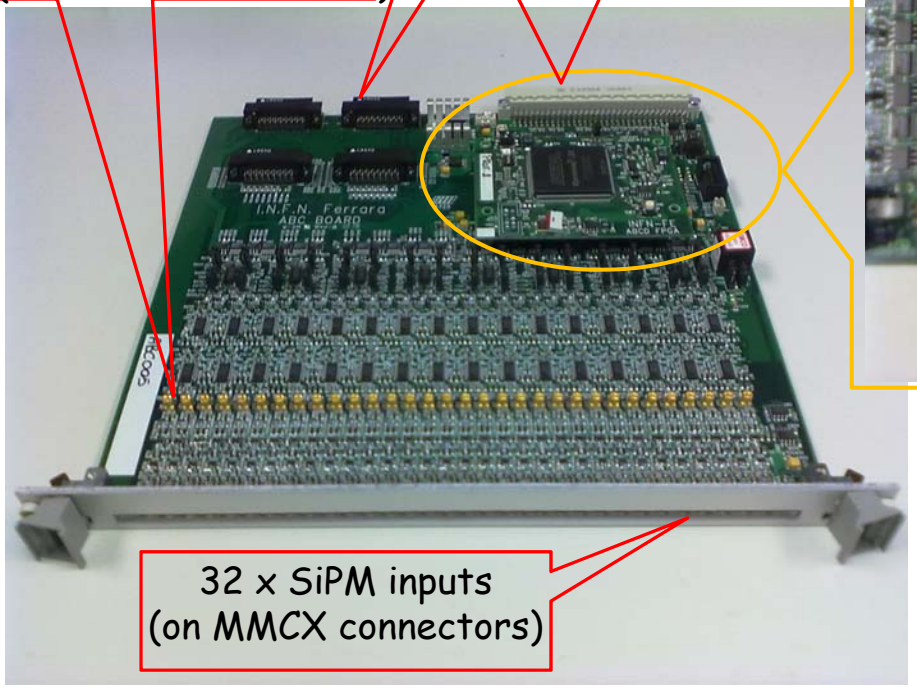
IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by **R. Malaguti,** INFN-Ferrara

SuperB IFR electronics : update on prototype electronics and DAQ

16 pairs x 4 P-ECL outputs to the TDCs

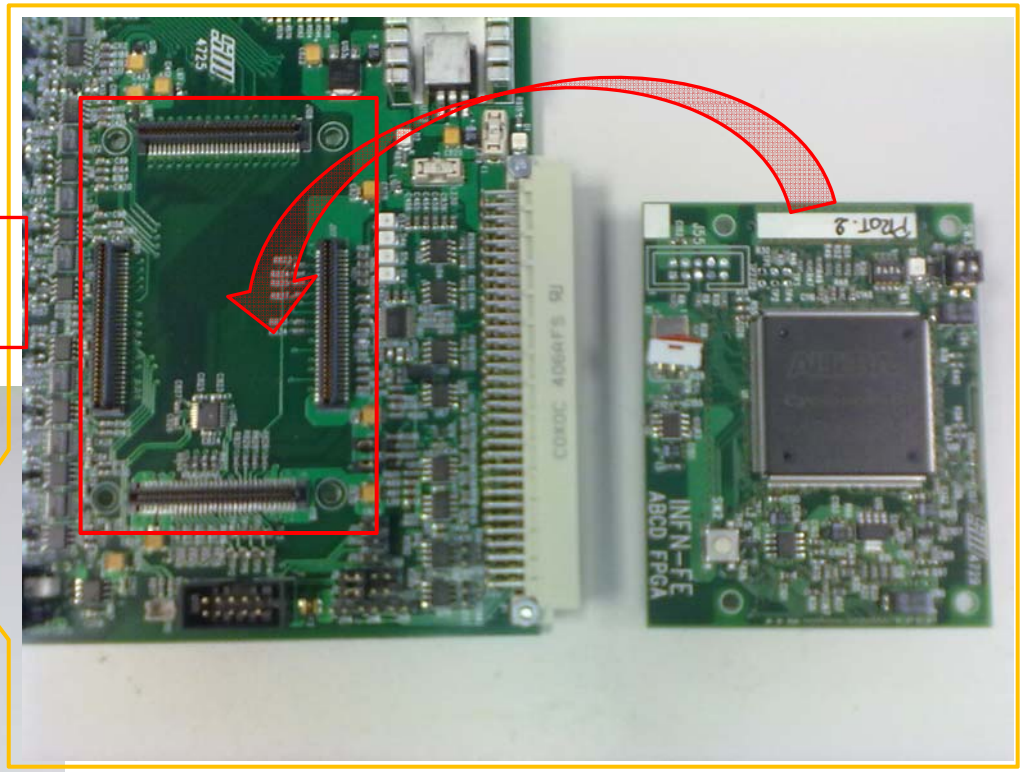
32 x monitor outputs (analog) from the amplifiers (on MMCX connectors)

96 pin DIN connector to the backplane



32 x SiPM inputs (on MMCX connectors)

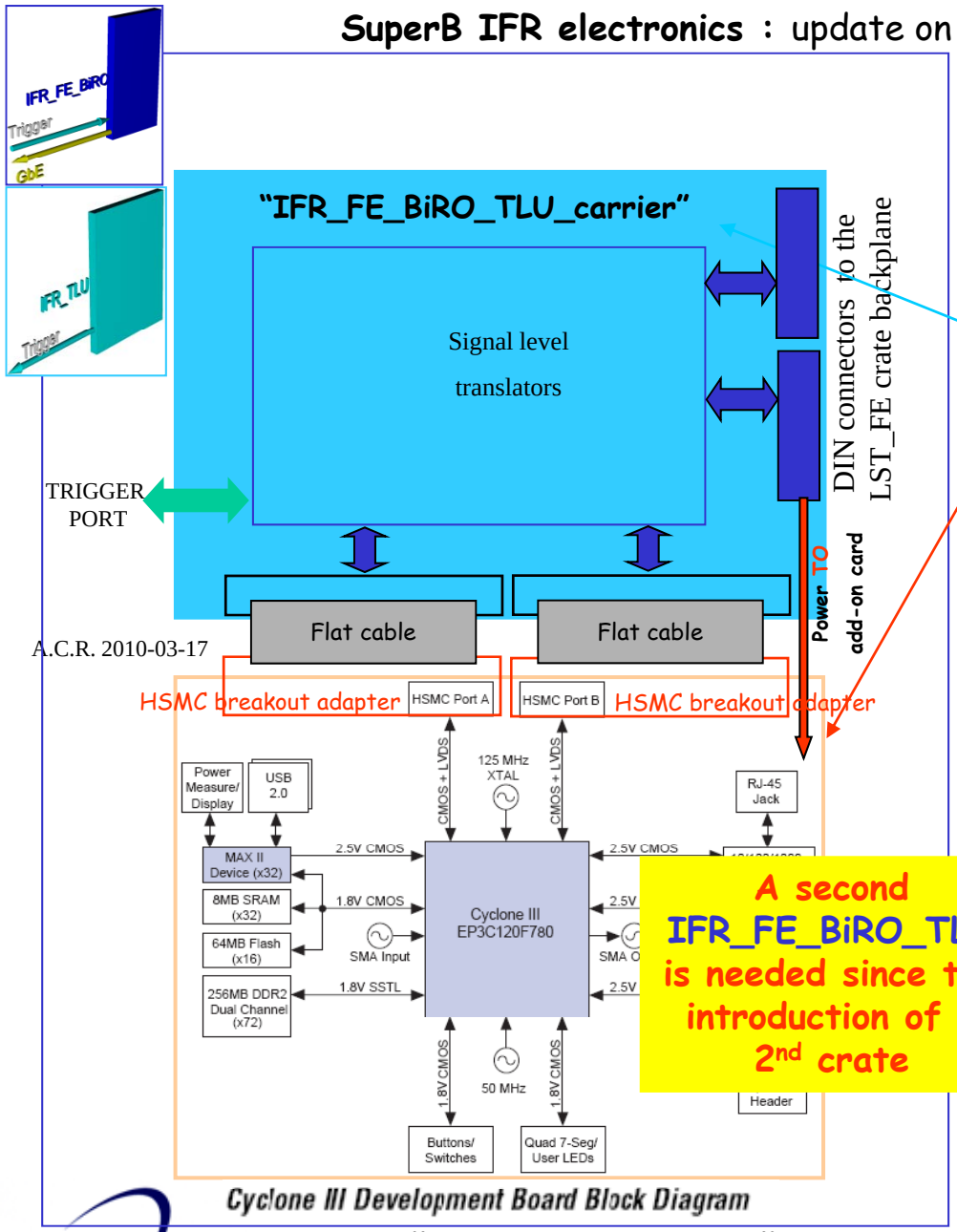
"IFR_ABCD" card



Detail of the digital "IFR_ABCD" daughter card

"IFR_ABCD" status update :

- 8 boards delivered and tested
- 4 boards expected in TWO WEEKS



Outline of the "IFR_FE_BiRO_TLU" module

A second IFR_FE_BiRO_TLU is needed since the introduction of a 2nd crate

"IFR_FE_BiRO_TLU" module features **(new)**:

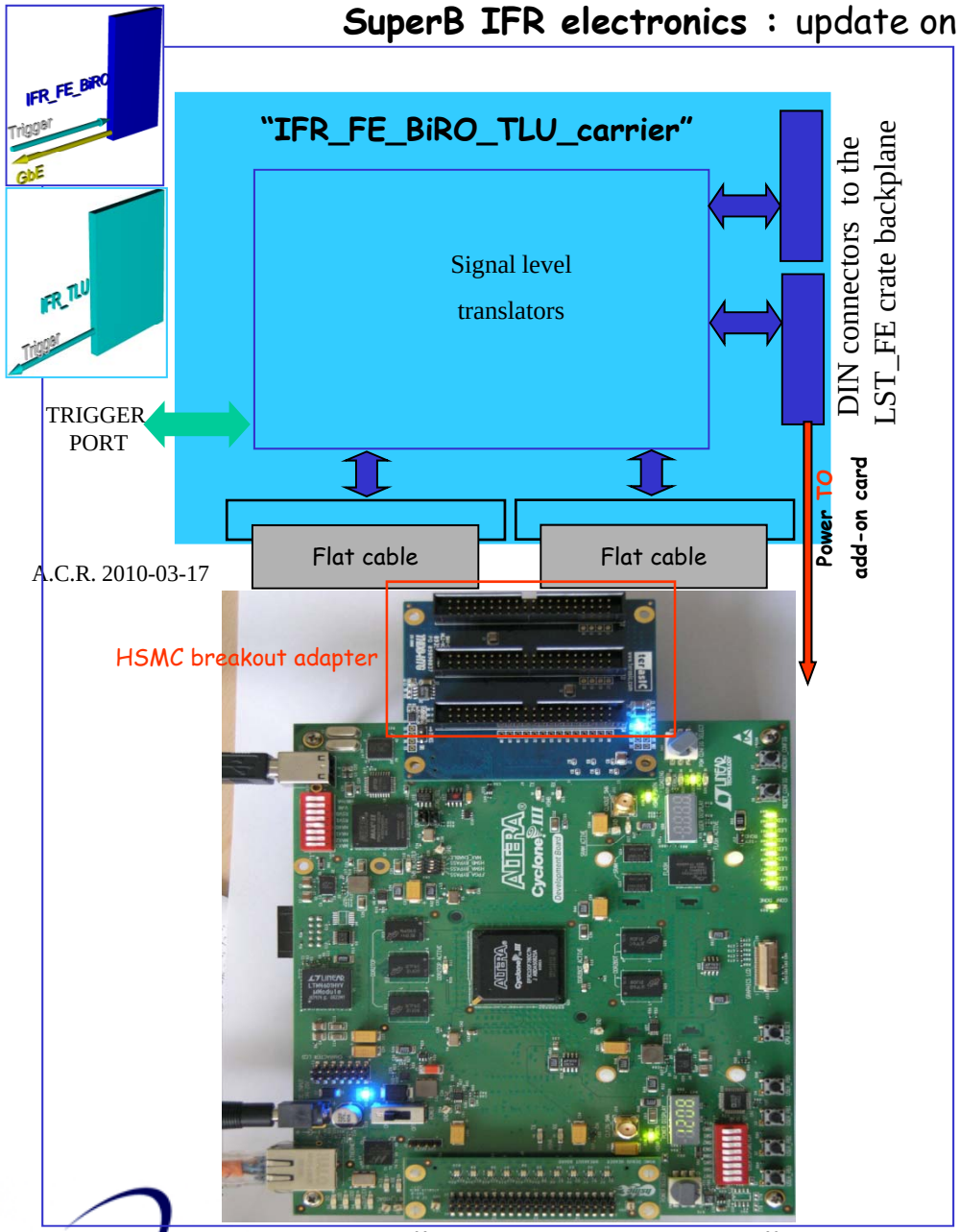
The functions of the IFR_FE_BiRO and of the IFR_FE_TLU cards are combined into a single system made of

- a **carrier** card which fits in the "LST_FE" crate (6U x 220mm depth)
- an **add-on** card : it's simply the ALTERA Cyclone III development kit (**DK-DEV-3C120N**) equipped with breakout adapters for the kit's HSMC connectors

The **carrier** card hosts level adaptors and application specific I/O ports which allow the **add-on** card to:

- receive power
- receive the "fast OR" signals from the "ABCD" cards to generate triggers from
- generate and distribute triggers (also to the TDC system)
- generate and distribute clock and reset signals (also to the TDC system)
- poll data from the "ABCD" cards
- configure the programmable resources on the "ABCD" cards
- connect to the host PC running the DAQ software via ethernet (tcp/ip)

Total "IFR_FE_BiRO_TLU" needed for the prototype readout: 1



Outline of the "IFR_FE_BiRO_TLU" module

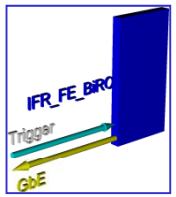
"IFR_FE_BiRO_TLU" module features: (continues)

The FPGA on board the **add-on** card is connected to the RUN CONTROL/DAQ PC of the prototype test setup via an Ethernet port.

The FPGA features a NIOS-II microcontroller which implements the full TCP/IP stack.

The NIOS-II receives commands (i.e. START, STOP, INIT) from the RUN CONTROL/DAQ PC on a TCP server socket and sends data to a TCP server socket on the PC. Data is collected through the LST_FE backplane from the "ABCD" cards upon a trigger request. The data collection section of the FPGA is coded in VHDL.

The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.



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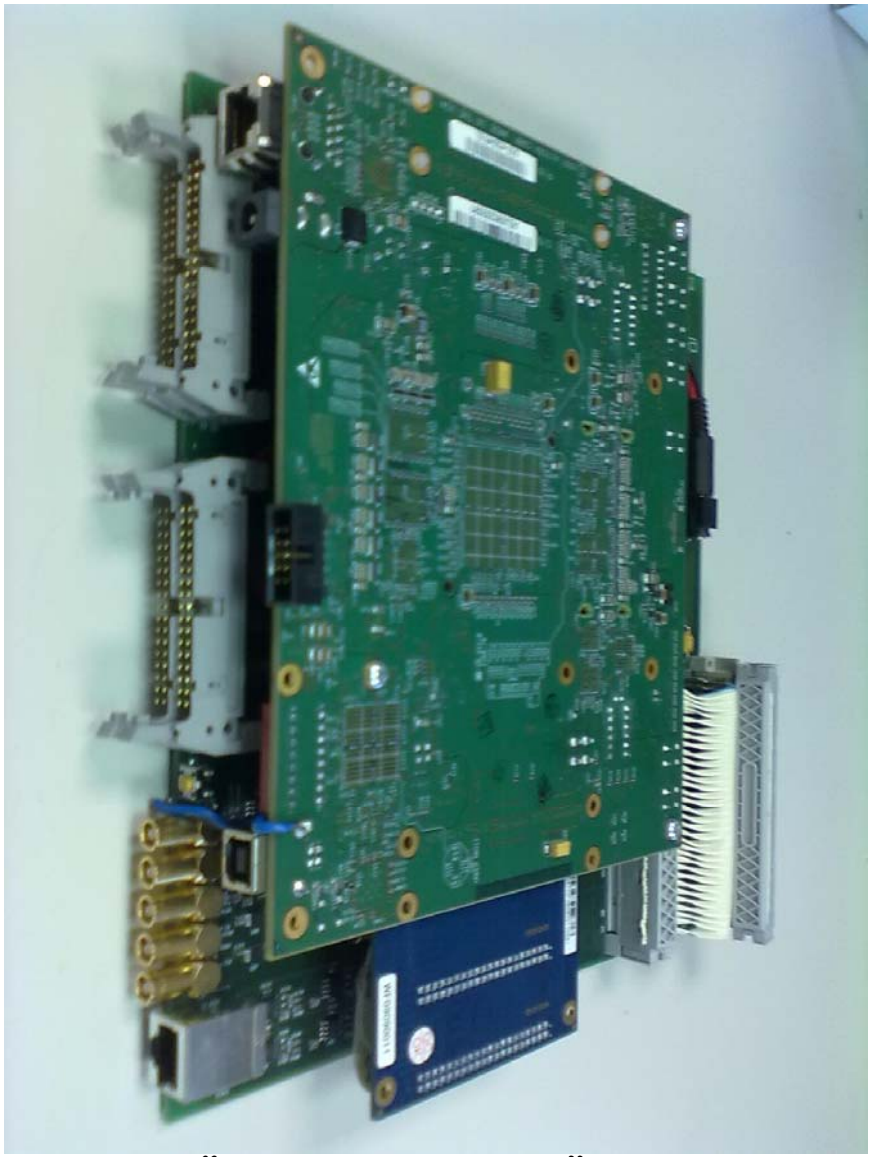


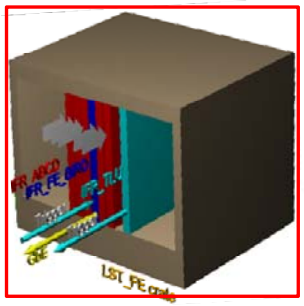
The "IFR_FE_BiRO_TLU" module

"IFR_FE_BiRO_TLU" interface

status update :

- **2 carrier boards have been delivered**
- **2 assemblies have been tested and are being used to test the Binary Mode readout ("BiRO") crates**

One more interface card will have to be stuffed to be kept as a spare



The "IFR_FE_BiRO" CRATE

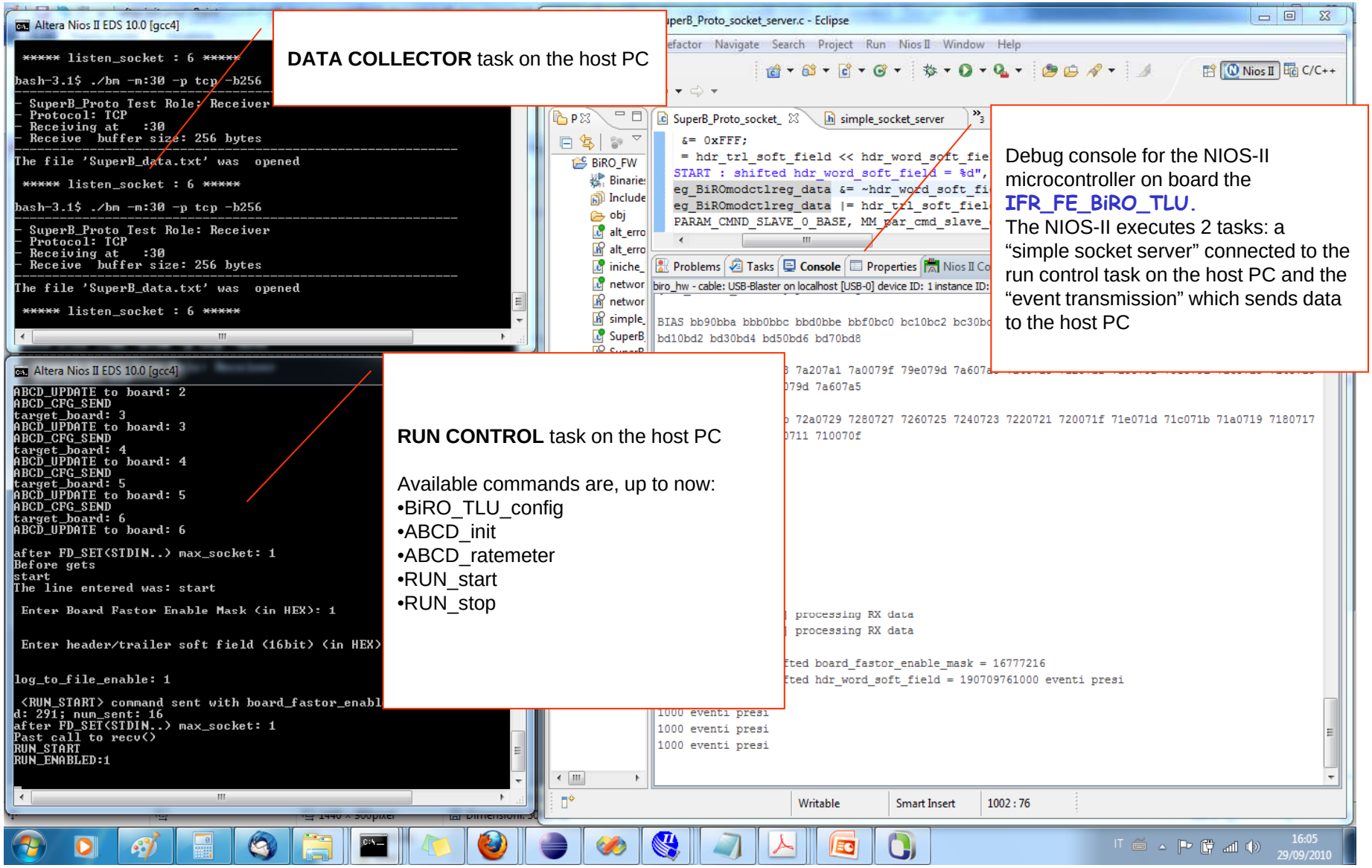
"IFR_FE_BiRO" crate status update:

A notebook PC is presently used to control the
IFR_FE_BiRO_TLU board via Ethernet using
standard TCP/IP socket programming.

The IFR_FE_BiRO_TLU has access to the IFR_ABCD cards to configure them and read them out

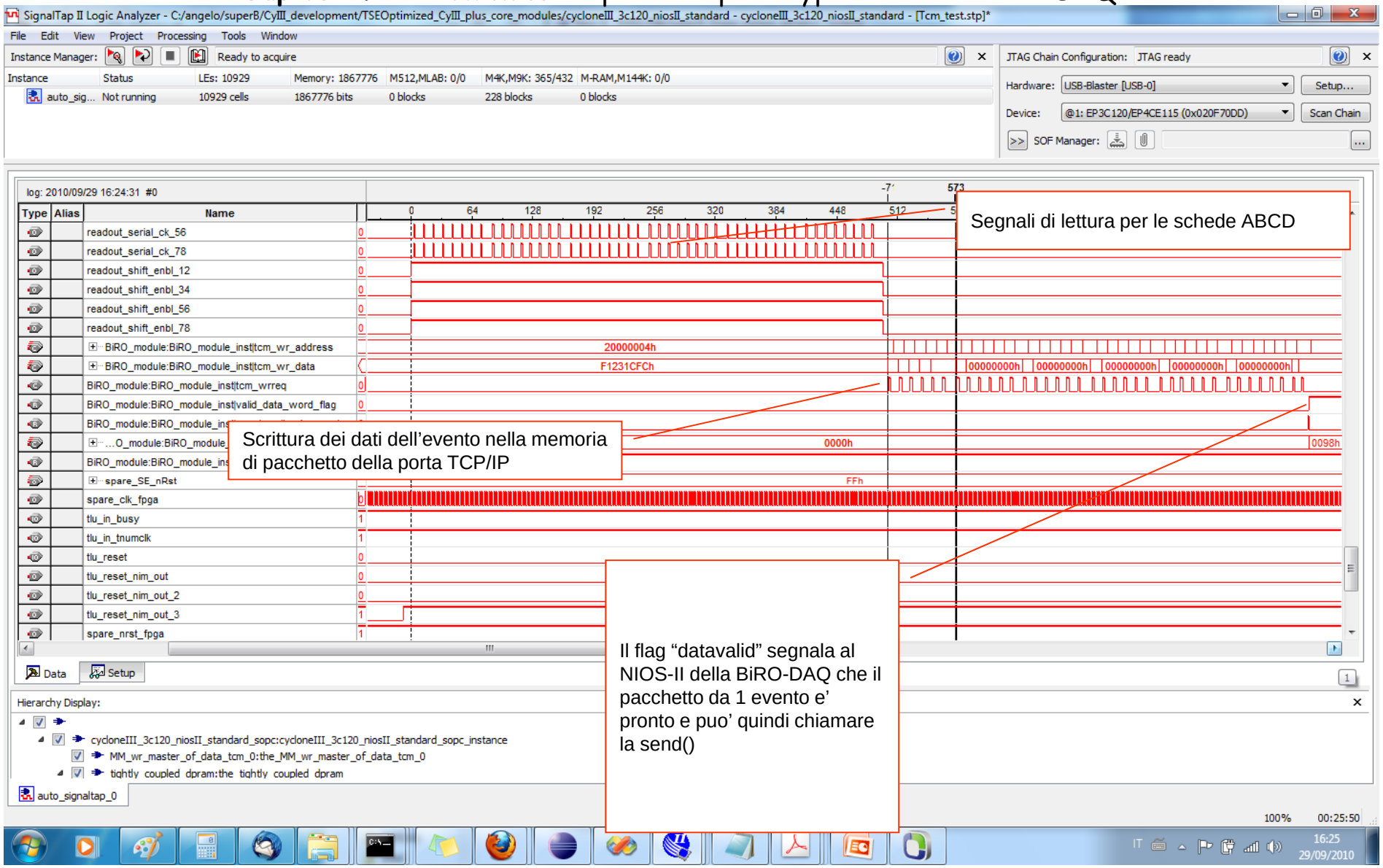
In the current test setup the IFR_ABCD cards are programmed to use their internal test pulse generators.
The "FAST_OR" outputs of the IFR_ABCD cards
are received by the IFR_FE_BiRO_TLU which generates a trigger and reads out the boards through the crate's backplane.

SuperB IFR electronics : update on prototype electronics and DAQ



Internal pulser test results: screenshots from the notebook used to control and collect data from the IFR_FE_BiRO crate

SuperB IFR electronics : update on prototype electronics and DAQ



Internal pulser test results: screenshots from the notebook used to control and collect data from the IFR_FE_BiRO crate

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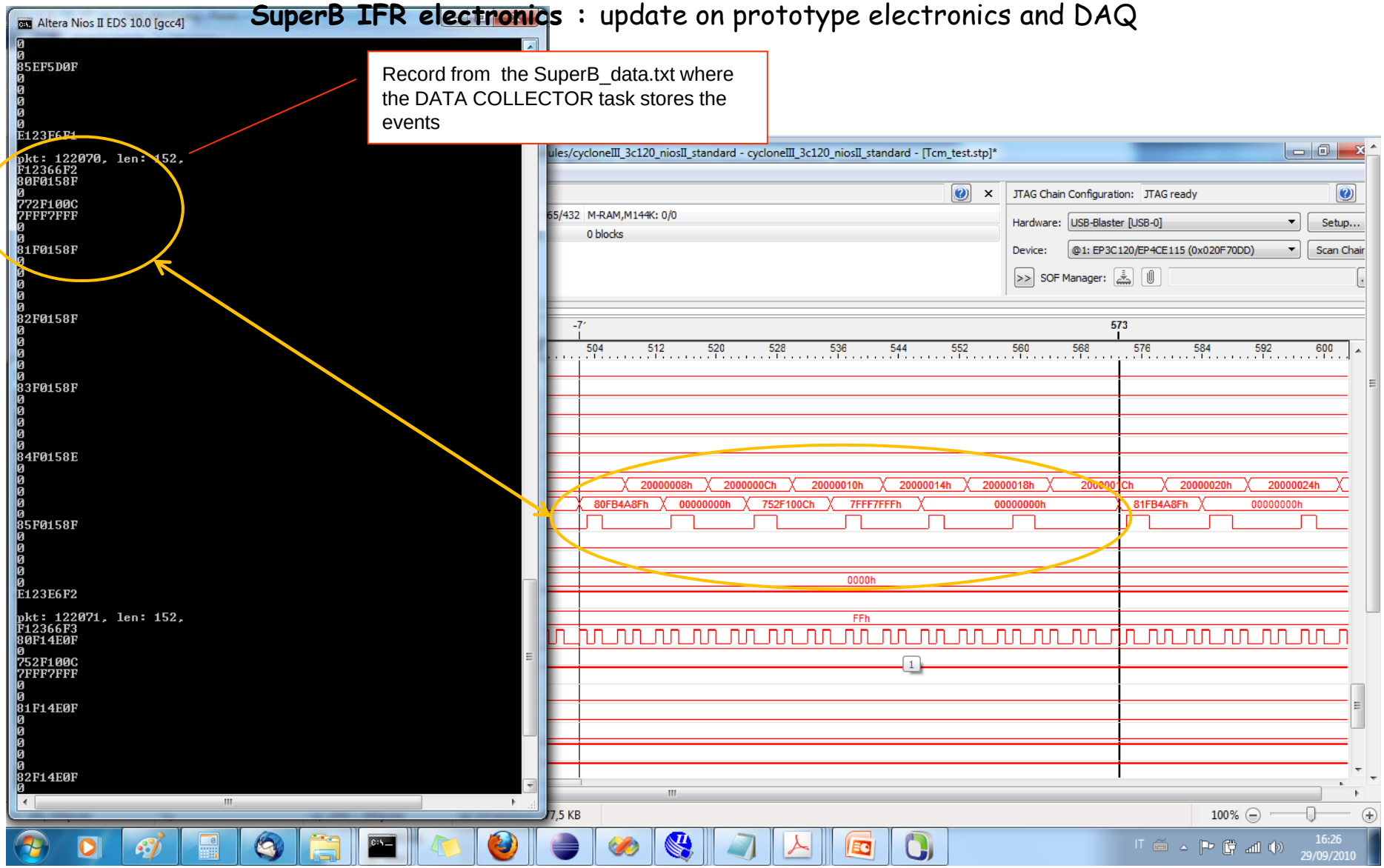
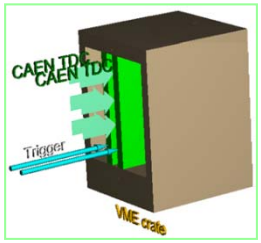
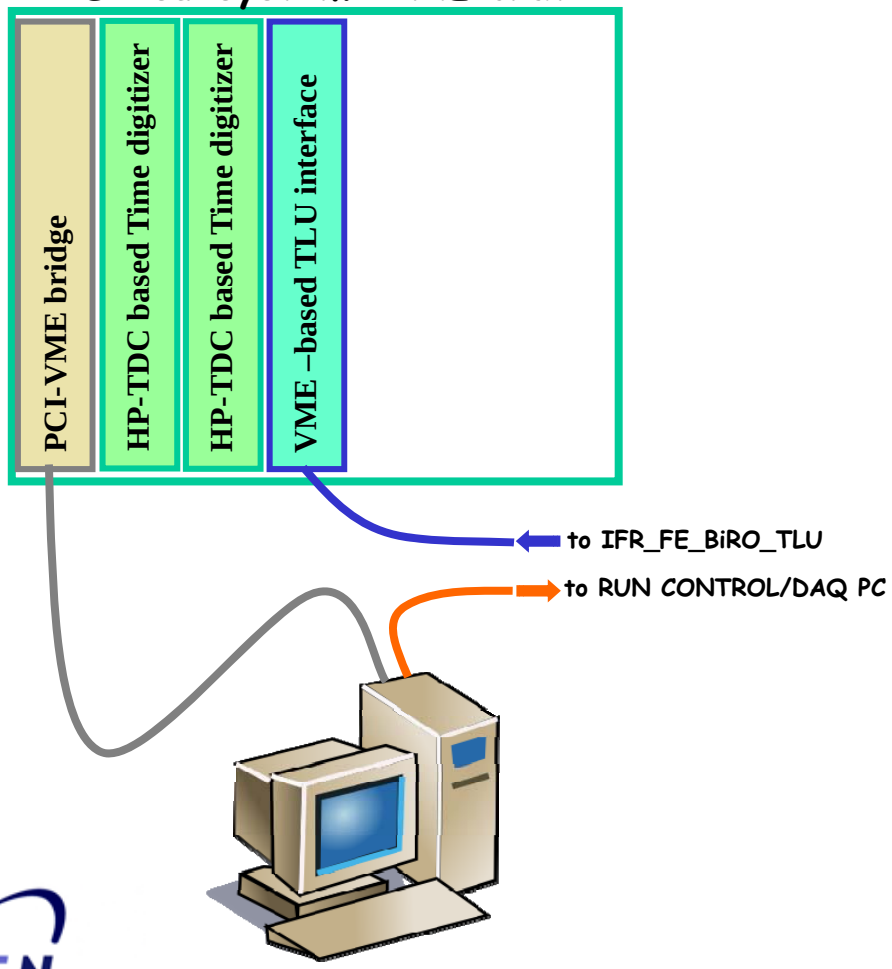


Internal pulser test results: screenshots from the notebook used to control and collect data from the IFR_FE_BiRO crate



"TDC subsystem" VME crate



"TDC subsystem" features:

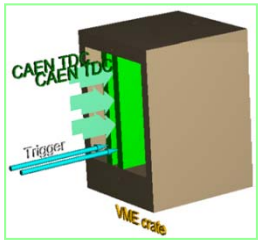
The TDC subsystem uses 2 commercial TDC modules based on CERN's HP-TDC to digitze the time of arrival of the pulses from the "ABCD" boards.

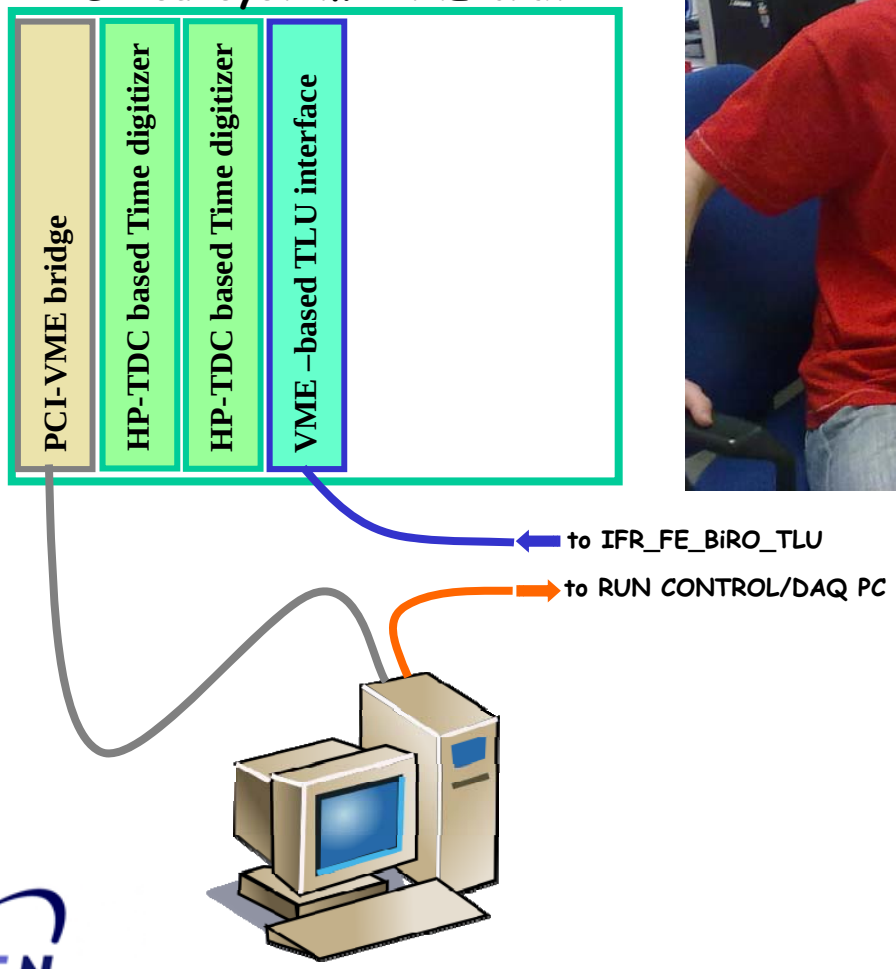
The TDC subsystem will also use a VME-based module to interface to the "IFR_FE_BiRO_TLU" and receive trigger/timing signals

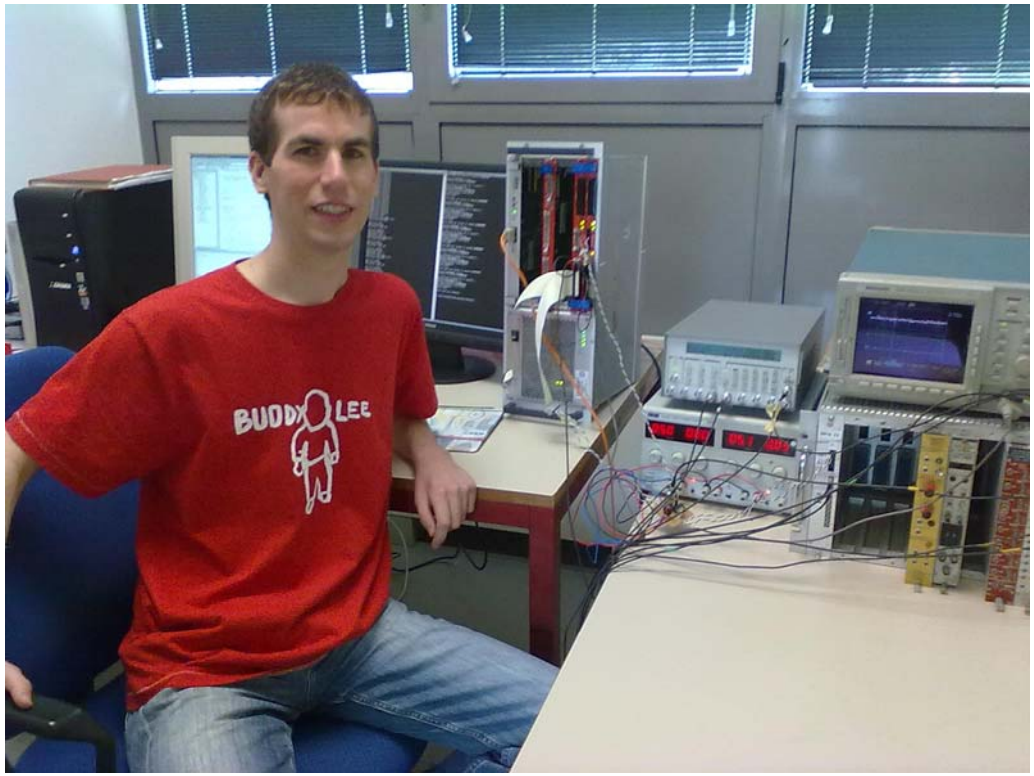
The TDC subsystem VME crate will be controlled and read out by the "TDC-PC" via a PCI-VME bridge.

The TDC_PC will then send the triggered data to the RUN CONTROL/DAQ PC via a TCP/IP connection.

SuperB IFR electronics : update on prototype electronics and DAQ

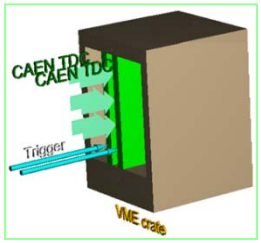






"TDC subsystem" status update :

- TDC readout: DONE
- port toward the Online Detector Control program : DONE,
- acknowledgments to **Stefano Chiozzi**, INFN-Ferrara and **Nicola Dalpasso**, above, undergraduate student at the Ferrara University



Introduction

- The aim is to read events from multiple TDC modules and send them to another computer via TCP / IP.
- A busy logic is introduced to block new events before the previous is read.
- The TDC's readout buffer hold no data or the data of a single event.

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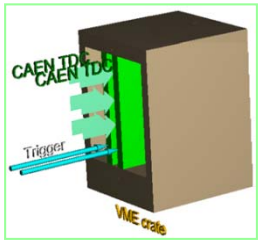
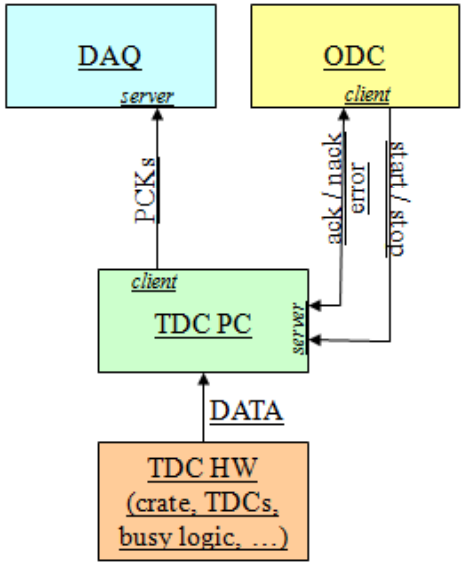


Overview

- The job of the TDC PC is:
  - to respond to start/stop acquisition commands. The ACK and NACK messages confirm the correct execution of the operation. Data acquisition errors are signaled via an error message to the ODC.
  - send acquired data to DAQ
- TCP/IP protocol is used for communication between TDC PC and DAQ / ODC.



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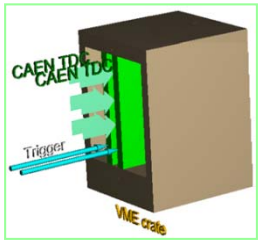
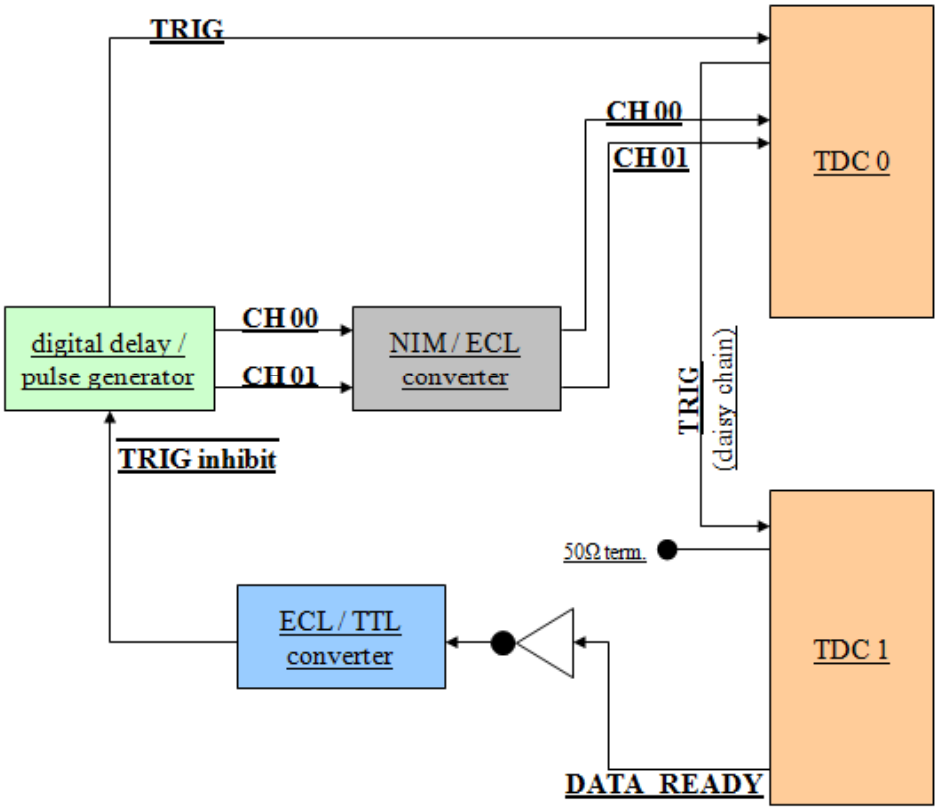
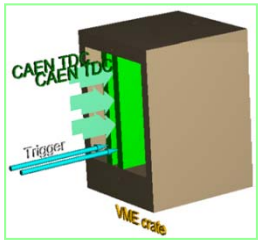


Overview (2)

- We are using only 2 TDCs (with, at the moment, only 2 inputs driven from the timing generator)
- TDCs are operated in trigger matching mode
- TDC's OUT_PROG outputs programmed to indicate the DATA_READY status
- The OUT_PROG output of the last TDC is used to create the busy logic





Read an event

- Steps to read a single event:
  - wait the DATA_READY flag for each TDC module, through polling the Status Register
  - read all the data (enclosed between Global Header and Global Trailer) from the TDCs
- Busy logic: a new event active the OUT_PROG output which is then negated an converted to TTL levels. This signal inihbit the trigger blocking the creation of new events. When all the data are read from the last TDC, the OUT_PROG is deactived and the trigger is enabled.

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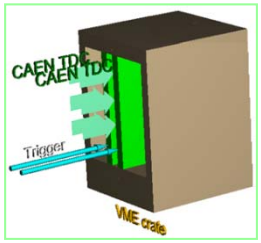

Format of the packets

- Data from a single event are copied in a packet and a header (holding the total size of the packet) and a trailer are added. The packet is then sent to DAQ.

Example of a packet:

0x78600000 : TDC_PC_HEADER : BYTE_COUNT 0096 : TRIGGER_NUMBER 00000
0x4000001f : CAEN_TDC_GLOBAL_HEADER : EVENT_COUNT 00000000 : GEO 31
0x0800076b : TDC_CHIP_HEADER : TDC 0 : EVENT_ID 00000000 : BUNCH_ID 00001899
0x00076d52 : TDC_DATA : EDGE 0 : CHANNEL 0000 : DATA 00486738
0x00176e97 : TDC_DATA : EDGE 0 : CHANNEL 0002 : DATA 00487063
0x18000004 : TDC_CHIP_TRAILER : TDC 0 : EVENT_ID 00000000 : WORD_CNT 00000004
0x0900076b : TDC_CHIP_HEADER : TDC 1 : EVENT_ID 00000000 : BUNCH_ID 00001899
0x19000002 : TDC_CHIP_TRAILER : TDC 1 : EVENT_ID 00000000 : WORD_CNT 00000002
0x0a00076b : TDC_CHIP_HEADER : TDC 2 : EVENT_ID 00000000 : BUNCH_ID 00001899
0x1a000002 : TDC_CHIP_TRAILER : TDC 2 : EVENT_ID 00000000 : WORD_CNT 00000002
0x0b00076b : TDC_CHIP_HEADER : TDC 3 : EVENT_ID 00000000 : BUNCH_ID 00001899
0x1b000002 : TDC_CHIP_TRAILER : TDC 3 : EVENT_ID 00000000 : WORD_CNT 00000002
0x8400019f : CAEN_TDC_GLOBAL_TRAILER : STATUS 4 : WORD_CNT 00000012 : GEO 31
0x4000001f : CAEN_TDC_GLOBAL_HEADER : EVENT_COUNT 00000000 : GEO 31
0x08000115 : TDC_CHIP_HEADER : TDC 0 : EVENT_ID 00000000 : BUNCH_ID 00000277
0x18000002 : TDC_CHIP_TRAILER : TDC 0 : EVENT_ID 00000000 : WORD_CNT 00000002
0x09000115 : TDC_CHIP_HEADER : TDC 1 : EVENT_ID 00000000 : BUNCH_ID 00000277
0x19000002 : TDC_CHIP_TRAILER : TDC 1 : EVENT_ID 00000000 : WORD_CNT 00000002
0x0a000115 : TDC_CHIP_HEADER : TDC 2 : EVENT_ID 00000000 : BUNCH_ID 00000277
0x1a000002 : TDC_CHIP_TRAILER : TDC 2 : EVENT_ID 00000000 : WORD_CNT 00000002
0x0b000115 : TDC_CHIP_HEADER : TDC 3 : EVENT_ID 00000000 : BUNCH_ID 00000277
0x1b000002 : TDC_CHIP_TRAILER : TDC 3 : EVENT_ID 00000000 : WORD_CNT 00000002
0x8400015f : CAEN_TDC_GLOBAL_TRAILER : STATUS 4 : WORD_CNT 00000010 : GEO 31
0xb8000000 : TDC_PC_TRAILER : STATUS_ERROR 0000 : TRIGGER_NUMBER 00000

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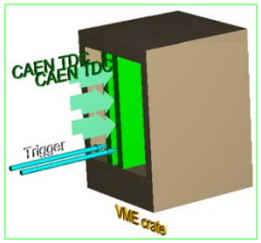

Behavior of the TDC PC

- The behavior of the data acquisition program is illustrated in the FSM bubble diagram. Blue lines mean the operation requested succeeds, otherwise a red line is used.

- For each command received, an ack/nack message is sent.
- Running errors are signaled to the OCL via an error message and the running continue.
- INIT is the initial state: in this state a TDC setup is done and then the program waits for connection from the OCL.