Low Level RF for superB

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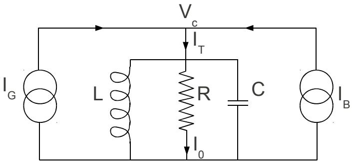
Cavity model

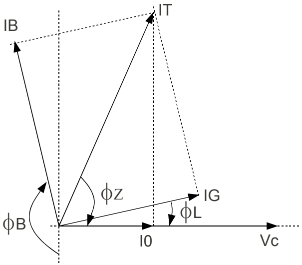


$$Z(s) = \frac{R\frac{\omega_r}{Q_l}s}{s^2 + \frac{\omega_r}{Q_l}s + \omega_r^2}$$

- I_G Generator current
- I_B Beam current
- I_T Cavity current ($\overrightarrow{I_T} = \overrightarrow{I_G} + \overrightarrow{I_B}$)
- I_0 Loss current in shunt resistance
- V_C Cavity voltage
- Q_l Loaded quality factor

- High intensity beam → cavity voltage perturbated by I_B
- Objective: maintain constant V_C
  - I_G contribution should compensate I_B
  - Modulation of I_B → modulation I_G

Cavity tuning / phasor diagram



- ϕ_{L} Loading angle
- ϕ_{Z} Cavity tuning angle
- ϕ_{B} Stable phase angle (above transition I_B points upward)

- From diagram study: $\tan\phi_Z = \tan\phi_0 + \frac{I_B}{I_0}(\tan\phi_0 \sin\phi_B + \cos\phi_B)$
- Maintaining generator current in phase with cavity voltage $\rightarrow$ $\tan\phi_Z = \frac{I_B}{I_0}\cos\phi_B$
- Cavity tuning angle increase with current
- Frequency shift due to cavity tuning $\delta f = -f_{RF}\frac{Z_{sh}}{Q}\frac{I}{V_{RF}}N_c$
  - In LER: 233 kHz
  - In HER: 252 kHz
- Values close to $\omega_{rev} - \omega_s$ (227 kHz- 2.65 kHz)

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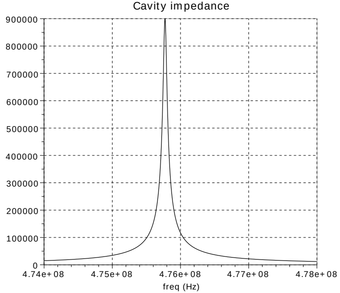
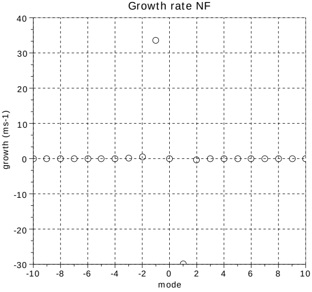
Instabilities and cavity impedance

- Instabilities growth rates proportionnal to the cavities impedance:

$$\tau_l^{-1} \approx \frac{e I_B F_{rf} \alpha}{2 E Q_s} \left[Re\ Z_c(\omega_{rf} + l\omega_{rev} + \omega_s) - Re\ Z_c(\omega_{rf} - l\omega_{rev} - \omega_s) \right]$$

- Applying this to the detunned cavity impedance yields:





- mode -1 growth rate is 33 ms^{-1} (baseline LER)
  - Comparable to synchrotron frequency $(1/\tau_{-1})/\omega_s \sim 0.5$
  - Exceed the radiation damping rate (LER damping time $=$20.3 ms) $(1/\tau_{-1})/(1/\tau_d) \sim 670$

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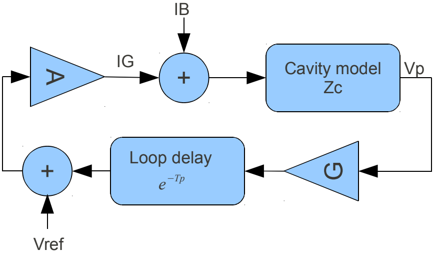
Direct RF feedback (1/2)



Expected impedance reduction

$$Z_{fbk}(\omega) = \frac{Z(\omega)}{1 + GAe^{-jT\Delta\omega} Z(\omega)}$$

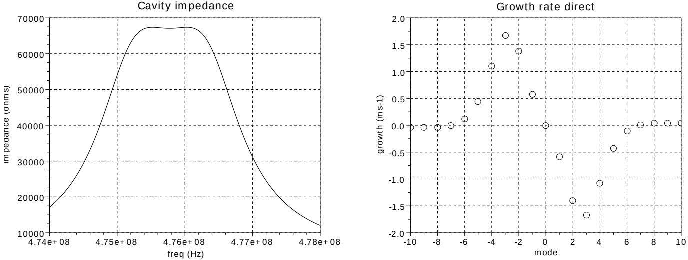
- In theory the highest gain GA is desired:
  - Maintain loop stability → Phase Margin is impacted by loop delay
  - Canonical value of PM $= \pi/4$ yields

$$GAR \leq \frac{Q}{\omega_r} \frac{\frac{\pi}{4T} + 2\omega_r}{1 + \omega_r \frac{4T}{\pi}} = G_{max}AR$$

  - Impedance reduction limited by the loop delay T

Direct RF feedback (2/2)

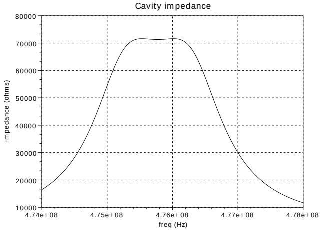
- Plots with loop gain $= 1.3 \times G_{max}AR$ (flat response) and T=440 ns (PEP2 delay value)

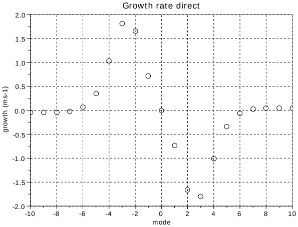


- Maximum impedance decreased by a factor of 12.8
- -1 Mode is damped by a factor of 20
- Side effect: other modes growth rates are increased!
- More impedance reduction is needed

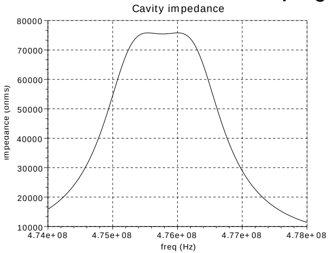
Delay influence

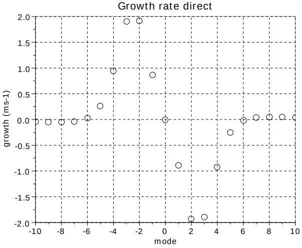
T=470 ns





T=500 ns





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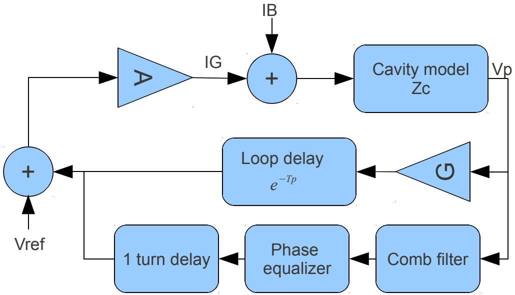
Comb filter feedback principle



- Overcome loop delay limitation
- Correction applied with one turn delay
- Minimize impedance at certain frequencies

- Attenuation needed at synchrotron sidebands → dual peaked comb filter $H_{comb}(jw) = \dfrac{G(1 - e^{-jwT_{rev}})}{1 - 2K\cos(2\pi\nu_s)e^{-jwT_{rev}} + K^2 e^{-j2wT_{rev}}}$
- Response is modified by the complement to reach one turn delay $H(jw) = H_{comb}(jw) \times e^{-jw(T_{rev} - T_g)}$
- Out of klystron bandwidth, large dephasing → loop instability
- Precompensation of the dephasing → phase equalizer

Comb filter feedback limitations

- Gain margin of 10 dB for loop stability (when $\phi = \pi$)
  $$G_{max} \leq \frac{1 + 2K\cos(2\pi\nu_s) + K^2}{6}$$
- The closest K come to the unity, higher the gain, and narrower the bandwidth
- Max gain on comb loop is function of K
  - with K=63/64 G=0.655
  - with K=127/128 G=0.660
- PEP2 practical value was 0.2? Something to understand here
- Reminder: longitudinal radiation damping rate: 0.0492 ms^{-1}

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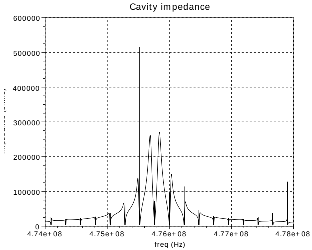
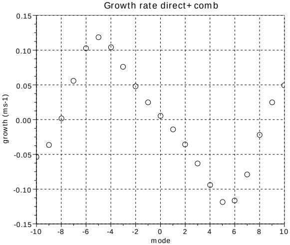
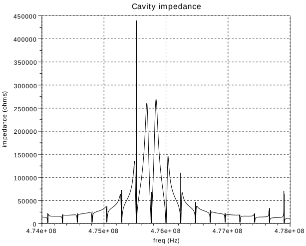
Simulations

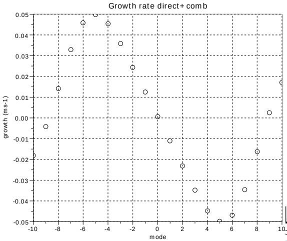
K=63/64





K=127/128
33 ms^{-1} $\rightarrow$
0.05 ms^{-1}





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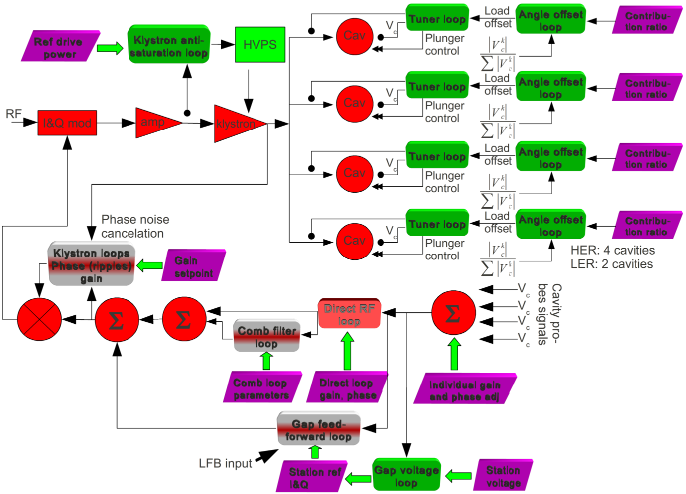
LLRF feedback overview



delay sensitive

setpoints

Slow processing

fast processing

- Tuner loop details
- GFF details
- Gap voltage loop
- Klystron loop details
- Hardware platform

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Cavity tuning

Tuner loop

- Minimizing of the phasing between cavity probe signal and cavity forward voltage
- Setpoint: load offset angle

Angle offset loop

PEP2 implementation arguments. Since all cavities have the same voltage applied, it may be necessary to:

- decrease the gap voltage by having non zero angle. Lowers voltage on fragile cavity
- compensate eventual misphasing between beam and generator current (relative beam phase due to geometry, waveguide length, ...)

Back to loops overview

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Gap feedforward (1/2)

Problem

- Gap in the ring, is like an amplitude modulation of the beam current
- Current generator with feedback loop is there to compensate beam current effect on the cavity
- Empty bunch $\rightarrow$ cavity voltage is not degraded by beam current, power not extracted by beam, unnecessary power used
- Need a way to avoid unnecessary modulation of the klystron

Back to loops overview

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Gap feedforward (2/2)

Solution

1. Detect periodic gap transients by sampling cavity sum signal over one turn
2. Adaptative filtering is done by combining previous sampling and station I&Q reference in order to minimize the gap transient effect
3. Correction is applied one turn later

Longitudinal feedback input

1. In order to provide more power for kicking lower order mode
2. Cosine and sine of LFB kick is applied to Q & I outputs of the model respectively

Back to loops overview

Gap voltage loop

Gap voltage has to be maintained constant

- Direct RF loop works well to damp transient but the loop gain is small
- Workaround: use a slow loop that will modify setpoints (station I&Q reference)
- Minimize error at fundamental frequency between gap voltage and forward voltage with higher gain

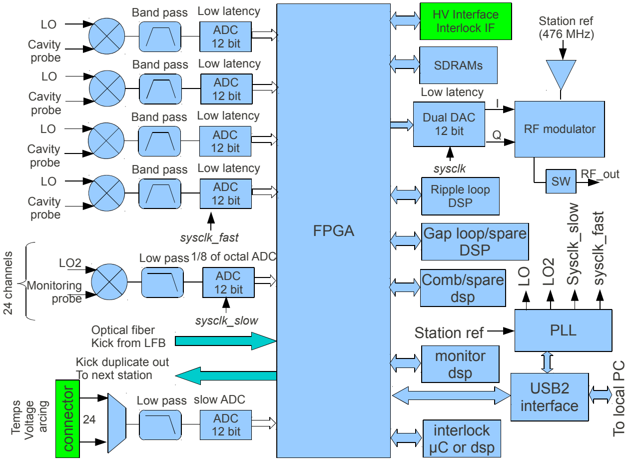
Back to loops overview

Klystron loops

- Anti saturation loop
  - tend to maintain a constant drive power by changing HVPS
  - $\rightarrow$ Keep Klystron out of saturation
- Klystron gain loop
  - Direct RF and comb loop must see a constant klystron gain
  - But previous loop plays with HVPS in order to keep constant drive power
  - This loop hides gain changes due to HVPS changes
- Klystron ripple (or phase) loop
  - Changes in HVPS induces phase shift in the klystron
  - Slow changes due to anti saturation loop could be hidden by a slow loop
  - However HVPS usually display ripples $\rightarrow$ fast computation needed

Back to loops overview
Hardware platform

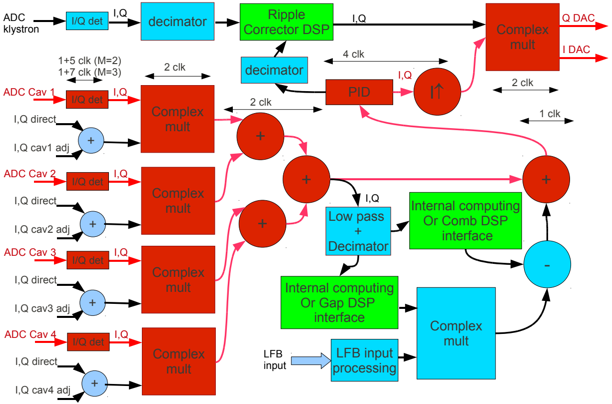
All digital solution



- Digital Down Conversion
- Group delay is critical
- Data in one board
- Computing power
- Memories for fault recording and excitation

- Monitoring DSP, build fast amplitude and phase monitoring signals
- Interlock interfaces (arcing???)

FPGA content - focus on latency critical path



Serv Group delay sensitive
One turn delay for computation
Eventual DSP interfaces

- The sharper the CIC filter, the larger the group delay
- PID used as lead compensator, negative group delay!
- PEP2 RFP module had 86 ns of I/O delay, BW=3 MHz (Teytelman)
- Total duration 17/19 + 12 due to ADC/DAC is 29/31 clock cycles
- Worst case: at 250 MHz $\rightarrow 31 \times 4\ ns = 124\ ns$!

back to delay influence

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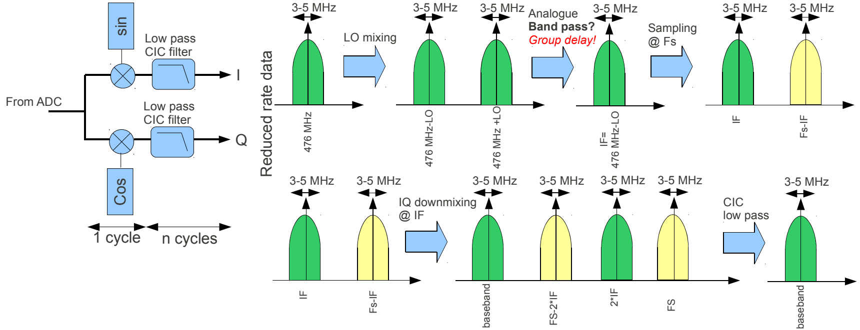
Digital Down Conversion (DDC) (1/2)

Principle



- Bring bandwidth of interest to baseband by multiplying a signal at Intermediate Frequency by a sine and cos at the same IF frequency
- Benefits:
  - No dissymmetry in I&Q pathes (path length, encoding, ...)
  - No susceptibility to DC offsets
- Focus on latency critical path

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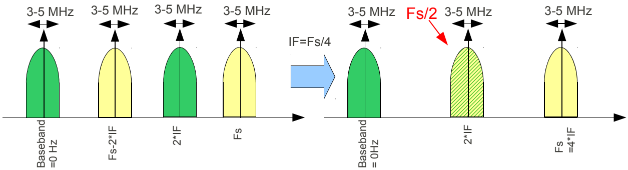
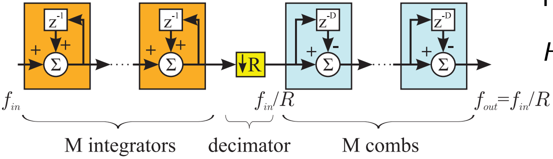
Digital Down Conversion (2/2)

Simplification possible by using $\mathrm{Fs} = 4 \times \mathrm{IF}$ in the limited latency path.



- Easier to implement, doesn't need real multipliers and sine/cos table (values 0,1,-1,0)
- Input should be clean or steeply bandpass filtered → at the cost of group delay!!
- Mixer quality (IF harmonics!) → existing chips have attenuation of first harmonics <-65 dB

CIC design

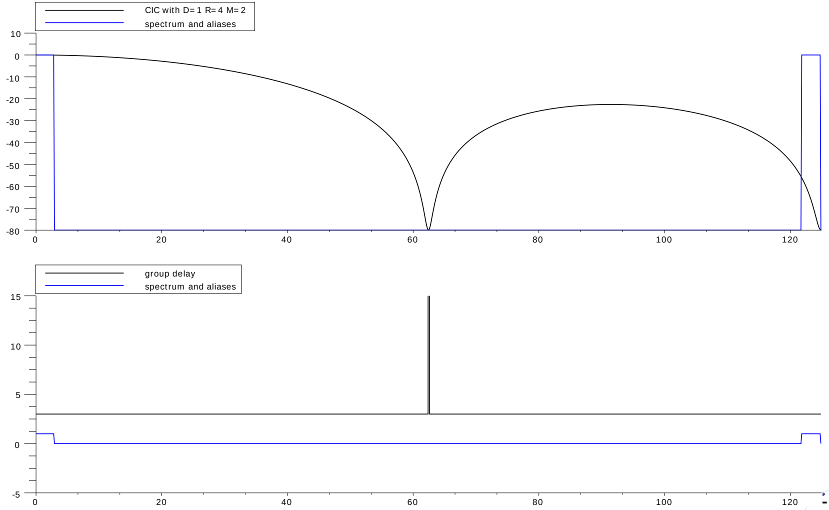


Filter equation :

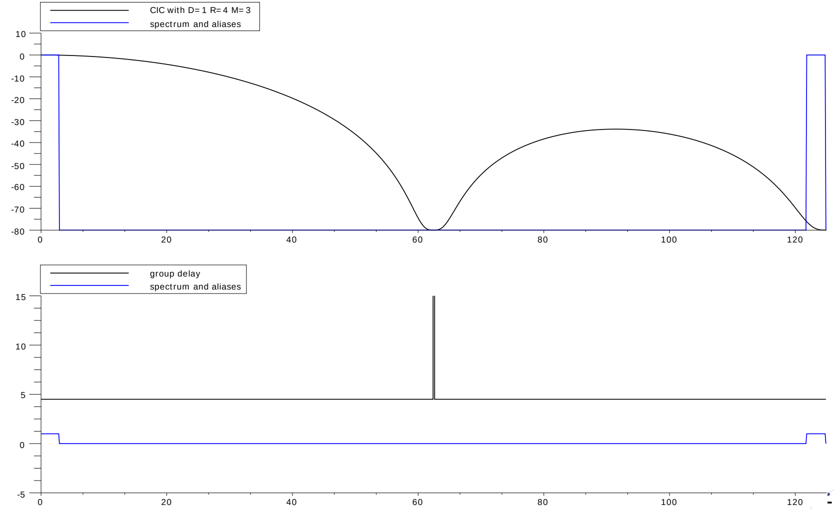
$$H(z) = \left(\frac{1 - z^{-RD}}{1 - z^{-1}} \right)^M$$

- Very simple to implement in FPGA
- Only additions/substractions
- Following slides will present two sets of parameters (D=1,R=4, M=2 or M=3).
- Interesting to note filter selectivity vs group delay.

CIC design


CIC with D= 1 R= 4 M= 2
spectrum and aliases
10
0
-10
-20
-30
-40
-50
-60
-70
-80
0
20
40
60
80
100
120
group delay
spectrum and aliases
15
10
5
0
-5

CIC design


CIC with D= 1 R= 4 M= 3
spectrum and aliases
10
0
-10
-20
-30
-40
-50
-60
-70
-80
0
20
40
60
80
100
120
group delay
spectrum and aliases
15
10
5
0
-5

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Conclusion

- By simulation, the highest growth rate should be 0.05 ms^{-1}, in real life should be a little bit higher
- All feedbacks can be implemented in a digital fashion (FPGA or software for slow loop) $\rightarrow$ Flexibility and maintenability
- Determine necessary signal range for an optimal feedback (filtering vs group delay)
- Any comments or questions?

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Open questions

- How to test an electronic prototype?
  - Possible to build a test setup with klystron, RF source, cavity, ???
  - Have access to a similar installation?
- Samples of very technical questions:
  - Tuner, HVPS, interlock interfaces?
  - Amplifier drive level? Need output attenuator (fix or programmable?)
  - Klystron recommended drive power
  - Klystron model for lead compensator
  - Arc interlock module ?
  - ...
- Interlocutors are needed

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