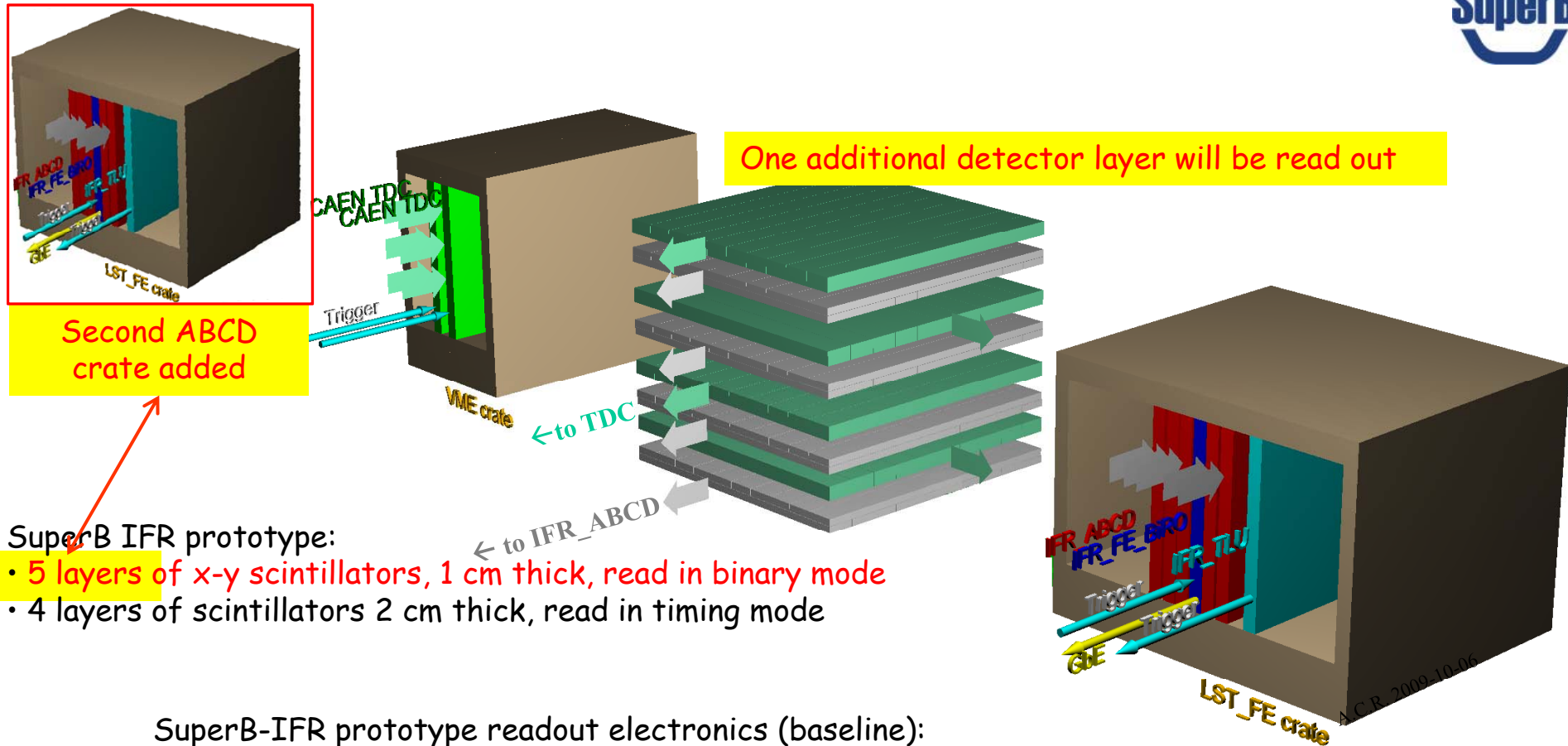


SuperB IFR electronics: update on prototype electronics and IFR_DAQ

Overview

- update on the development of the IFR prototype electronics and DAQ system



SuperB IFR prototype:

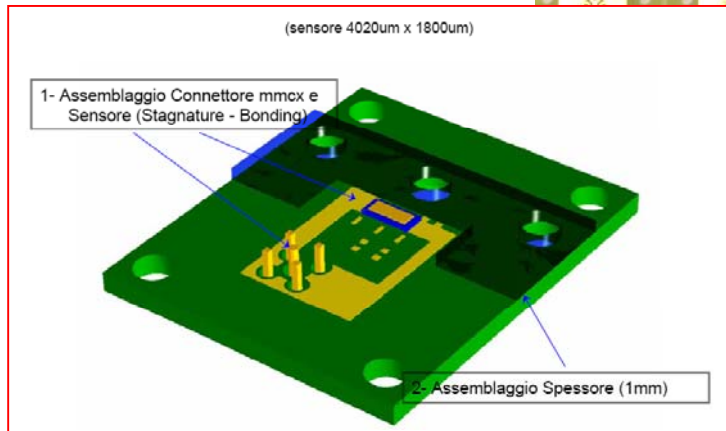
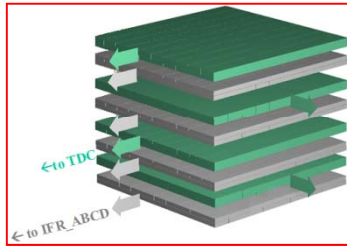
- 5 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

SuperB-IFR prototype readout electronics (baseline):

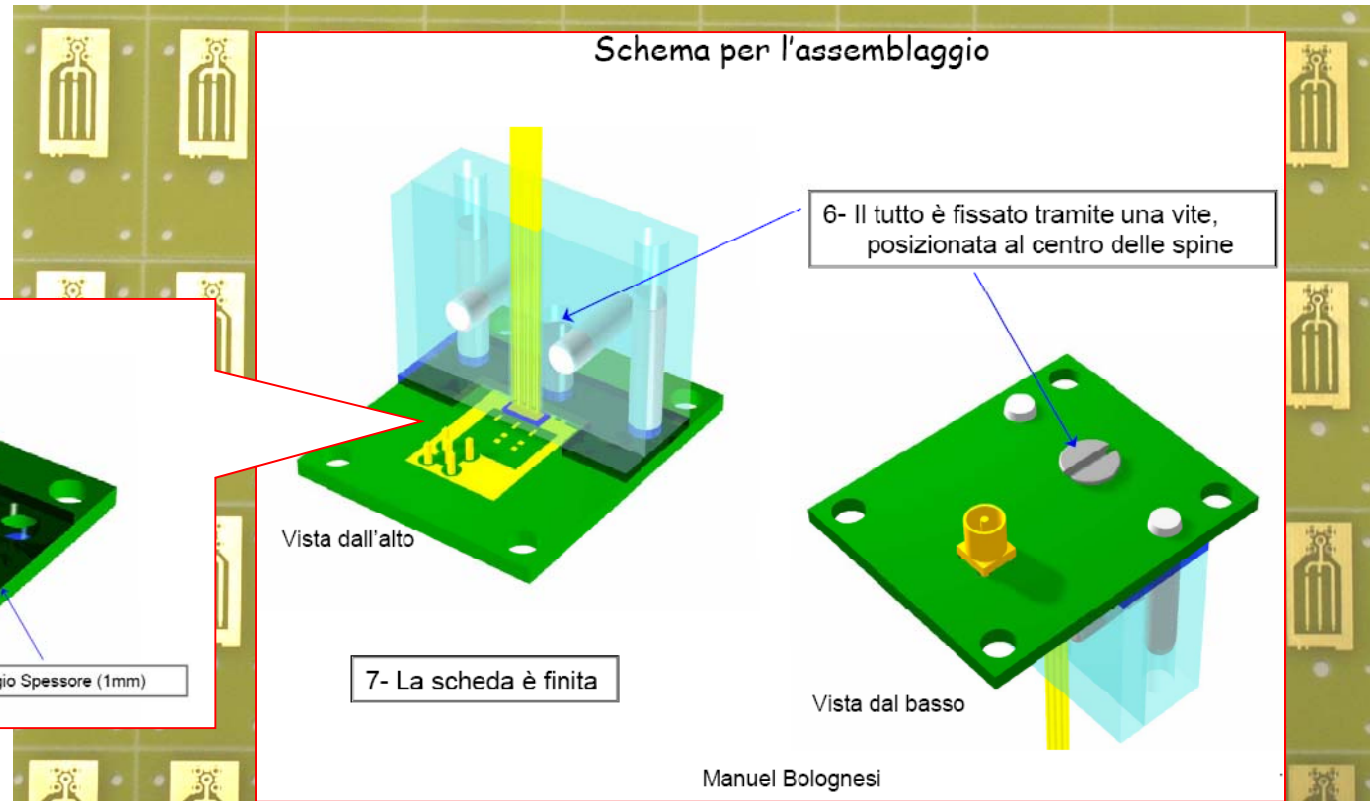
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing: it samples the level of the comparators outputs @ $\geq 80\text{MHz}$ and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

IFR_FE_BiRO + IFR_TLU are now a single module

SuperB IFR electronics : update on prototype electronics and DAQ SiPM carrier PCB



SiPM carrier PCB with NiAu plating for bonding: fits all three type of sensors being manufactured by FBK-Trento. Sensor die gluing position is determined by a removable countermask.



Status:

- all parts needed have been delivered
- **SiPM bonding is ongoing at INFN-Perugia thanks to Dr. Giovanni Ambrosi and Dr. Maria Ionica**
- **bonded SiPM already delivered to INFN-Ferrara are being characterized**

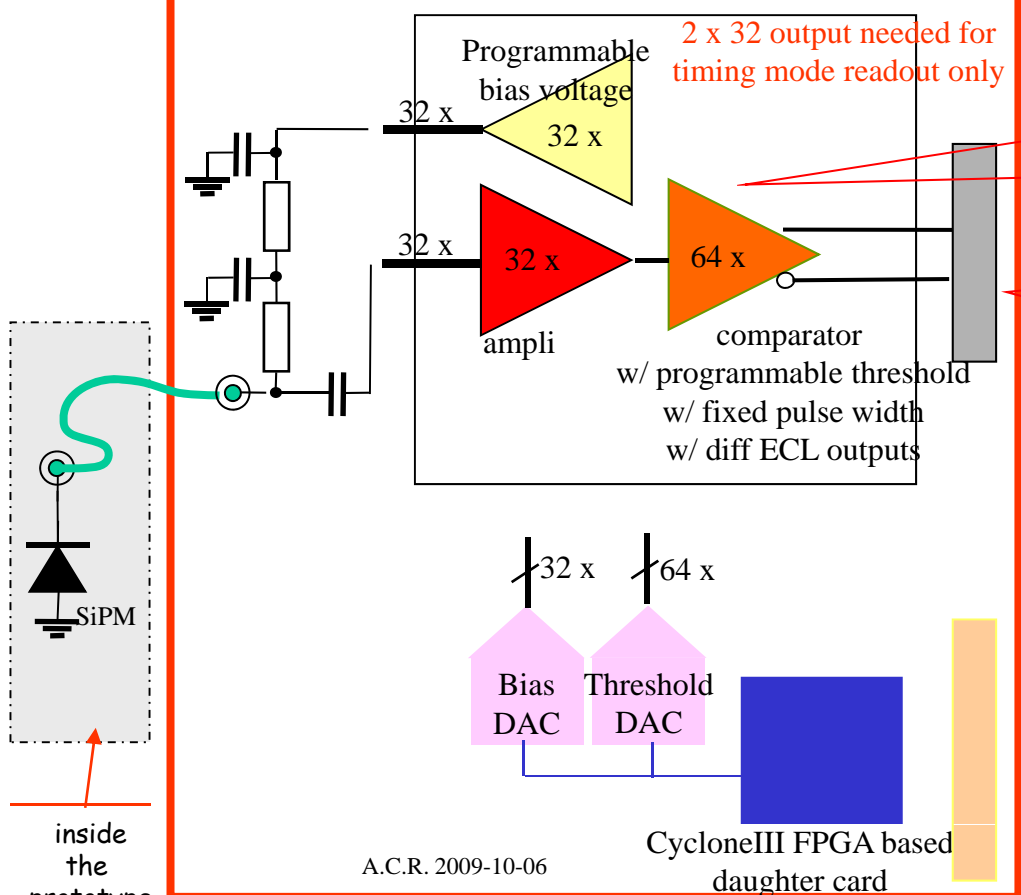
SuperB IFR electronics : update on prototype electronics and DAQ



dimensions: VME 6U x 220mm

"IFR_ABCD" card features:

- ampli: two stage w/discrete components: BGA2748 + BGA2716
- discri: ADCMP563BRQ (ECL out, dual)



For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

- DAC: LTC2625CGN#PBF (I²C, 12bit, octal)
- FPGA: Cyclone III ALTERA EP3C25Q240C8

"IFR_ABCD" needed for prototype readout :
 1 for each of 4 BiRO planes (readout at only one end of scintillator) +
 1 for each of 4 planes read with TDCs (readout at both ends of scintillator)

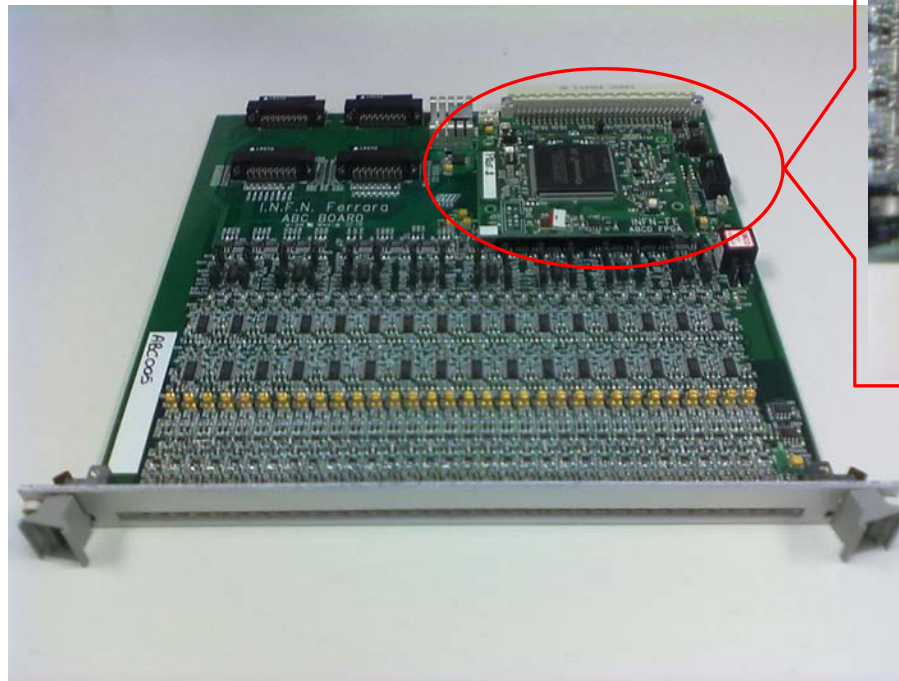
TOTAL "IFR_ABCD" cards: 8

TOTAL "IFR_ABCD" cards produced: 12
To enable the reading of a 9th prototype layer

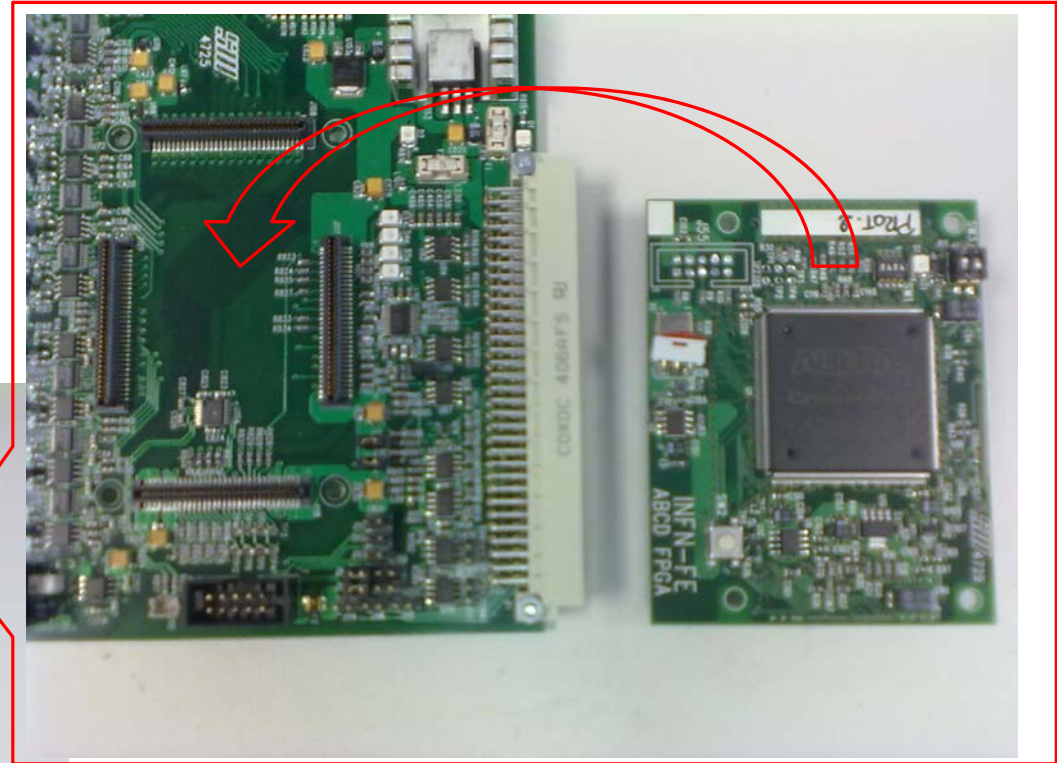
Outline of the "IFR_ABCD" card
 (Amplifier, Bias, Comparator, DataProcessing)

IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by R. Malaguti, INFN-Ferrara

SuperB IFR electronics : update on prototype electronics and DAQ



"IFR_ABCD" card

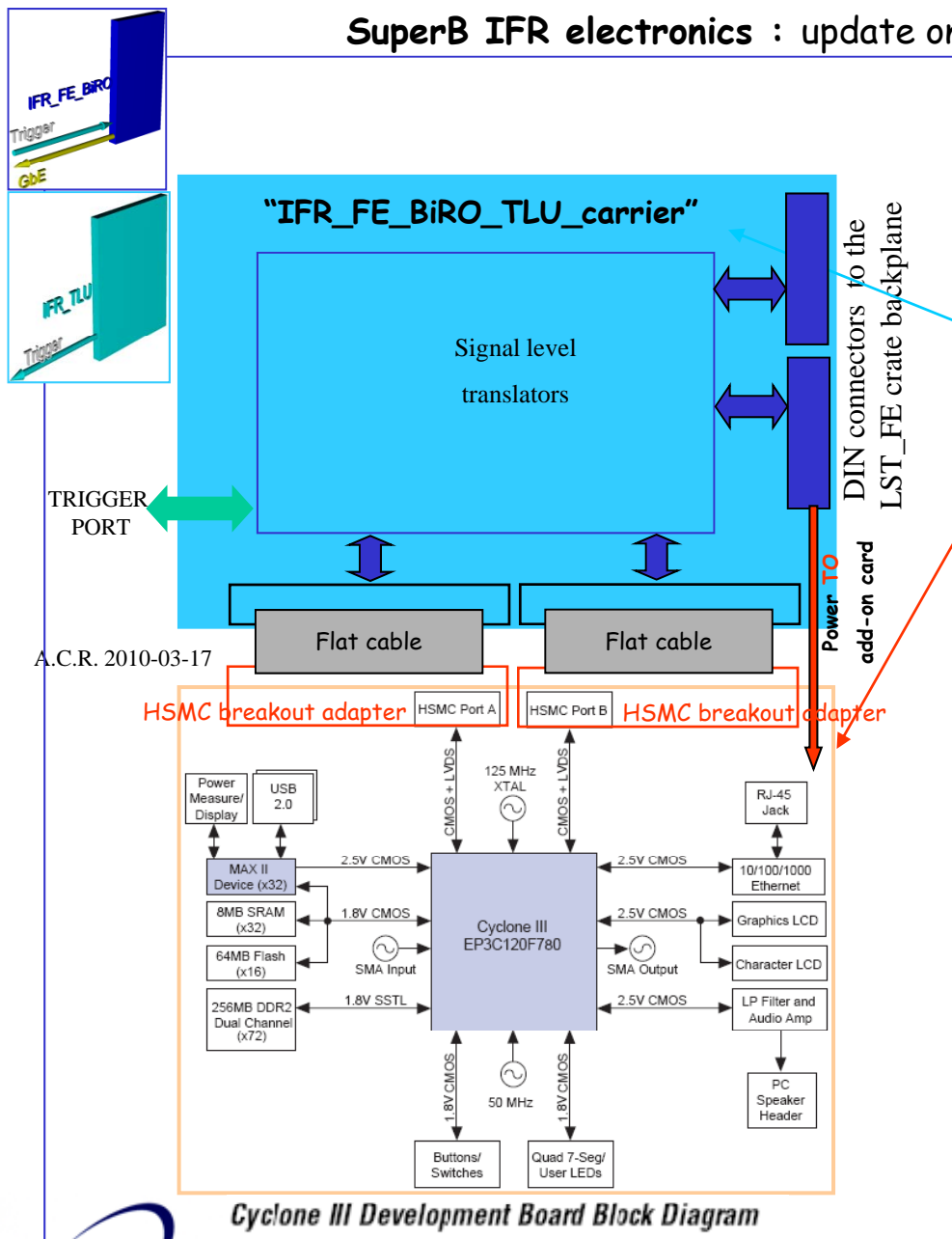


Detail of the digital "IFR_ABCD" daughter card

"IFR_ABCD" status update :

- 8 boards delivered and tested
- 4 boards expected

SuperB IFR electronics : update on prototype electronics and DAQ



"IFR_FE_BiRO_TLU" module features (new):

The functions of the IFR_FE_BiRO and of the IFR_FE_TLU cards are combined into a single system made of

- a **carrier card** which fits in the "LST_FE" crate (6U x 220mm depth)
- an **add-on card** : it's simply the ALTERA Cyclone III development kit (DK-DEV-3C120N) equipped with breakout adapters for the kit's HSMC connectors

The **carrier card** hosts level adaptors and application specific I/O ports which allow the **add-on card** to:

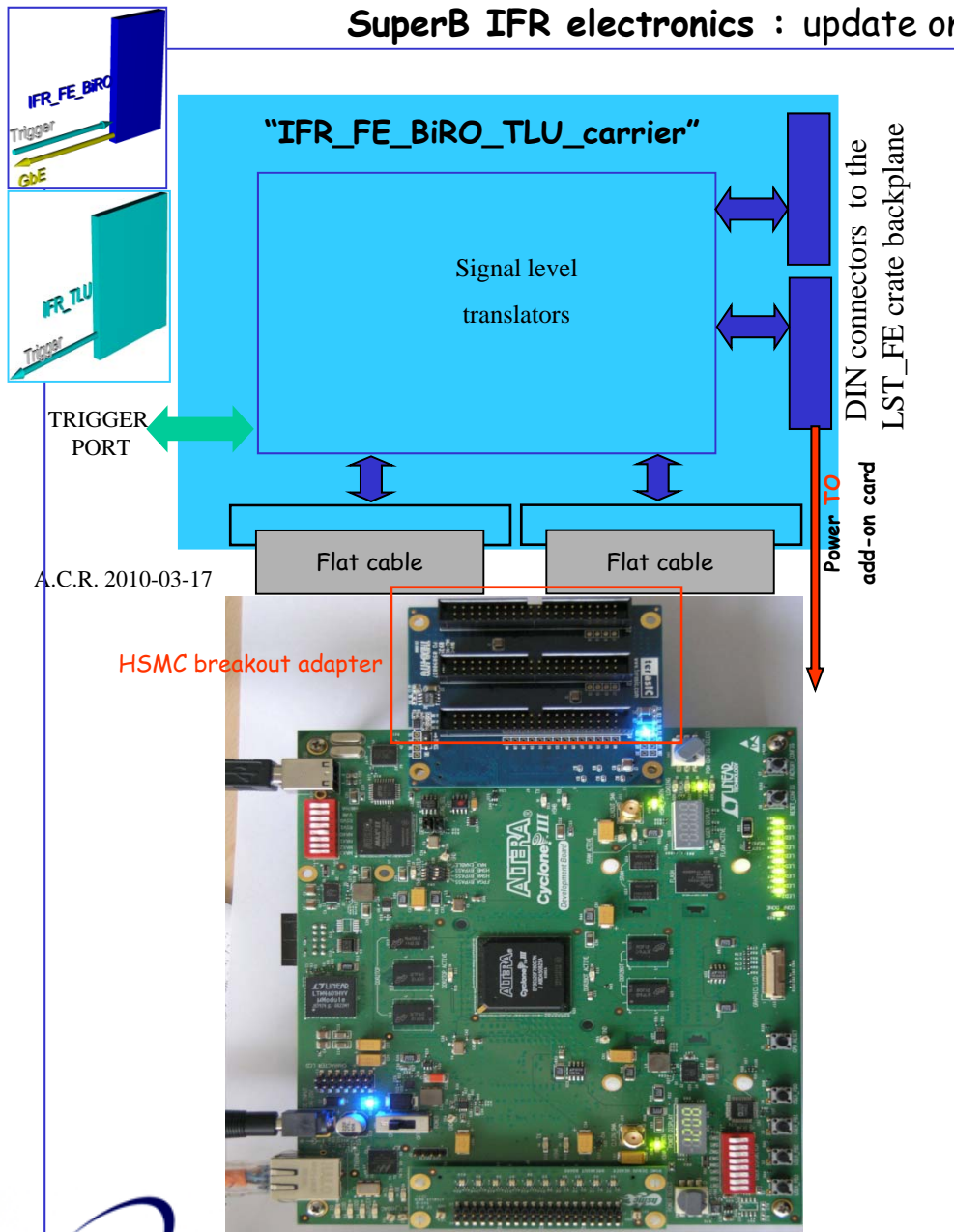
- receive power
- receive the "fast OR" signals from the "ABCD" cards to generate triggers from
- generate and distribute triggers (also to the TDC system)
- generate and distribute clock and reset signals (also to the TDC system)
- poll data from the "ABCD" cards
- configure the programmable resources on the "ABCD" cards
- connect to the host PC running the DAQ software via ethernet (tcp/ip)

Total "IFR_FE_BiRO_TLU" needed for the prototype readout: **1**

Cyclone III Development Board Block Diagram

Outline of the "IFR_FE_BiRO_TLU" module

SuperB IFR electronics : update on prototype electronics and DAQ



"IFR_FE_BiRO_TLU" module features: (continues)

The FPGA on board the **add-on** card is connected to the RUN CONTROL/DAQ PC of the prototype test setup via an Ethernet port.

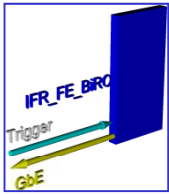
The FPGA features a NIOS-II microcontroller which implements the full TCP/IP stack.

The NIOS-II receives commands (i.e. START, STOP, INIT) from the RUN CONTROL/DAQ PC on a TCP server socket and sends data to a TCP server socket on the PC. Data is collected through the LST_FE backplane from the "ABCD" cards upon a trigger request. The data collection section of the FPGA is coded in VHDL.

The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.

The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.

SuperB IFR electronics : update on prototype electronics and DAQ



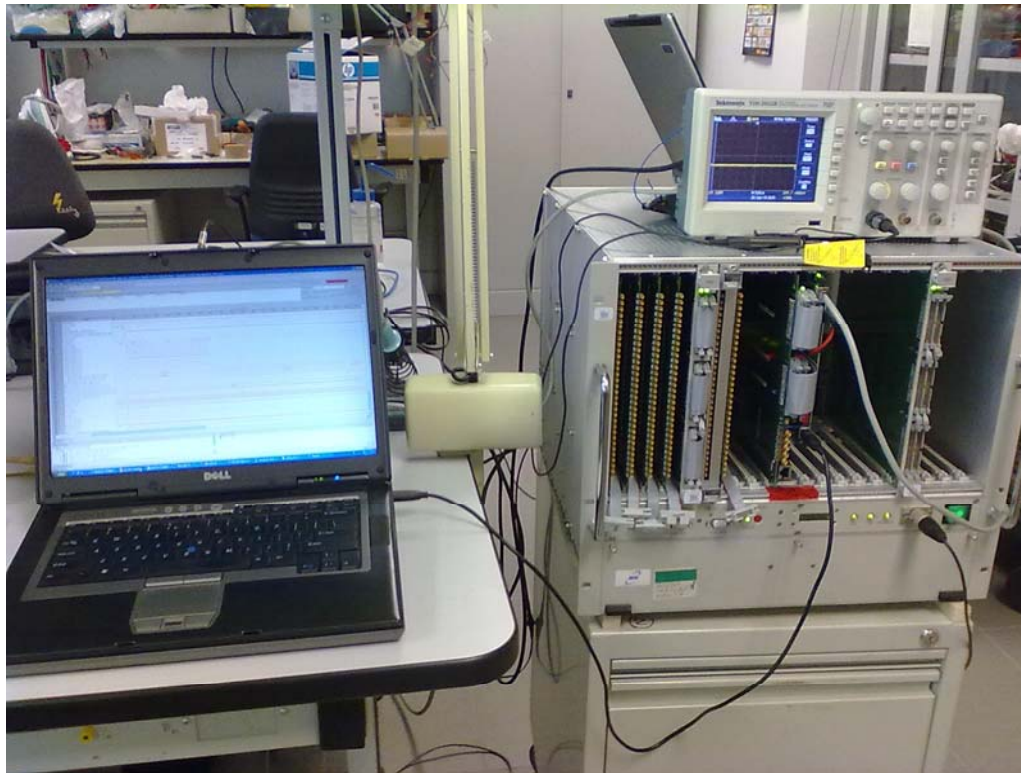
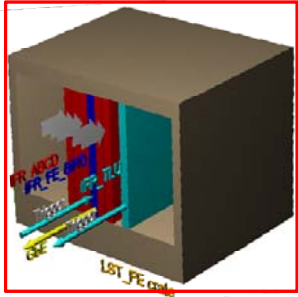
"IFR_FE_BiRO_TLU" interface

status update :

- 2 carrier boards have been delivered
- 2 assemblies have been tested and are being used to test the Binary Mode readout ("BiRO") crate

The "IFR_FE_BiRO_TLU" module

SuperB IFR electronics : update on prototype electronics and DAQ



"IFR_FE_BiRO" crate status update:

A notebook PC is presently used to control the **IFR_FE_BiRO_TLU** board via Ethernet using standard TCP/IP socket programming.

The **IFR_FE_BiRO_TLU** has access to the **IFR_ABCD** cards to configure them and read them out

Presently the **IFR_ABCD** cards are programmed to use their internal test pulse generators. The "FAST_OR" outputs of the **IFR_ABCD** cards are received by the **IFR_FE_BiRO_TLU** which generates a trigger and reads out the boards through the crate's backplane.

The "IFR_FE_BiRO" CRATE

DATA COLLECTOR task on the host PC

```

**** listen_socket : 6 ****
In:
C:\qdrives\angel..._CylII_development\SuperB_PC_side\benchmark_source
[NiosII EDS] $ ./bm -m:30 -p tcp -b256
- SuperB_Proto Test Role: Receiver
- Protocol: TCP
- Receiving at :30
- Receive buffer size: 256 bytes
The file 'SuperB_data.txt' was opened
C:\qdrives\angel..._CylII_development\SuperB_PC_side\benchmark_source
[NiosII EDS] $ ./bm -m:30 -p tcp -b256
- SuperB_Proto Test Role: Receiver
- Protocol: TCP
- Receiving at :30
- Receive buffer size: 256 bytes
The file 'SuperB_data.txt' was opened
**** listen_socket : 6 ****

```

Debug console for the NIOS-II microcontroller on board the IFR_FE_BIRO_TLU.
The NIOS-II executes 2 task: a "simple socket server" connected to the run control task on the host PC and the "event transmission" which sends data to the host PC

```

Date - October 24, 2006
Module - simple_socket_server.c
*****
Simple Socket Server (SSS) example.
*****
Software License Reminder
This software project uses an unlicensed version of Network Stack - Nios II Edition. If you want to ship code in your product, you must purchase a license for Altera. For information go to: "http://www.altera.com"
portable TCP/IP, v3.1
Copyright (c) 1996-2008 by InterNiche Technologies. All rights reserved.
0
eth MAC address is 00:07:ed:ff:4a:7d
IP address is 137.57.235.80
Network interface, initializing...
[0]
Ethernet MAC 0 found at address 0x01003800
PHY Marvell 88E1111 found at PHY address 0x12 of MAC Group[0]
FY[0.0] - Automatically mapped to cse_mac_device[0]
FY[0.0] - Restart Auto-Negotiation, checking PHY link...
FY[0.0] - Auto-Negotiation PASSED
FY[0.0] - Checking link...
FY[0.0] - Link established
FY[0.0] - Speed = 1000, Duplex = Full
CONFIG=0x00000000
Initialization: CMD_CONFIG=0x0400020b
read init[] RX descriptor chain desc (1 depth) created
called
of eth : 137.57.235.80
start main" task (Prio: 2)
clock tick" task (Prio: 3)
Simple Socket Server starting up
[sss_task] Simple Socket Server listening on port 50
Created "simple socket server" task (Prio: 4)
Created "event transmission module" task (Prio: 6)
"talk" Socket creation succeeded
"talk" Socket is connected!!!
sss_handle_accept: sizeof(incoming_addr): 16
[sss_handle_accept] accepted connection request from 137.57.235.81

```

RUN CONTROL task on the host PC

Available commands are, up to now:

- BIRO_TLU_config
- ABCD_init
- ABCD_ratemeter
- RUN_start
- RUN_stop

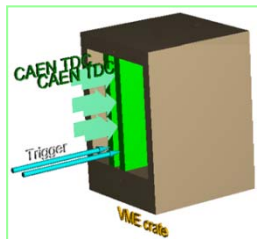
```

AVAILABLE COMMANDS:
ABCD_CFG_SEND
ABCD_UPDATE
RUN_START
RUN_STOP
RATEMETER_RDBCK
STORE_BIRO_CFG
IPGEN
STORE_ABCD_CFG
ABCD_CFG_STORE_NUM
ABCD_CFG_RDBCK
RUN_INIT
Enter your choice & press return:
after FD_SET(STDIN..) max_socket: 1
Before gets
quit
The line entered was: quit
- Test Role: Sender
- Protocol: TCP
- Status: Completed
- Total Bytes: 339
- Total Time: 13.321000 seconds
- Bits per second: 203.588318 bits/sec
- Total Packets: 1
C:\qdrives\angel..._CylII_development\SuperB_PC_side\benchmark_source
[NiosII EDS] $ ./bm -m:137.57.235.80:50 -p tcp -b256 -d100
- SuperB_Proto Test Role: Sender
- Protocol: TCP
- Sending to 137.57.235.80:50
- Send buffer size: 256 bytes
The file 'superBproto_param.txt' is open
The file 'superBproto_log.txt' is open
after FD_SET(STDIN..) max_socket: 1
Past call to recv()
SuperB BiRO Control menu
AVAILABLE COMMANDS:
ABCD_CFG_SEND
ABCD_UPDATE
RUN_START
RUN_STOP
RATEMETER_RDBCK
STORE_BIRO_CFG
IPGEN
STORE_ABCD_CFG
ABCD_CFG_STORE_NUM
ABCD_CFG_RDBCK
RUN_INIT
Enter your choice & press return:

```

Preliminary test results: screenshots from the notebook used to control and collect data from the **IFR_FE_BiRO** crate

SuperB IFR electronics : update on prototype electronics and DAQ



“TDC subsystem” features:

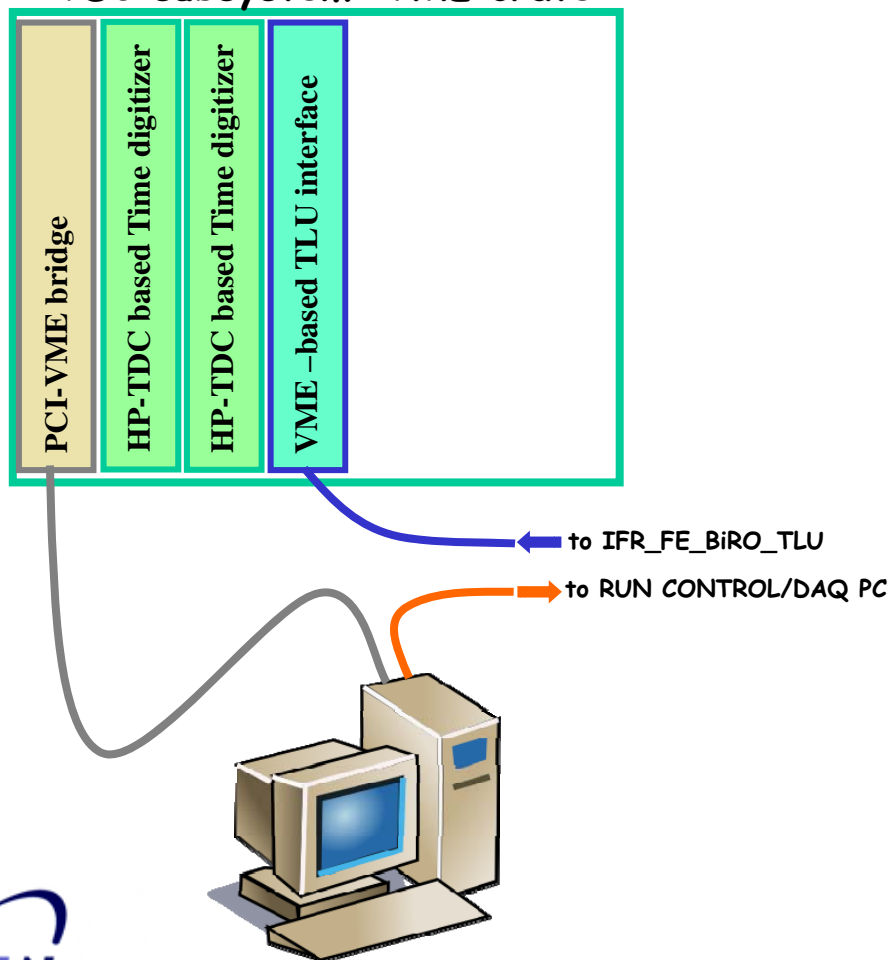
The **TDC subsystem** uses 2 commercial TDC modules based on CERN's HP-TDC to digitize the time of arrival of the pulses from the “ABCD” boards.

The **TDC subsystem** will also use a VME-based module to interface to the “**IFR_FE_BiRO_TLU**” and receive trigger/timing signals

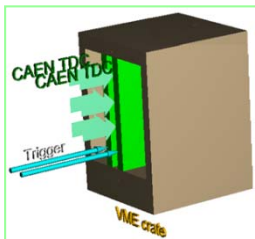
The **TDC subsystem** VME crate will be controlled and read out by the “TDC-PC” via a PCI-VME bridge.

The TDC_PC will then send the triggered data to the RUN CONTROL/DAQ PC via a TCP/IP connection.

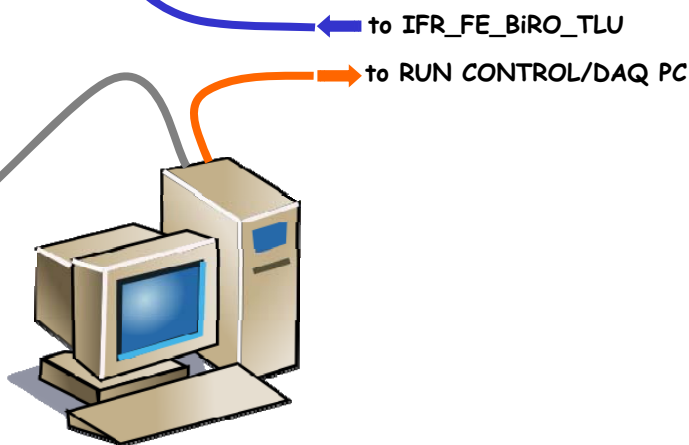
“TDC subsystem” VME crate



SuperB IFR electronics : update on prototype electronics and DAQ



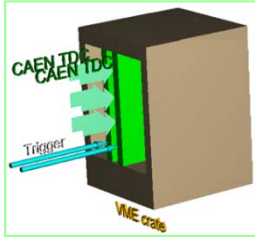
"TDC subsystem" VME crate



"TDC subsystem" status update :

- TDC readout: DONE
- port toward the Online Detector Control program : DONE,
- acknowledgments to **Stefano Chiozzi**, INFN-Ferrara and **Nicola Dalpasso**, above, undergraduate student at the Ferrara University

SuperB IFR electronics : update on prototype electronics and DAQ



Introduction

- The aim is to read events from multiple TDC modules and send them to another computer via TCP / IP.
- A busy logic is introduced to block new events before the previous is read.
- The TDC's readout buffer hold no data or the data of a single event.



XIV SuperB Meeting - LNF

Sept-28-2010

NICOLA DALPASSO, Università Ferrara



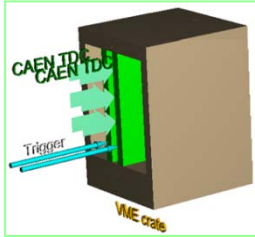
XIV SuperB Meeting - LNF

Sept-28-2010

A.Cotta Ramusino, INFN Ferrara

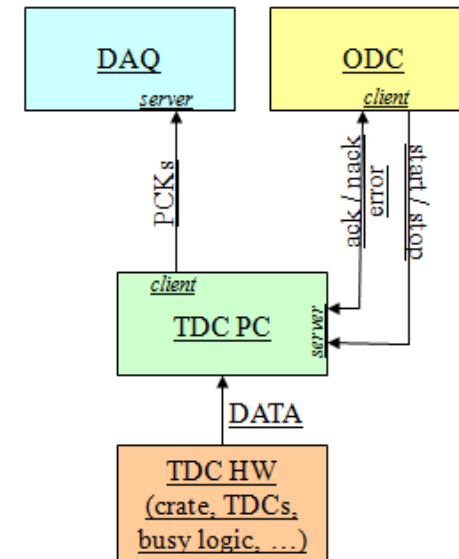


SuperB IFR electronics : update on prototype electronics and DAQ

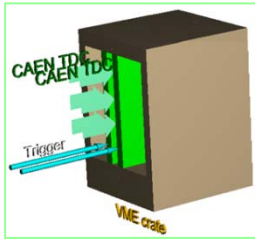


Overview

- The job of the TDC PC is:
 - to respond to start/stop acquisition commands. The ACK and NACK messages confirm the correct execution of the operation. Data acquisition errors are signaled via an error message to the ODC.
 - send acquired data to DAQ
- TCP/IP protocol is used for communication between TDC PC and DAQ / ODC.

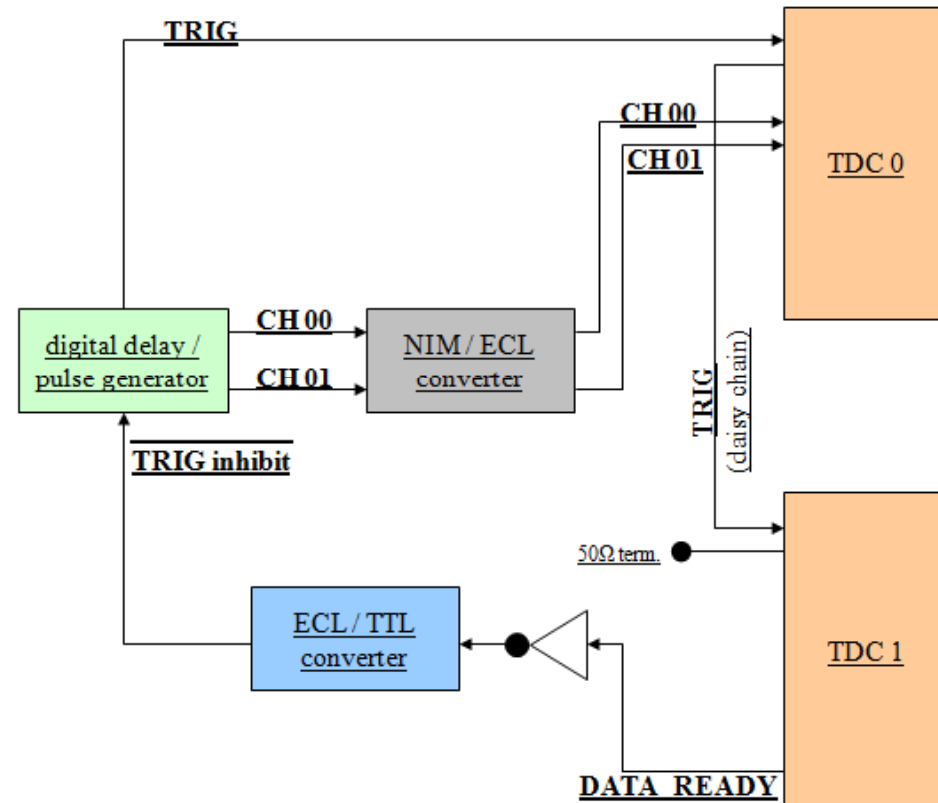


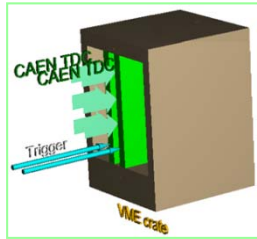
SuperB IFR electronics : update on prototype electronics and DAQ



Overview (2)

- We are using only 2 TDCs (with, at the moment, only 2 inputs driven from the timing generator)
- TDCs are operated in trigger matching mode
- TDC's OUT_PROG outputs programmed to indicate the DATA_READY status
- The OUT_PROG output of the last TDC is used to create the busy logic

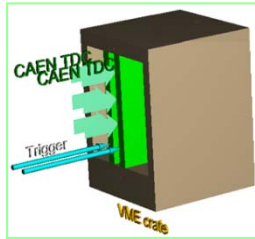




Read an event

- Steps to read a single event:
 - wait the DATA_READY flag for each TDC module, through polling the Status Register
 - read all the data (enclosed between Global Header and Global Trailer) from the TDCs
- Busy logic: a new event active the OUT_PROG output which is then negated and converted to TTL levels. This signal inhibit the trigger blocking the creation of new events. When all the data are read from the last TDC, the OUT_PROG is deactivated and the trigger is enabled.

SuperB IFR electronics : update on prototype electronics and DAQ



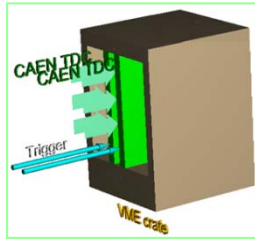
Format of the packets

- Data from a single event are copied in a packet and a header (holding the total size of the packet) and a trailer are added. The packet is then sent to DAQ.

Example of a packet:

```
0x78600000 : TDC PC HEADER : BYTE COUNT 0096 : TRIGGER NUMBER 00000
0x4000001f : CAEN TDC GLOBAL HEADER : EVENT COUNT 00000000 : GEO 31
0x0800076b : TDC CHIP HEADER : TDC 0 : EVENT ID 00000000 : BUNCH ID 00001899
0x00076d52 : TDC DATA : EDGE 0 : CHANNEL 0000 : DATA 00486738
0x00176e97 : TDC DATA : EDGE 0 : CHANNEL 0002 : DATA 00487063
0x18000004 : TDC CHIP TRAILER : TDC 0 : EVENT ID 00000000 : WORD CNT 00000004
0x0900076b : TDC CHIP HEADER : TDC 1 : EVENT ID 00000000 : BUNCH ID 00001899
0x19000002 : TDC CHIP TRAILER : TDC 1 : EVENT ID 00000000 : WORD CNT 00000002
0x0a00076b : TDC CHIP HEADER : TDC 2 : EVENT ID 00000000 : BUNCH ID 00001899
0x1a000002 : TDC CHIP TRAILER : TDC 2 : EVENT ID 00000000 : WORD CNT 00000002
0x0b00076b : TDC CHIP HEADER : TDC 3 : EVENT ID 00000000 : BUNCH ID 00001899
0x1b000002 : TDC CHIP TRAILER : TDC 3 : EVENT ID 00000000 : WORD CNT 00000002
0x8400019f : CAEN TDC GLOBAL TRAILER : STATUS 4 : WORD CNT 00000012 : GEO 31
0x4000001f : CAEN TDC GLOBAL HEADER : EVENT COUNT 00000000 : GEO 31
0x08000115 : TDC CHIP HEADER : TDC 0 : EVENT ID 00000000 : BUNCH ID 00000277
0x18000002 : TDC CHIP TRAILER : TDC 0 : EVENT ID 00000000 : WORD CNT 00000002
0x09000115 : TDC CHIP HEADER : TDC 1 : EVENT ID 00000000 : BUNCH ID 00000277
0x19000002 : TDC CHIP TRAILER : TDC 1 : EVENT ID 00000000 : WORD CNT 00000002
0x0a000115 : TDC CHIP HEADER : TDC 2 : EVENT ID 00000000 : BUNCH ID 00000277
0x1a000002 : TDC CHIP TRAILER : TDC 2 : EVENT ID 00000000 : WORD CNT 00000002
0x0b000115 : TDC CHIP HEADER : TDC 3 : EVENT ID 00000000 : BUNCH ID 00000277
0x1b000002 : TDC CHIP TRAILER : TDC 3 : EVENT ID 00000000 : WORD CNT 00000002
0x8400015f : CAEN TDC GLOBAL TRAILER : STATUS 4 : WORD CNT 00000010 : GEO 31
0xb8000000 : TDC PC TRAILER : STATUS ERROR 0000 : TRIGGER NUMBER 00000
```





Behavior of the TDC PC

- The behavior of the data acquisition program is illustrated in the FSM bubble diagram. **Blue** lines mean the operation requested succeeds, otherwise a **red** line is used.
- For each command received, an ack/nack message is sent.
- Running errors are signaled to the OCL via an error message and the running continue.
- INIT is the initial state: in this state a TDC setup is done and then the program waits for connection from the OCL.

