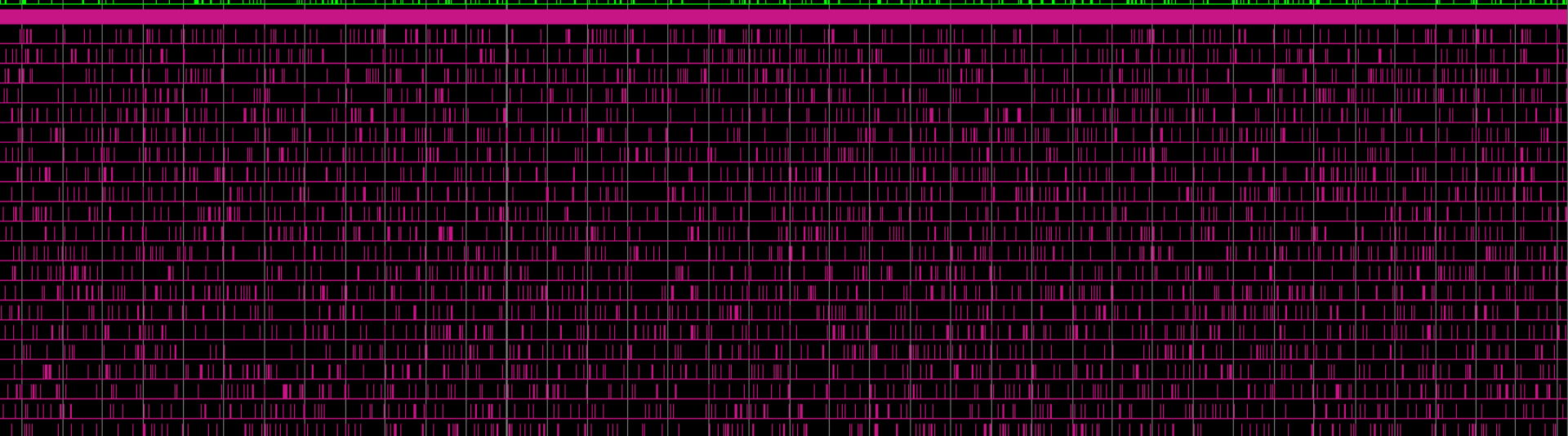


Pixel readout simulation updates

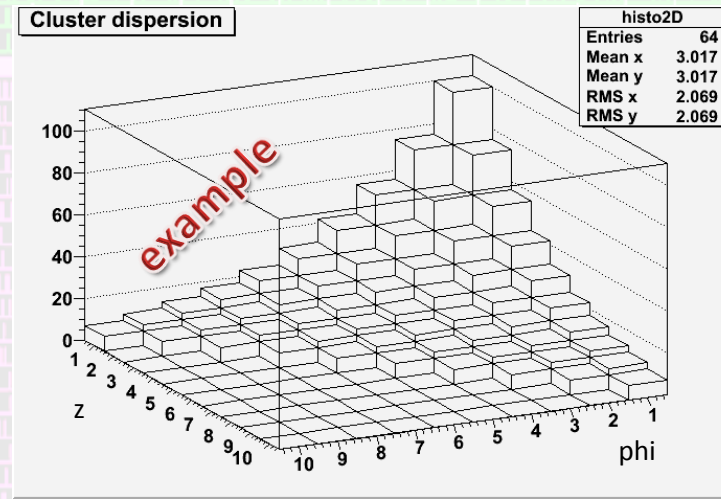
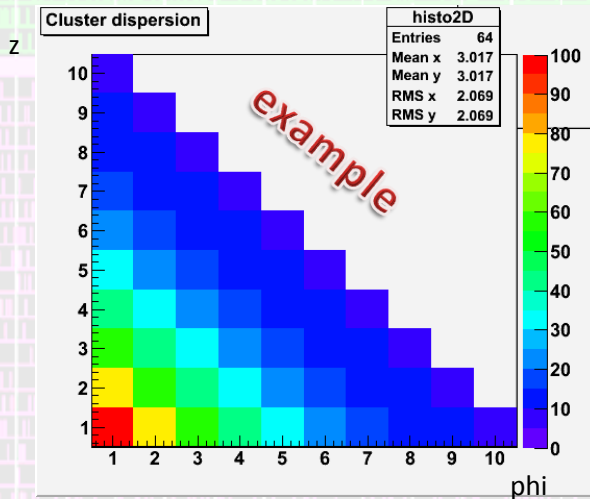


Outline

- Updates on:
 - Monte Carlo Hit generator
 - Simulation Environment
 - Integration of Cluster Distributions from Physics Simulations
 - SQUARE Readout Core

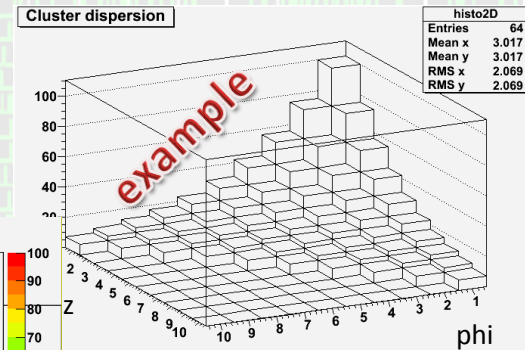
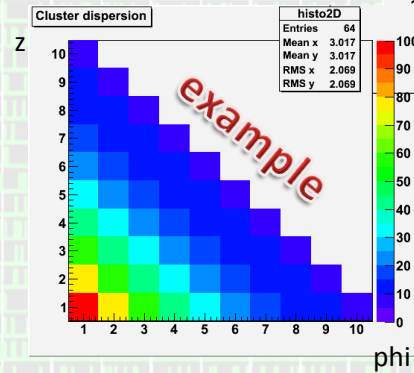
Monte Carlo Hit Generator

- Monte Carlo generator
 - Rewritten from scratch
 - Now generation of **clustered** events
 - **Knobs:**
 - Cluster dispersion distribution in (z,phi)
 - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate

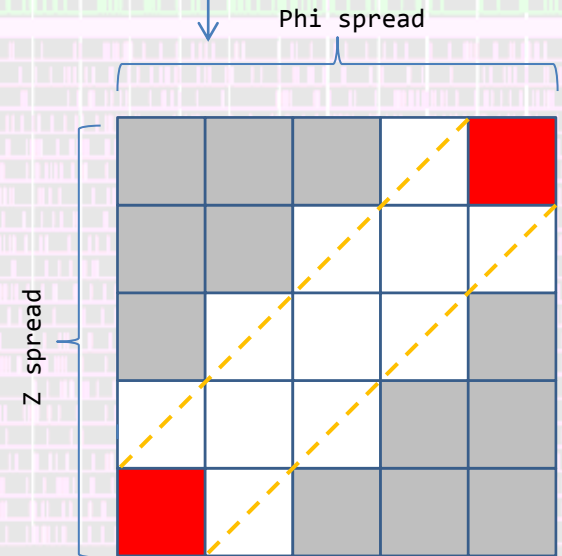


Monte Carlo Hit Generator

- Arbitrary pattern extraction by geometrical rules

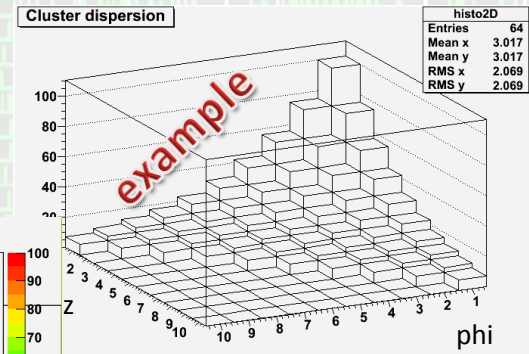
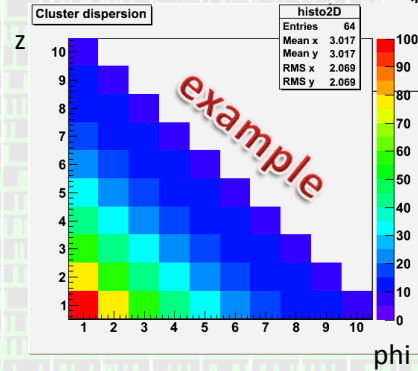


Cluster spread extraction
Es. (5,5)



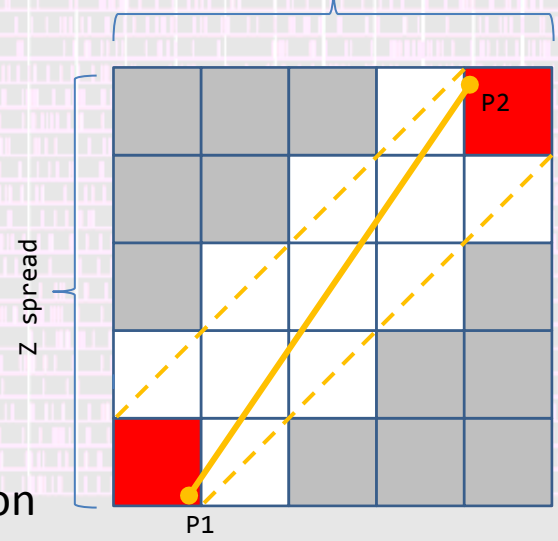
Monte Carlo Hit Generator

- Arbitrary pattern extraction by geometrical rules



Cluster spread extraction
Es. (5,5)

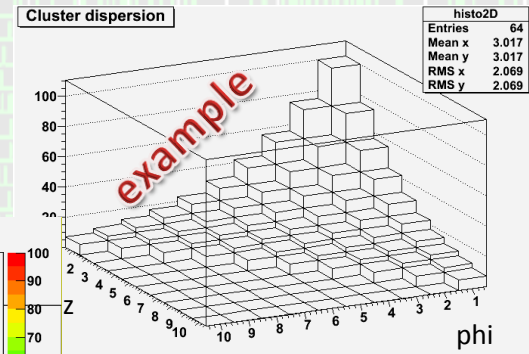
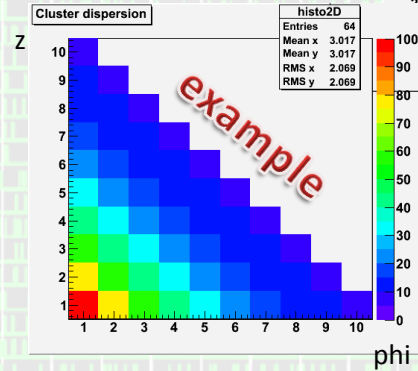
Phi spread



P1- P2 points extraction

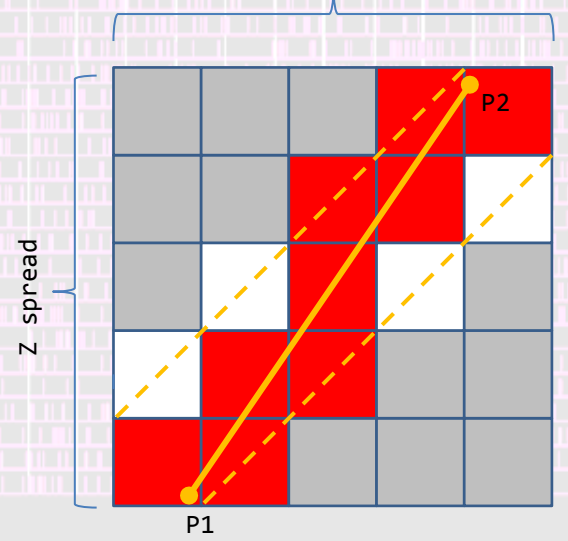
Monte Carlo Hit Generator

- Arbitrary pattern extraction by geometrical rules



Cluster spread extraction
Es. (5,5)

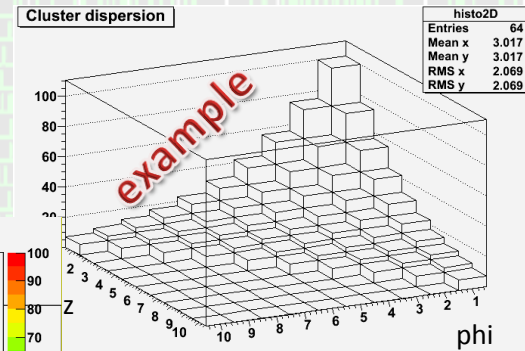
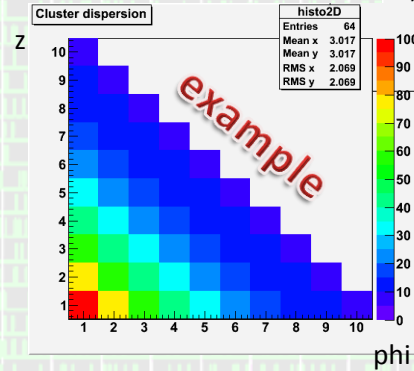
Phi spread



Pattern evaluation

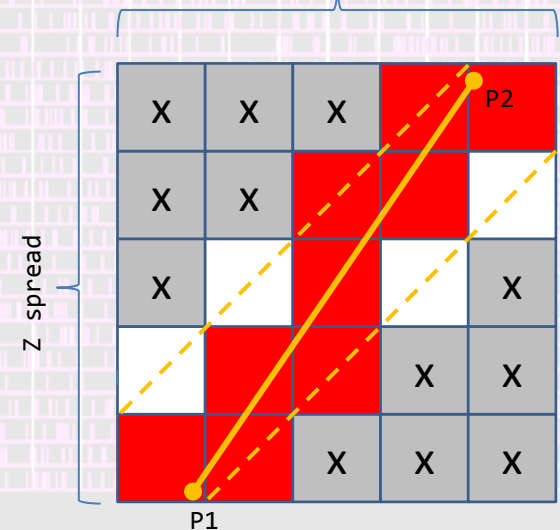
Monte Carlo Hit Generator

- Arbitrary pattern extraction by geometrical rules
- Pattern check (grey pixels are forbidden)



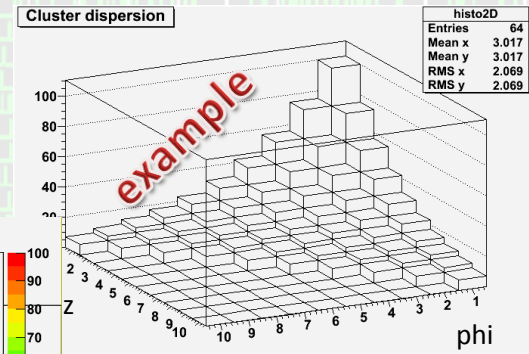
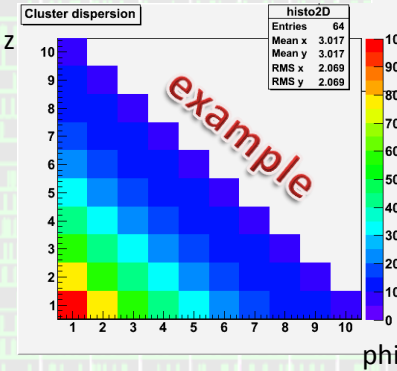
Cluster spread extraction
Es. (5,5)

Phi spread



Monte Carlo Hit Generator

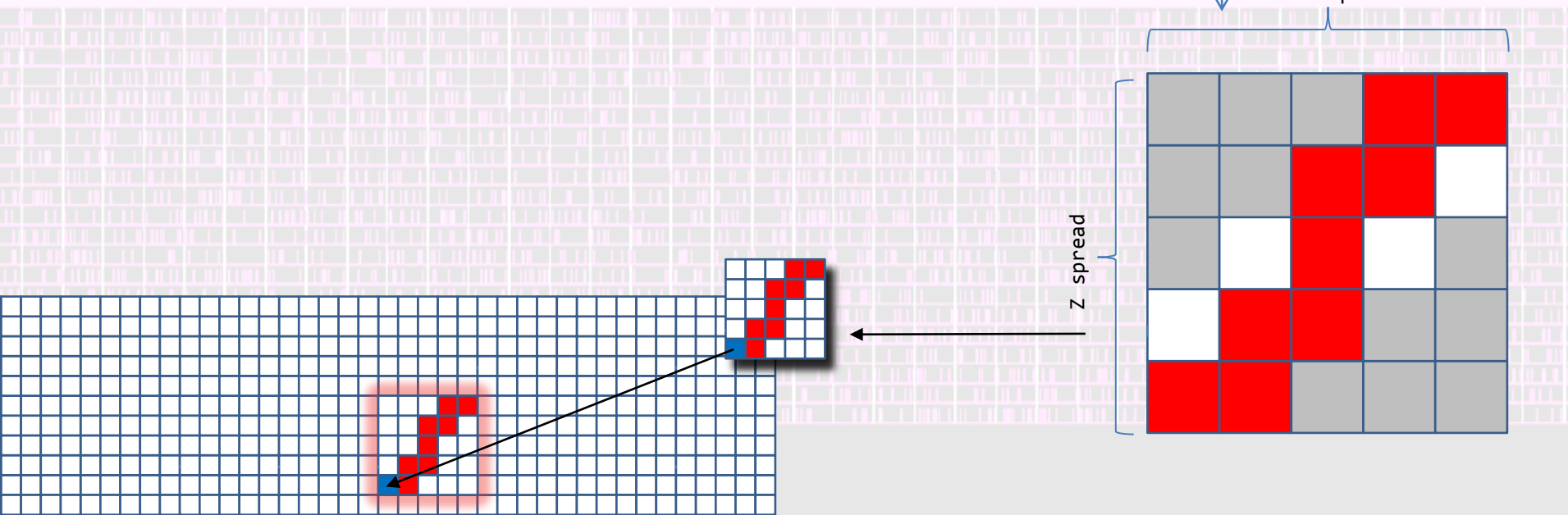
- Arbitrary pattern extraction by geometrical rules
- Pattern check (grey pixels are forbidden)
- Pattern application to a random pixel of the matrix



Cluster spread extraction
Es. (5,5)

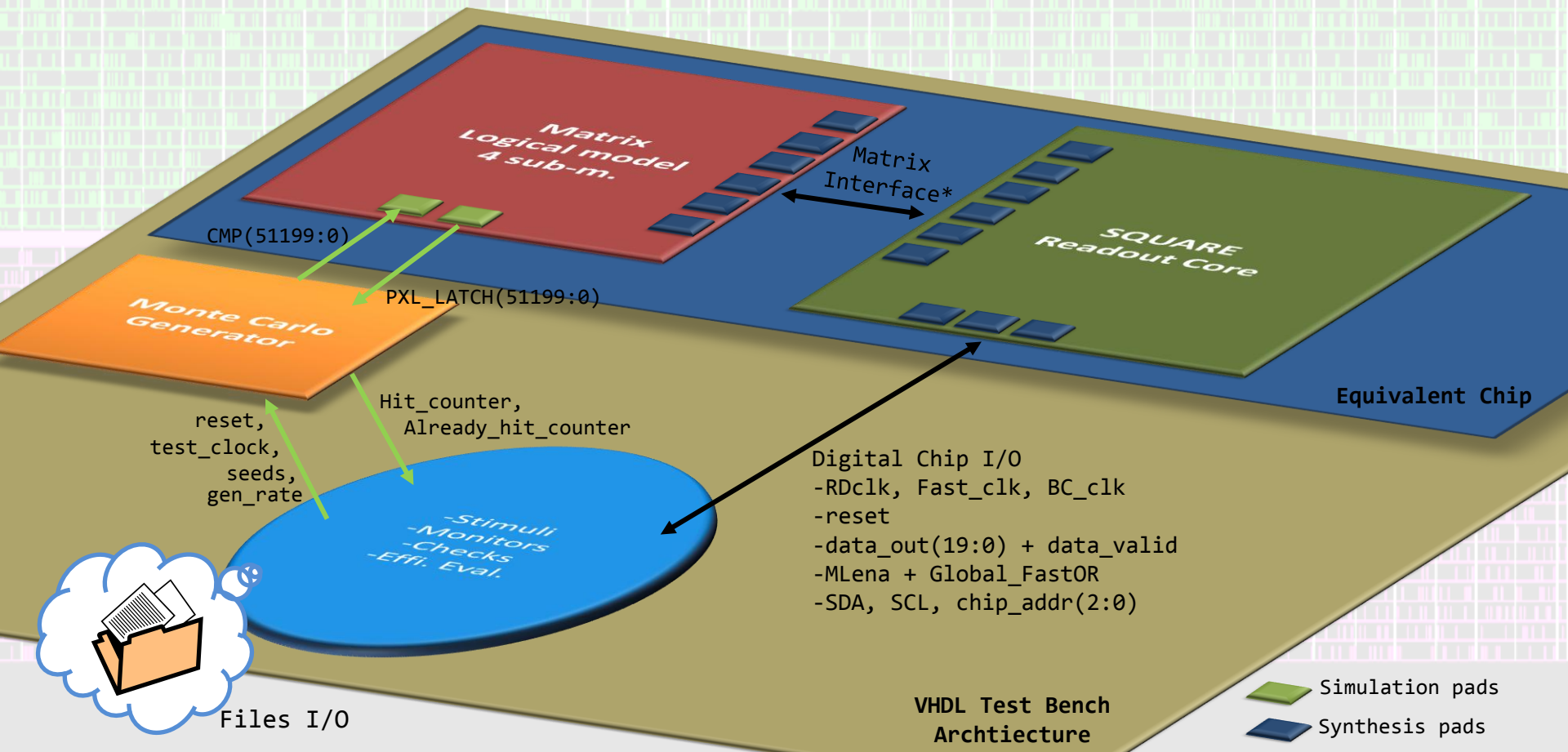
Phi spread

Z spread



Simulation Environment

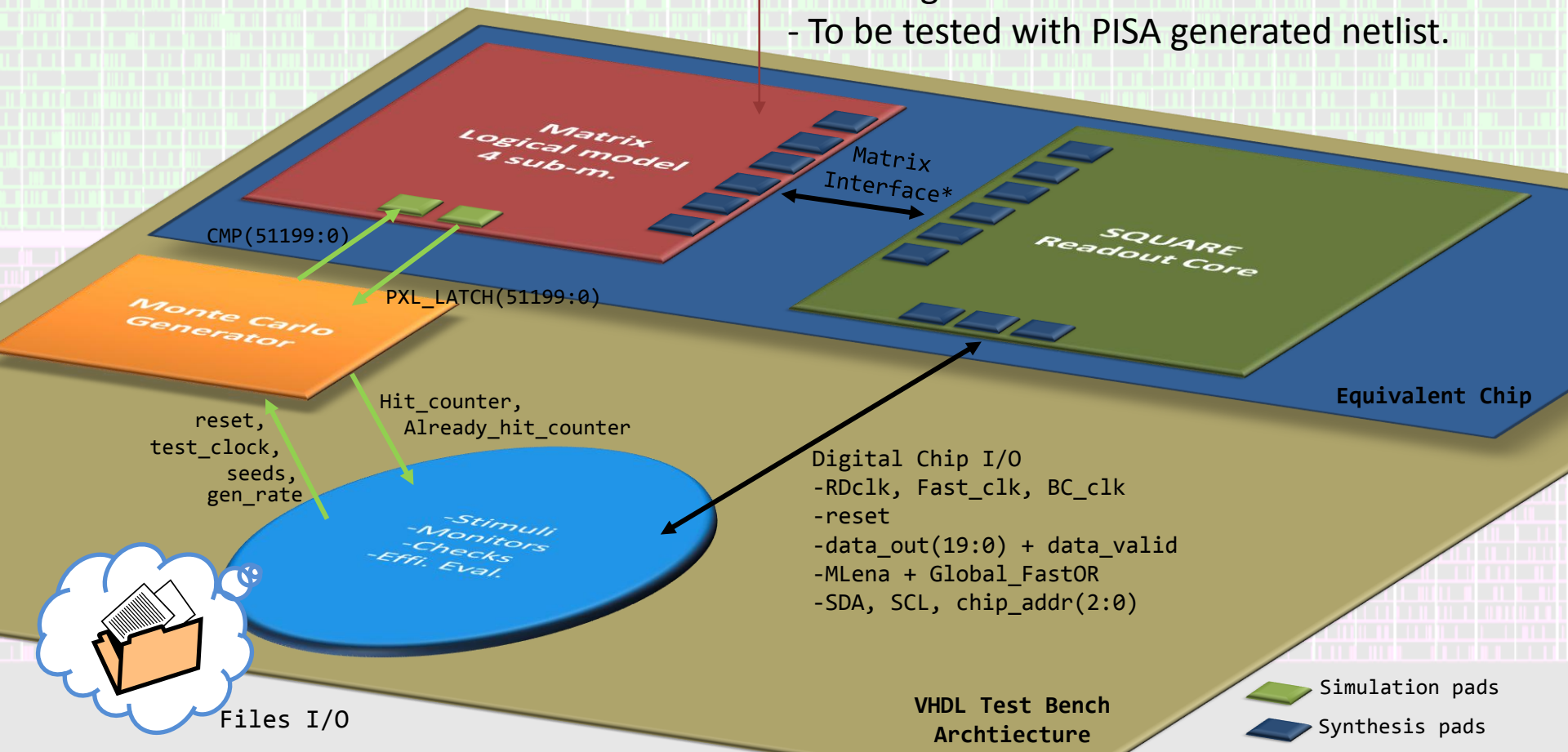
- Simulation Tool: **Modelsim SE 6.3f**
- Simulation components
 - **Readout Core Arch. SQUARE** (.vhd synthesizable code)
 - **Monte Carlo Generator** (.vhd **NOT** synthesizable code)
 - **Matrix Behavioral Model** (.vhd/.v code)
 - **Test Bench** (.vhd code)



Simulation Environment

- Simulation Tool: **Modelsim SE 6.3f**
- Simulation components
 - **Readout Core Arch. SQUARE** (.vhd synthesizable code)
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 - **Matrix Behavioral Model** (.vhd/.v code)
 - **Test Bench** (.vhd code)

Logical model of digital matrix components:
- Now logic model made in BO.
- To be tested with PISA generated netlist.



SQUARE architecture tests with new test bench infrastructure

Preliminary simulations with matrix model
made in Bo and hypothetic cluster distribution

Try-outs

(rate: 100MHz/cm², duration: 3 ms, statistics: 350k/400k hits):

classic simulation, 100 MHz/cm², NO cluster

	1	2	3	4
1	100%	0%	0%	0%
2	0%	0%	0%	0%
3	0%	0%	0%	0%
4	0%	0%	0%	0%

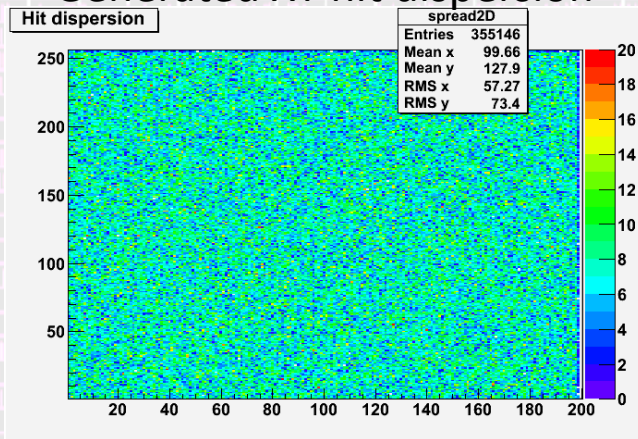
Cluster Factor=1

TEST: Symmetrical Cluster spread in zeta/phi

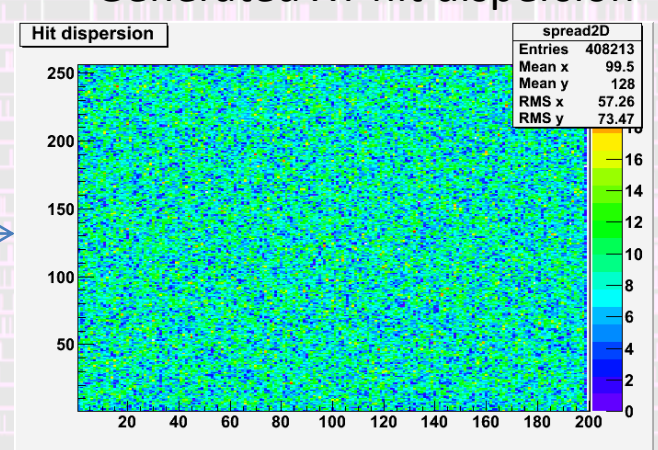
	1	2	3	4
1	50%	12.5%	4%	1%
2	12.5%	4%	1%	0%
3	4%	1%	0%	0%
4	1%	0%	0%	0%

Cluster Factor 1.4

Generated XY hit dispersion



Generated XY hit dispersion

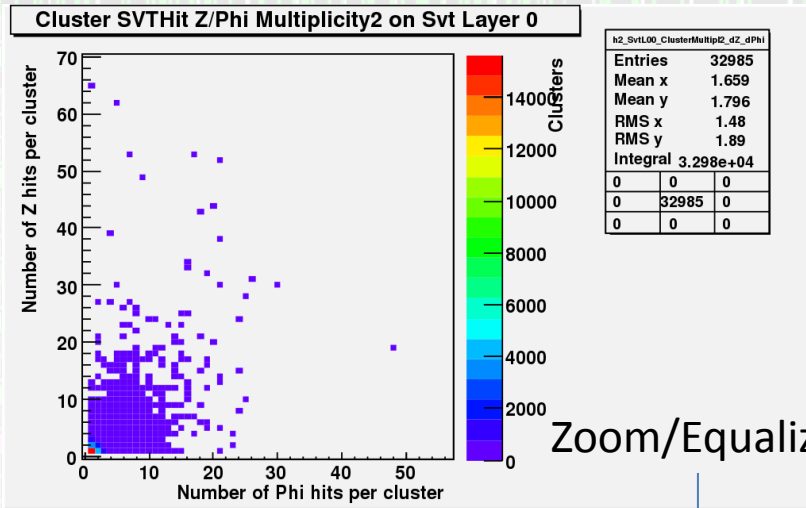


About optimization: 350k hits → >350k words

400k hits → ~300k words, save 25% bandwidth

Integration of physical cluster distribution

- **CLUSTER SPREAD DISTRIBUTION NOW FROM PHYSICS SIMULATIONS**
- Connection point between physics and electronics simulation

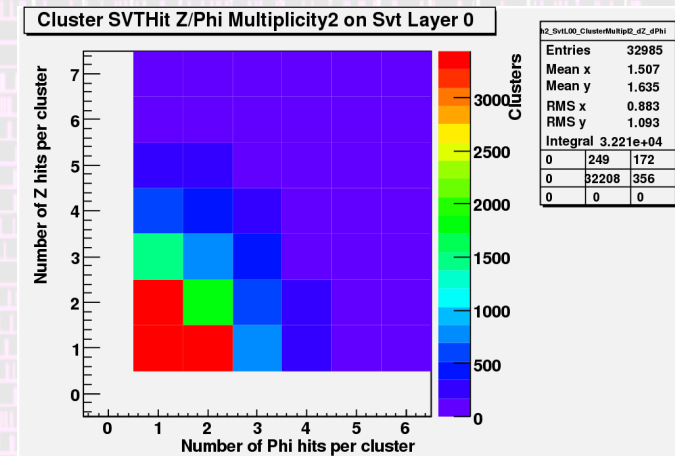
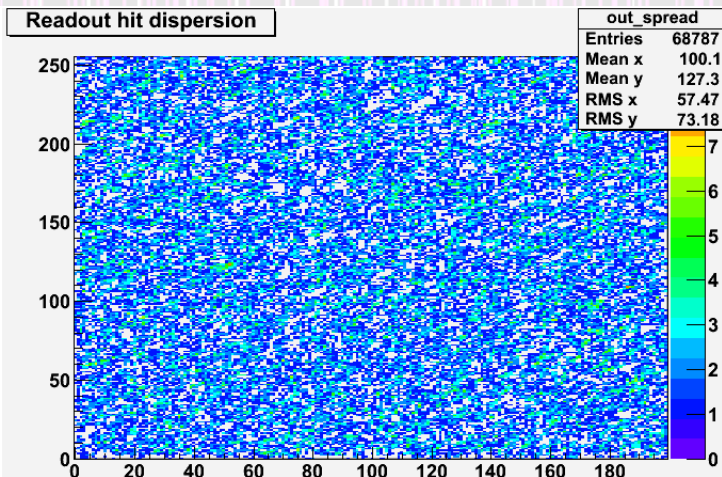


%	1	2	3	4	phi
1	47,28	12,65	2,47	0,71	...
2	10,62	5,81	1,77	0,56	
3	4,32	2,31	1,07	0,40	
4	2,01	1,15	0,57	0,27	
zeta	...				

Data from physic simulations by **R.Cenci**

Zoom/Equalize

Implemented and simulated



XY Hit disperion on sensor (electronics simulation)

Zone algorithm effects:

Statistics : 70k hits →

Zones along beam direction (Z) ~58k words → compression factor ~ 15%

Zone algorithm effects:

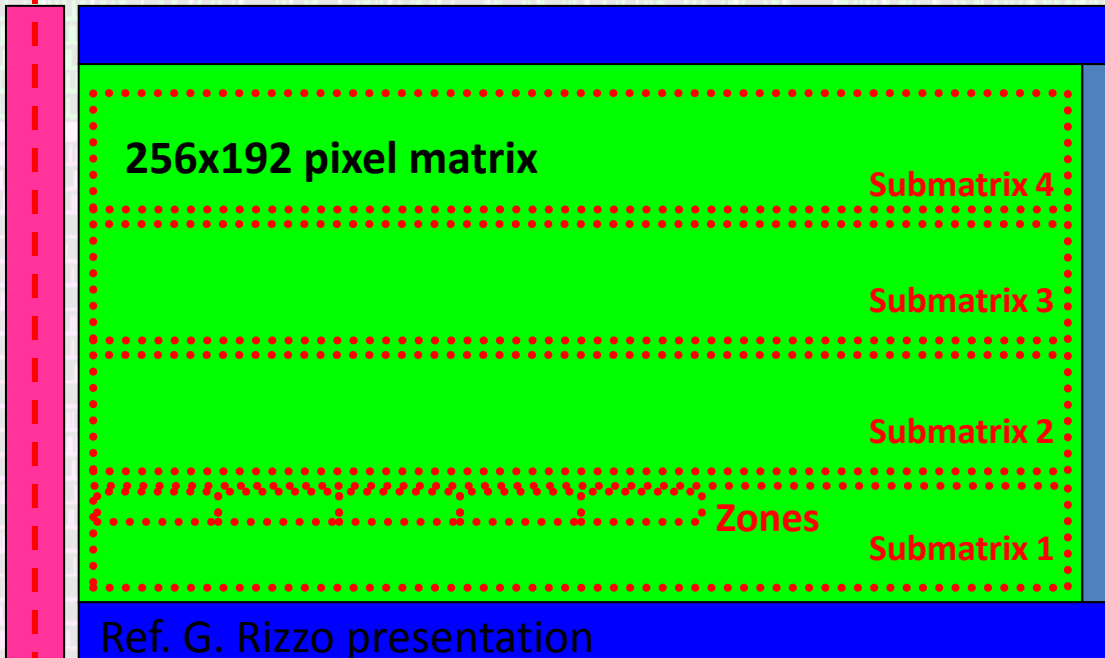
Statistics : 70k hits →

Zones along beam direction (Z) ~58k words → compression factor ~ 15%

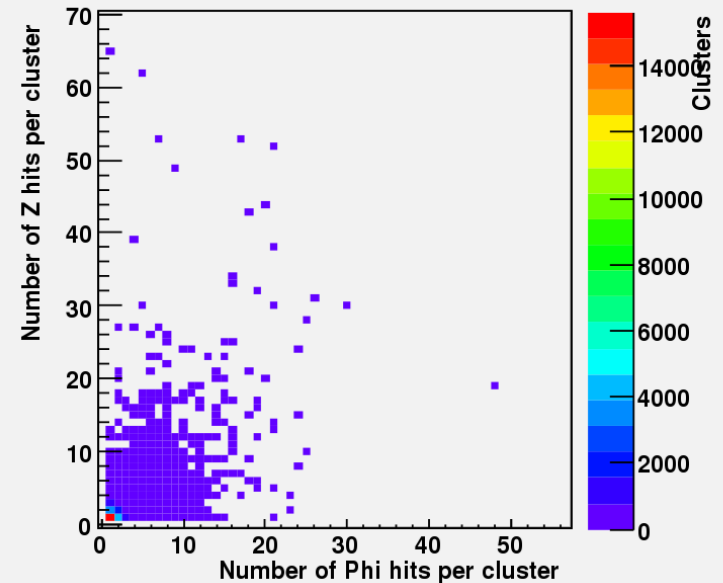
Zones along Phi direction ~62k words → **compression factor ~ 10%**

(Current chip/module project)

↑
Z axis



Cluster SVTHit Z/Phi Multiplicity2 on Svt Layer 0



Phi axis →

Zone algorithm effects:

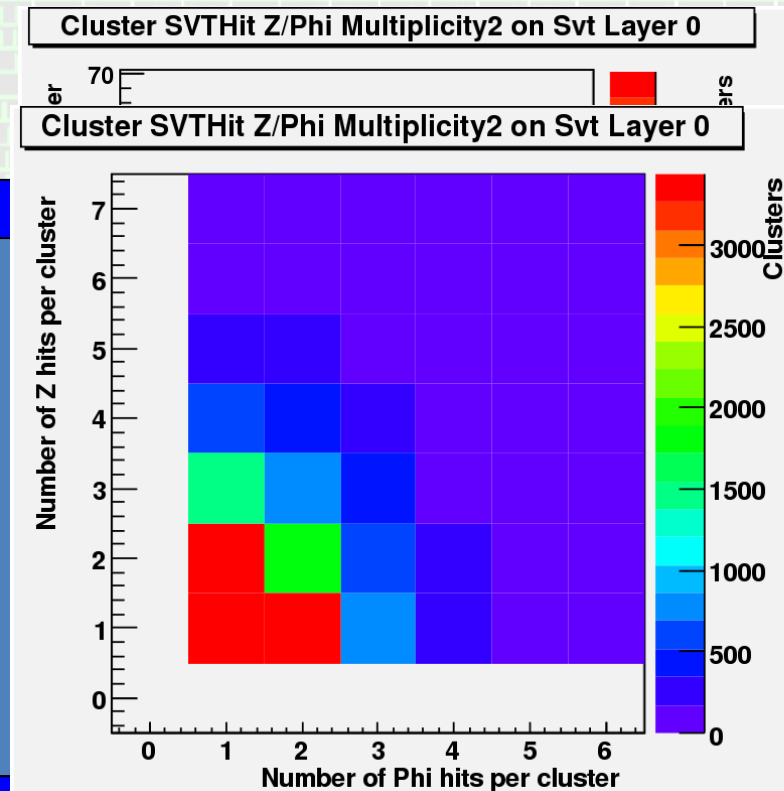
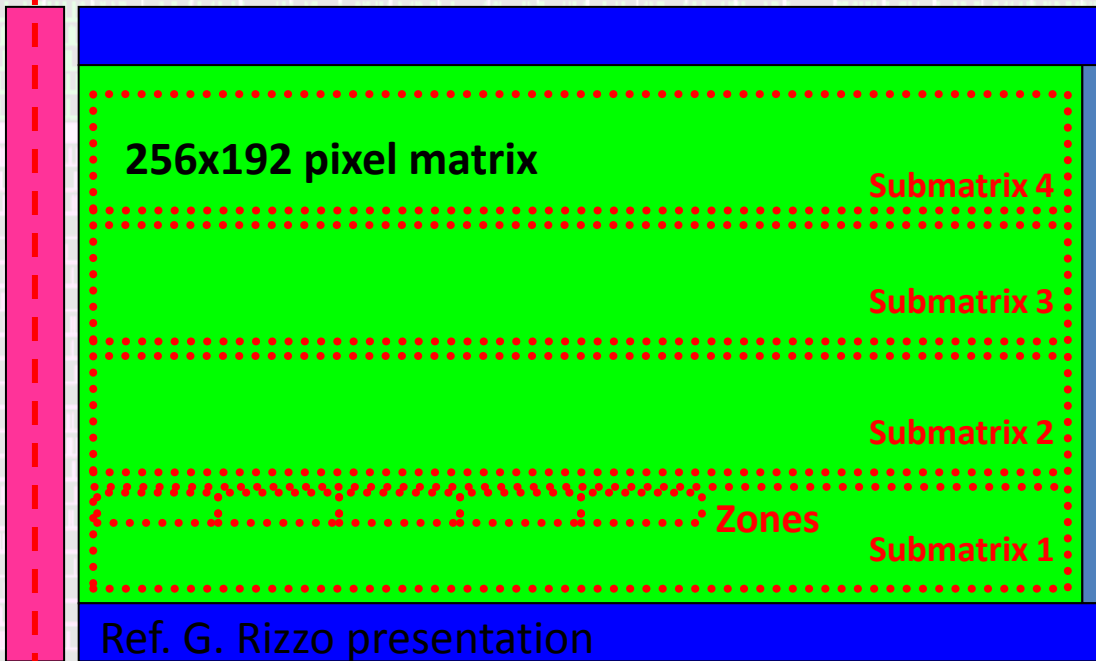
Statistics : 70k hits →

Zones along beam direction (Z) ~58k words → compression factor ~ 15%

Zones along Phi direction ~62k words → compression factor ~ 10%

(Current chip/module project)

↑
Z axis



→
Phi axis

Simulation Checks

- Time Stamps Check (all for all sub-matrices, sorting)
- Generated hits VS Read Out hits (cross check)
- Barrels overflow monitor
- Barrels average fill level monitor
- Errors detection at concentrators level (Missing TS...)

SQUARE READOUT CORE

- NEWS
 - Improved algorithm on concentrators (shorter BC → more chaotic time sorting).
 - Re-organized register set.
 - Row and column masks (Readout masks) over I2C.
 - Matrix masks setting protocol over I2C.
- On the Way...
 - Triggered sweeper algorithms with selectable latency.
 - Code optimization for clock speed and synthesis time.
- TO DO
 - Calibration mode
 - Tailor the SQUARE readout for APSEL_VI & SuperPX1
 - First Synthesis with new Design Kit

Conclusions

- Simulation environment ready for:
 - Intensive simulations with Physical events for efficiency estimations.

Conclusions

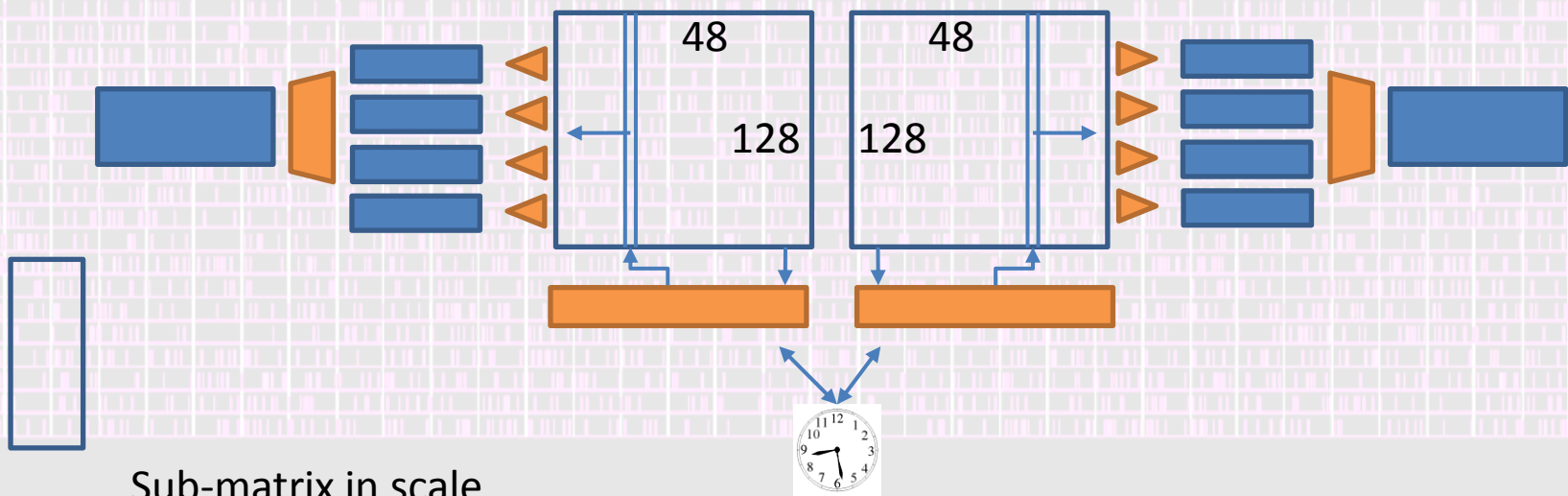
- Simulation environment ready for:
 - Intensive simulations with Physical events for efficiency estimations.
 - Intensive simulations with extracted netlist of matrix for **bug-hunting**.



BackUp

Readout for ApseVI Tezz. Char.

- MATRIX 128x96 (2 sub-m. 48x128)
 - 4 sparsifiers
 - 32 rows for each sparsifier
 - 8 zones for each sparsifier ($W_{\text{zone}}=4$ pixels)



Readout for Superpix1 Tezz. Char.

- MATRIX 32x128 (2 sub-m. 16x128)
 - 4 sparsifiers
 - 32rows for each sparsifier
 - 8 zones for each sparsifier ($W_{\text{zone}} = 4$ pixels)

