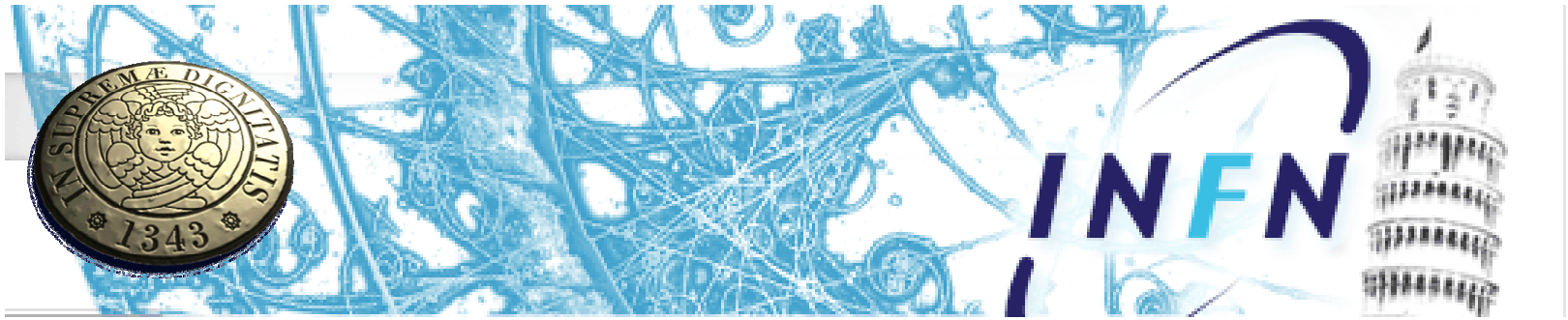
Update on SVT activities

S. Bettarini

Universita' di Pisa & INFN

on behalf of the SuperB SVT Group



XIV SuperB General Meeting @ INFN-LNF – Plenary session 1st Oct. 2010

Outline

- SVT: towards TDR
- Progress in R&D activities reported on the SVT parallel sections:

  - Pixel Layer0 read-out arch. (F.M.Giorgi)
  - Simulation BKG update (R.Cenci)
  - First Results from n-irr. Maps (S.B.)

  } SVT#1

  - Mechanics Layer0 support/cooling & B.P. (F.Bosi)
  - Progress in UK Activities on pixels (F.Wilson)
  - Activities in Trieste (L.Vitale) SVT1

  } SVT#2

  - Review talk on mimosa-MAPS by M. Winter
  - R&D on DNW MAPS (V.Re)
  - Aluminum bus & HDI (M.Citterio)

  } SVT#3

- Conclusions

SVT enters into the TDR phase

G.Rizzo

Layer0 Strategy

- Striplets baseline option:
  - Better physics performance (lower material ~0.5% vs 1% hybrid pixel, MAPS or thin hybrid pixel in between but not yet mature!)
- Upgrade to pixel (Hybrid or CMOS MAPS), more robust against background, foreseen for a second generation of Layer0

- SVT Mechanics will be designed to allow a quick access/removal of Layer0

Layer 1-5

- Double sided strip detectors modules (up to 37 cm long)

Describe the upgrade path for the Layer0: Status of the R&D on pixel (hybrid, CMOS MAPS, 3D pixels)

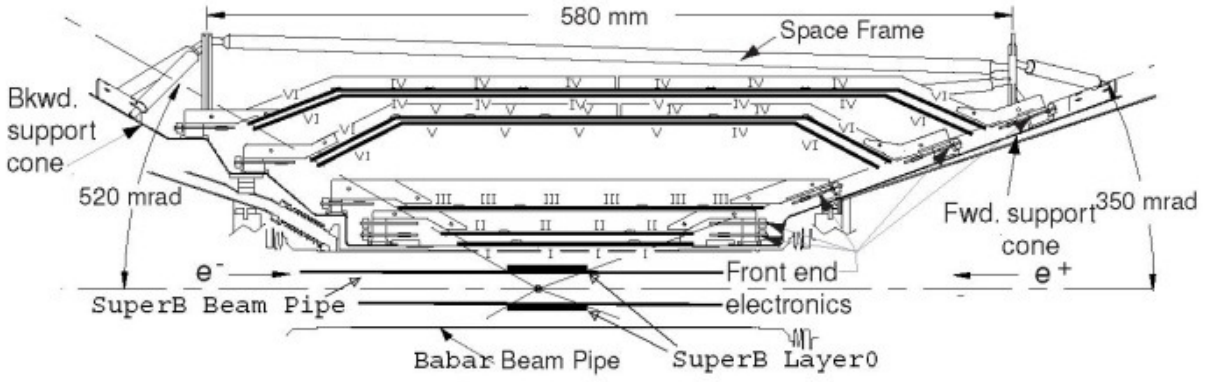
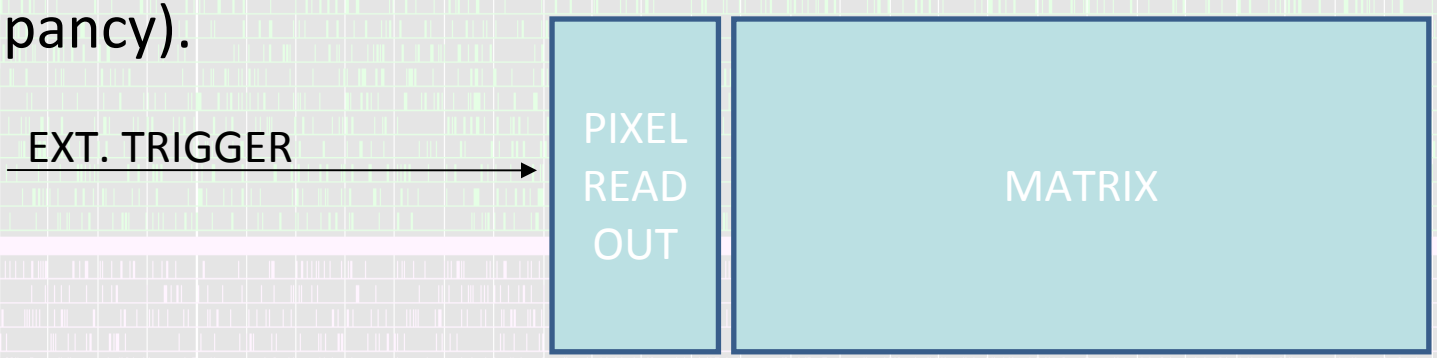


Figure 5: Longitudinal section of the SVT

Pixels Readout Core Updates

- NEW CAPABILITY
  - Under development a triggered architecture with no extra memory required on chip. (to be studied the trade off between trigger latency and increasing pixels occupancy).

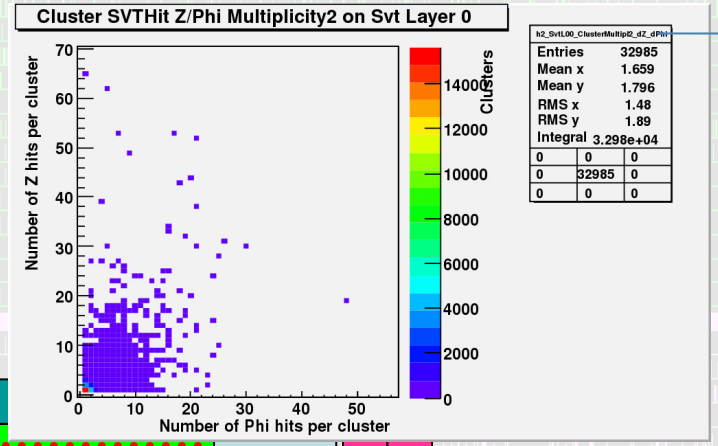


- IMPROVEMENTS
  - Improved algorithms on data concentrators (shorter BC → more chaotic time sorting).
  - Code optimization for clock speed and synthesis time.

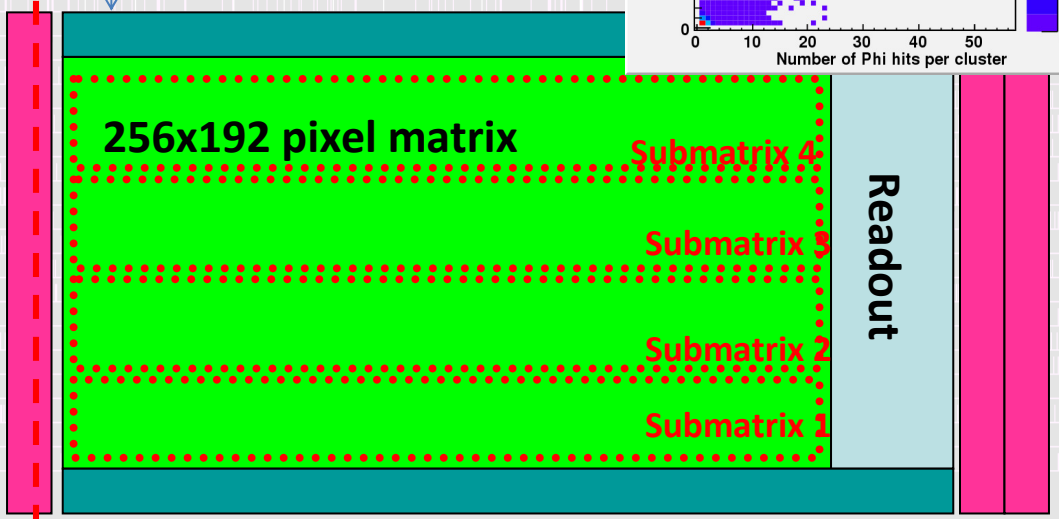
Pixels readout simulation environment: Integration of physical cluster distribution

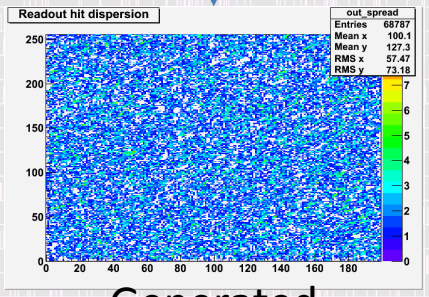
- **CLUSTER SPREAD DISTRIBUTION (Z-Phi)** NOW FROM **PHYSICS SIMULATIONS**
  - **Columns along Phi direction → compression factor ~ 10%**
  - (Columns along beam direction (Z) → compression factor ~ 15%)

Phys. Sim.
by **R.Cenci**



VHDL SIM

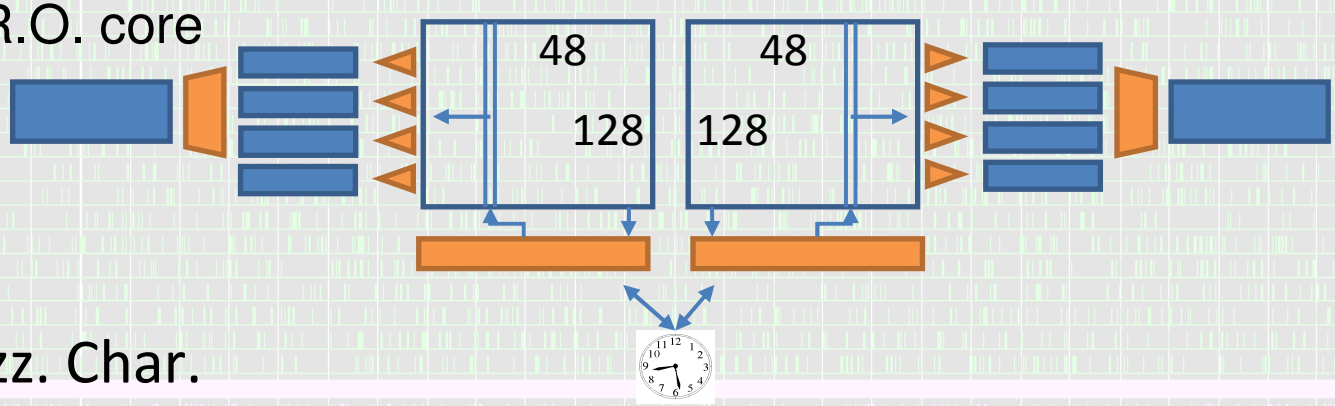




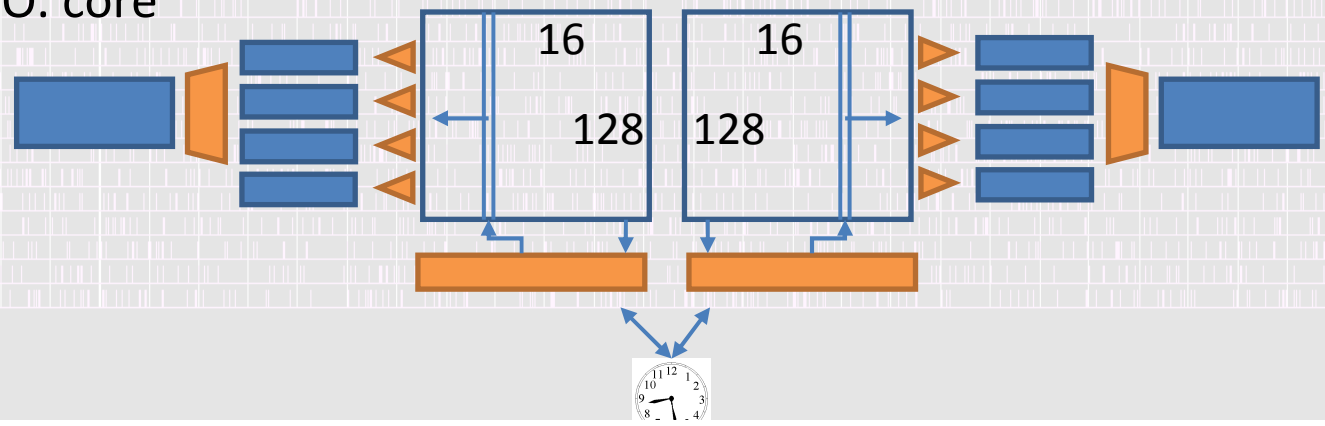
Generated
hit dispersion on sensor

Next 3D Submissions:

- **ApselVI** Tezz. Char.
  - 2 Tiers (MAP Sensor & Readout)
  - MATRIX **128x96** (2 sub-m. 48x128)
  - SQUARE R.O. core



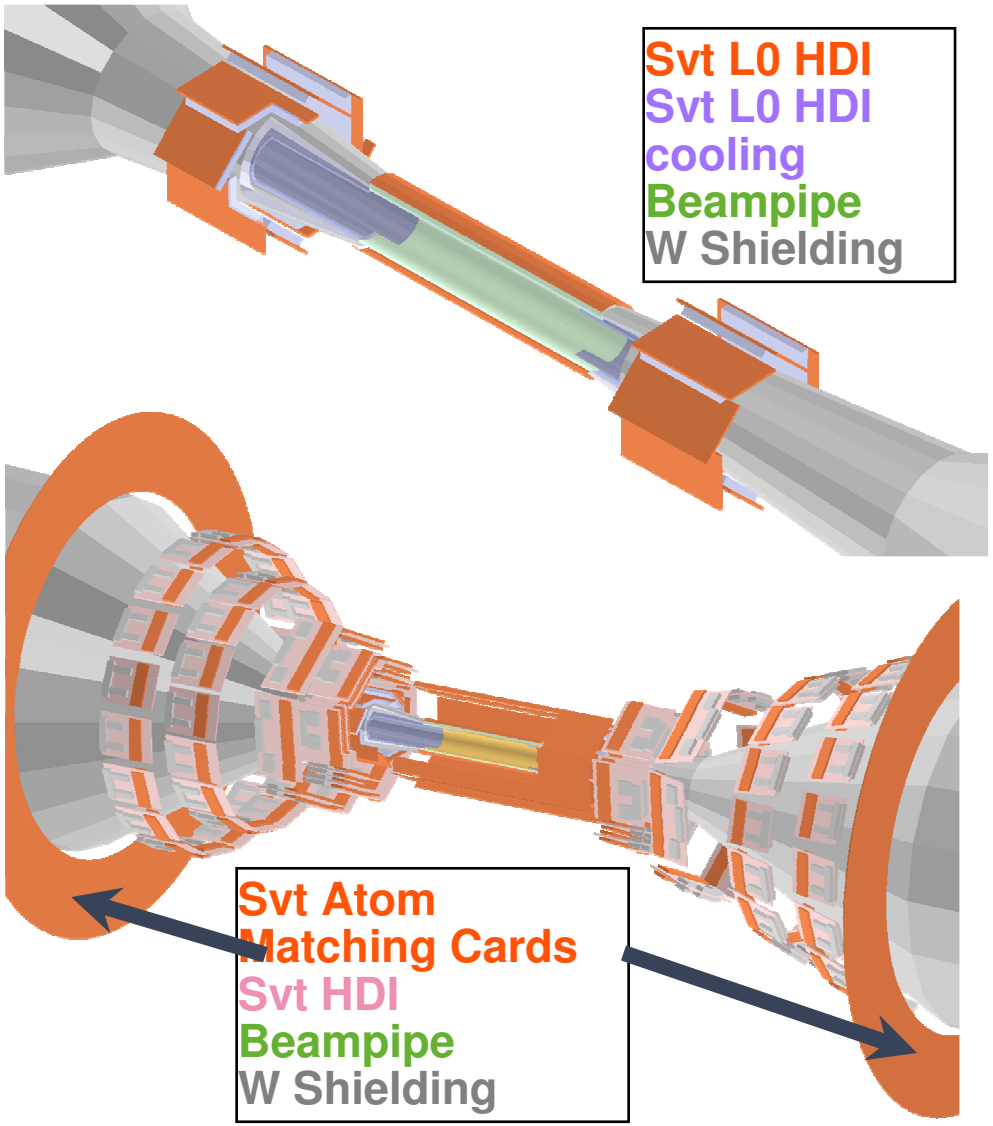
- **SuperPX1** Tezz. Char.
  - 2 Tiers (Digital & Analog) + bumb bonded High Res. sensor
  - MATRIX **128x32** (2 sub-m. 16x128)
  - SQUARE R.O. core



Update on SVT Background simulation with Bruno

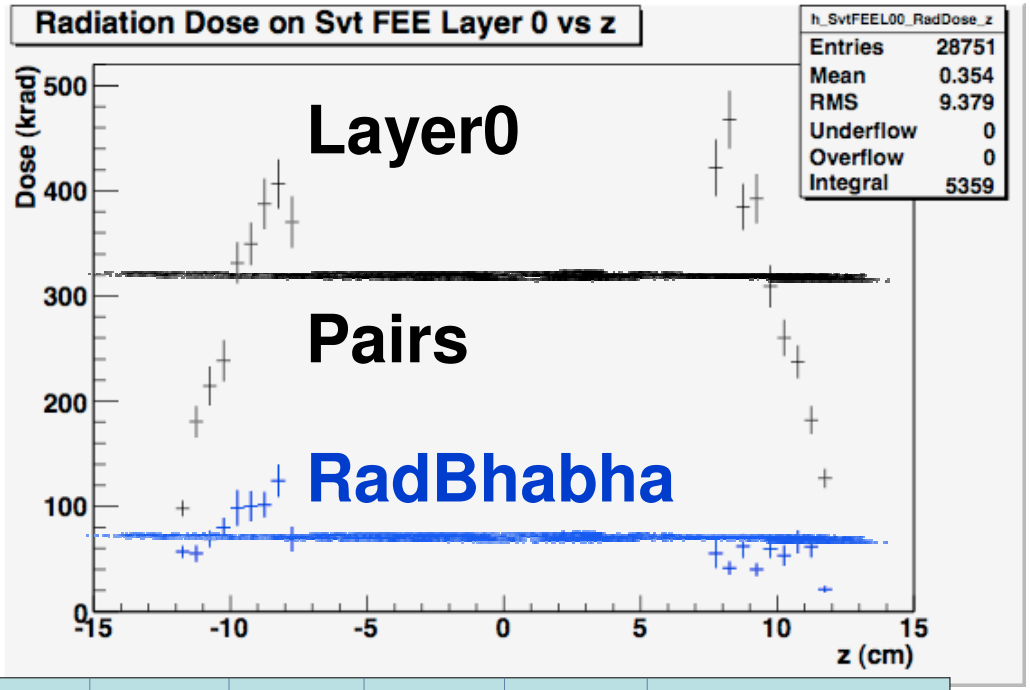
Full simulation: Svt electronics

- Drawing by F. Bosi, realistic HDI for L0 in GDML description, no need to resize container volume
- Full simulation: hits collected also on HDI's for outer layer and dummy volumes on matching cards location
- More detailed description, like pin-wheeled L0 modules, will be added soon



Radiation dose on Svt electronics

- Integrated Dose (1 nominal year)
- Pairs (40k evts) and RadBhabha (10k evts) bkgs, B field ON
- Average dose consistent with previous test
- Touschek still missing
- Phi asymmetries?



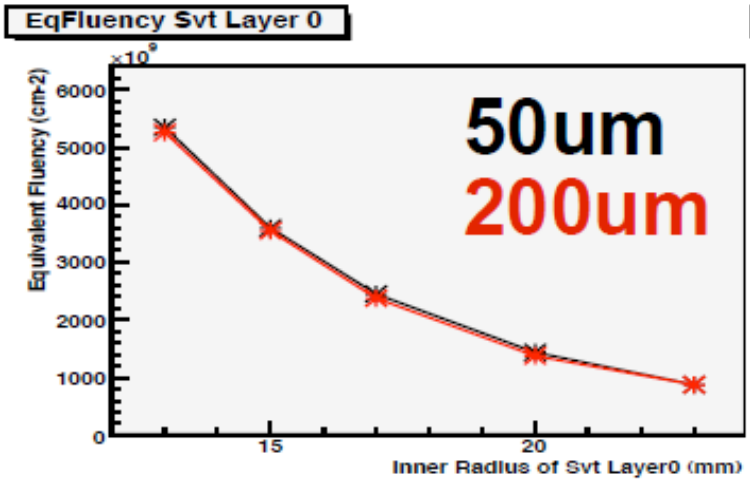
Av. Dose (krad)	L0	L1	L2	L3	L4	L5	MCard
Pairs	**319**	45	44	12	3	2	0.5
RadBhabha	**72**	10	14	6	2	1	1.4

First results on MAPS neutron irradiation

- The lifetime (➔ diffusion length) of minority carriers is reduced by radiation-induced defects. Carriers are trapped by extra recombination centers placed in the substrate before reaching the collecting electrode
- 3 irradiation steps (so far): 2 x 10^{11}, 5 x 10^{11}, 1 x 10^{12} n/cm2
- Our Deep-Nwell MAPS are expected to:
  - suffer a loss in the signal
  - withstand an increase of the dark current (safe up to ~pA, 100 nA/cm2 @ V=300 mV)
  - No change in noise & gain

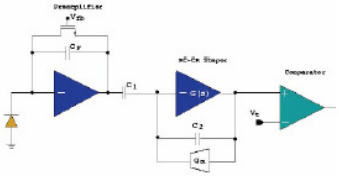
(electronics rad.hard)

Expected equivalent fluence:
ϕ ~ 5 x 10^{12} n/cm2 (1 nominal year)

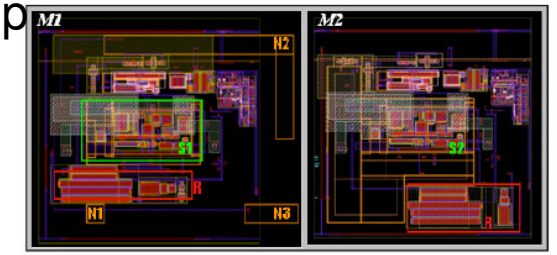


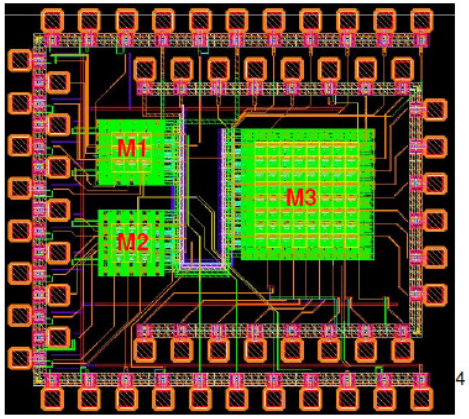
The irradiated chip
Apsel3T1

- Two electrode geometries implemented in the chip apsel3T1:
  - satellite N-wells (matrix M1)
  - T sensor (matrix M2)
- The CR-RC shaper:
  Pulse (t) ~ t exp(-t / τ_{peak})
  with τ_{peak} = 400 ns



- Available the 9 (analog) shaper-outputs of M1/2
- Digital R/O of M3



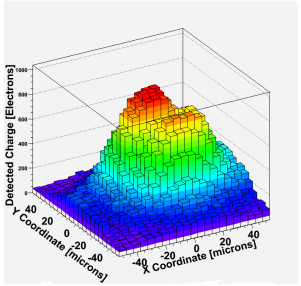


S.B.

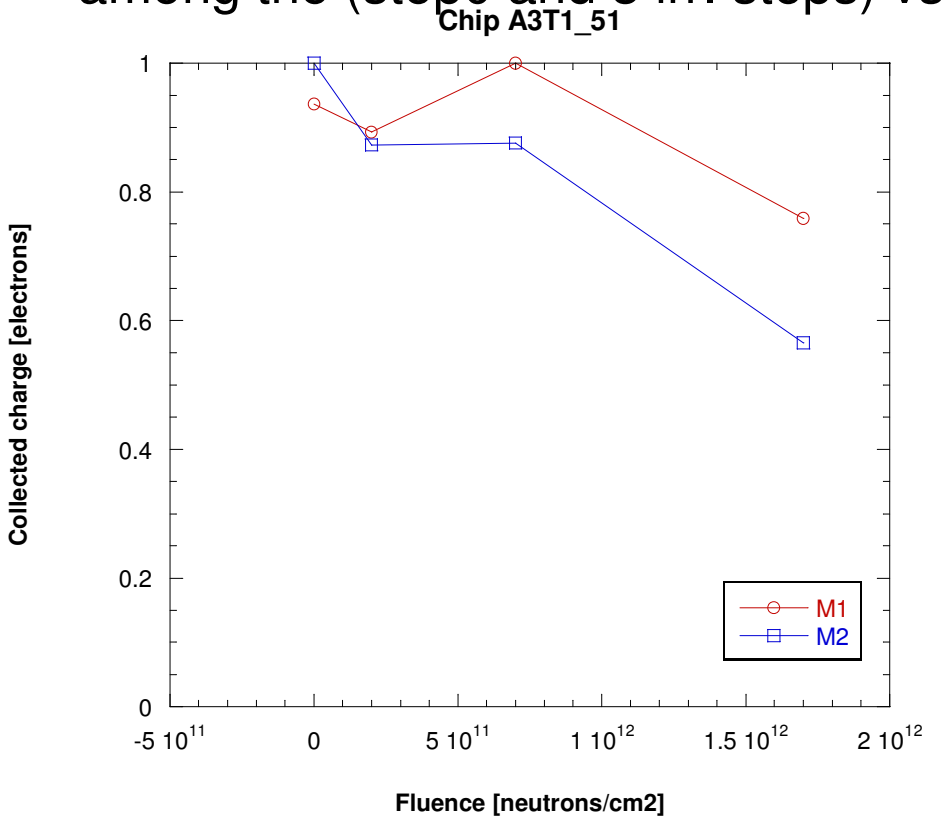
Charge Collection

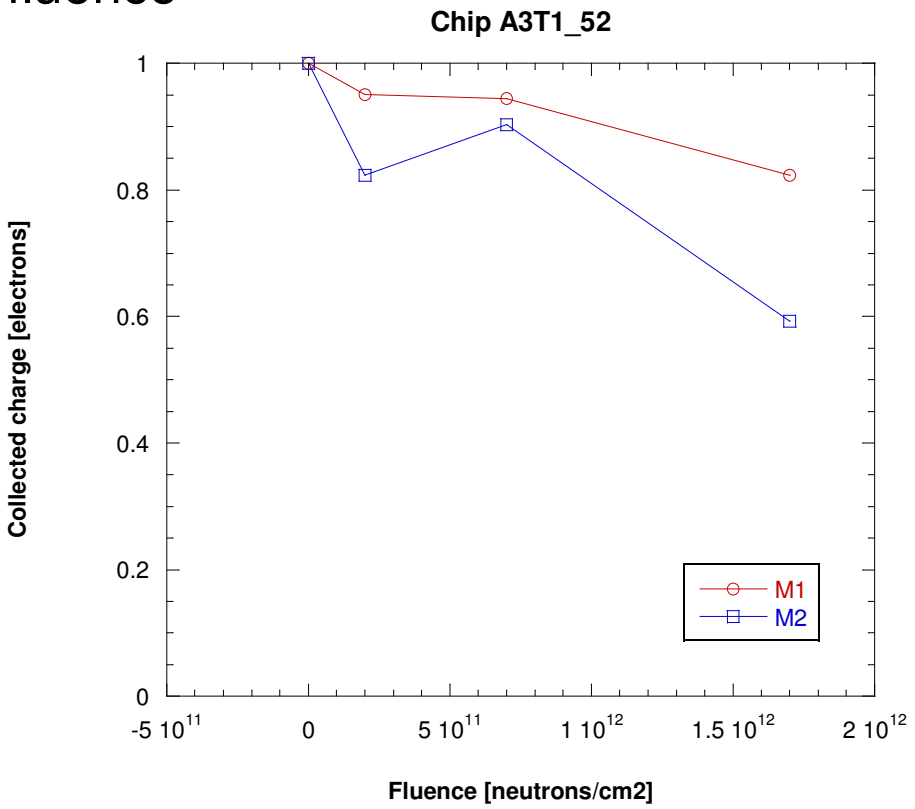
LASER (λ=1060 nm) SCAN

Charge collected by the central pixel varying the position (step=5 um) of the laser spot (σ~20 um)



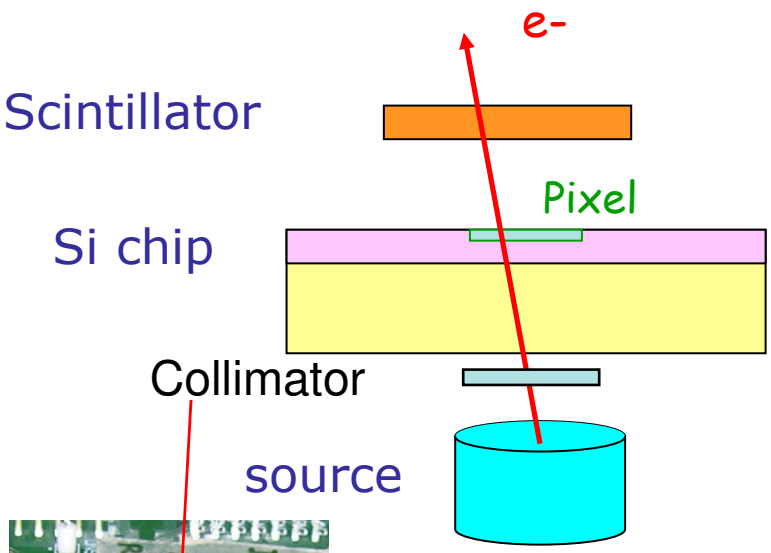
Charge collected normalized to the maximum charge seen by the central pixel among the (step0 and 3 irr. steps) vs fluence

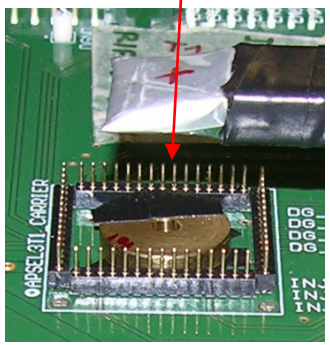




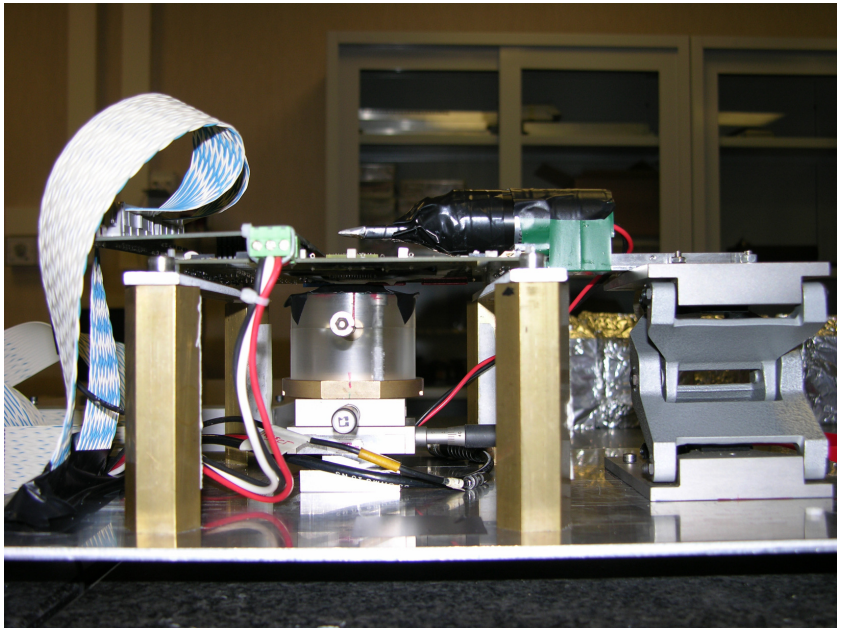
The reduction of the collected charge is larger for M2 (60 %) than for M1 (80 %). This effect may be due to the electrode geometry.

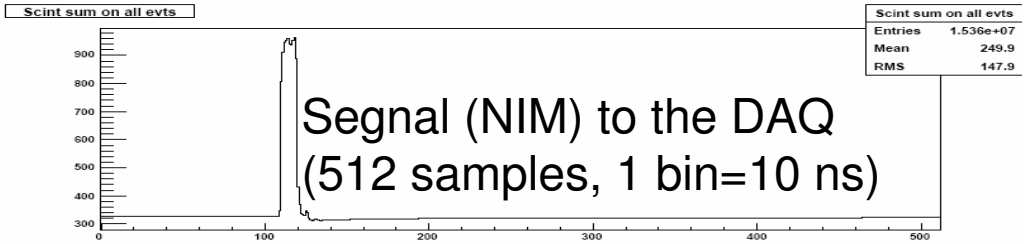
Trigger for β: the scintillator

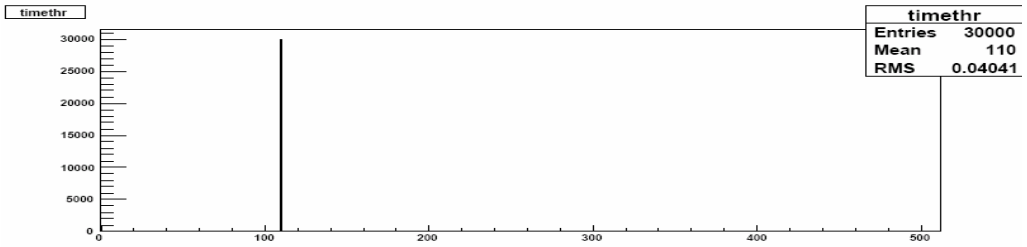




3 mm (diameter)

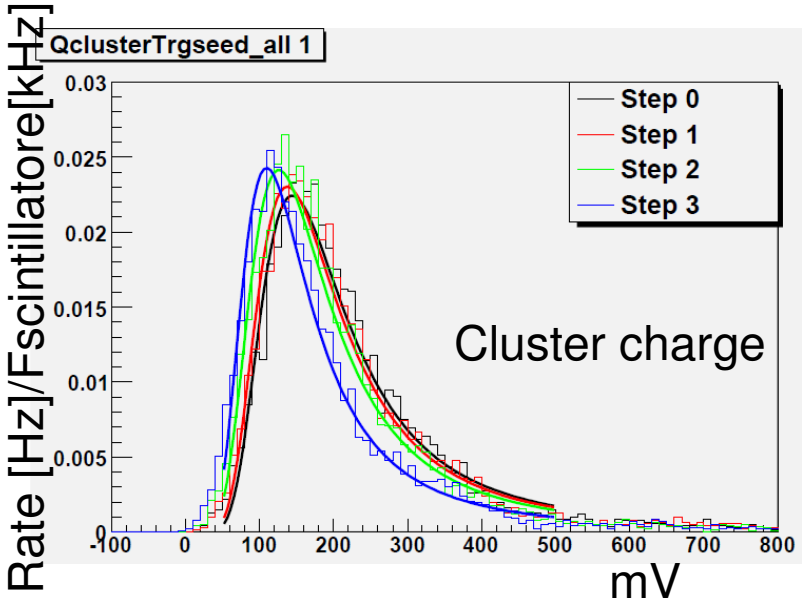


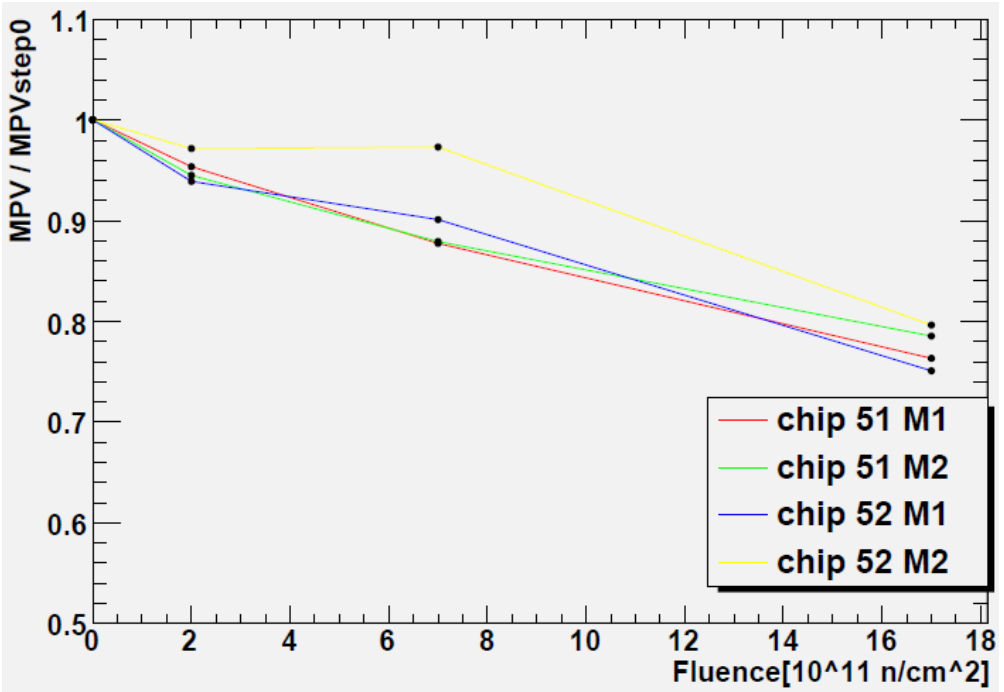


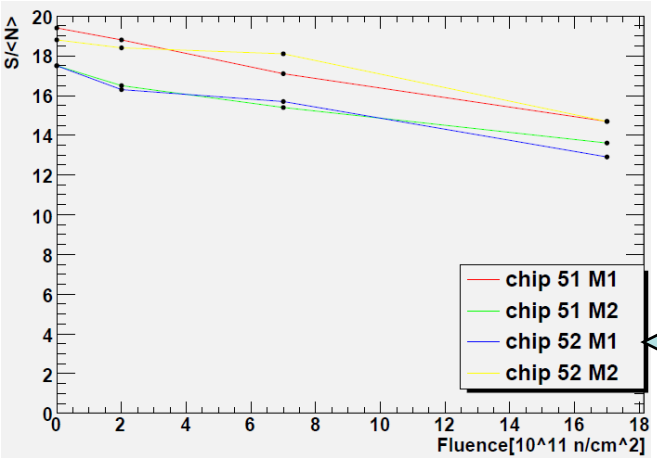


The pulse of the scintillator opens a 500 ns-wide window and if the central pixel has a signal greater than 4σ the trigger fires: waveform records from 1.1 us before to 4 us after the scintillator (i.e. the arrival of the electron).
The values of the analog signals are taken as the maxima at T_{peak} = 400 ns.

Results from β spectra







- The MPVs of the Landau curves undergo a 20% reduction.
- S/N decreases.

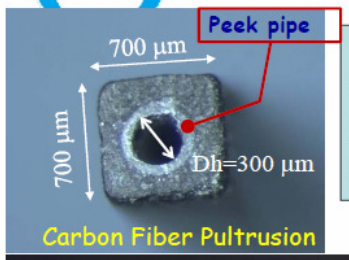
Next irr. step: +(5 x 10^{12} n/cm^2)

Layer0 support & SVT Mechanics

Design of Layer 0 modules (striplets and pixel) & beam pipe well advanced

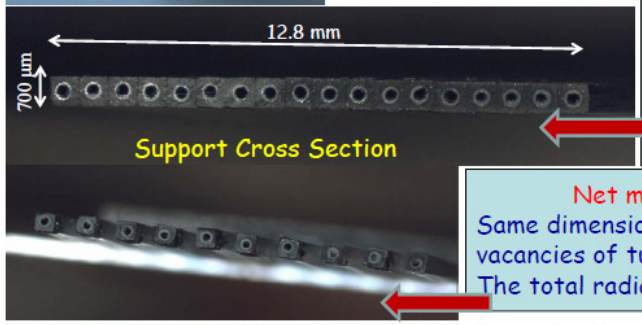
F.Bosi

Module supports summary



The single base microchannel unit

A square CF micro-tube with an internal peek tube 50 µm thick used to avoid moisture on carbon fiber



Full micro-channel module

The total radiation length (*) of this support is 0.28 %X_0

Net micro-channel module

Same dimensions of full micro-channel but vacancies of tubes in the structure.

The total radiation length (*) is 0.15 %X_0

(*): Material of the support structure: (All C.F. material + peek tube + Water)

Results:

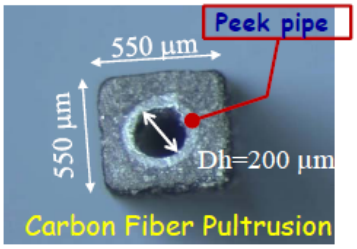
Temperature along the module: ΔT = 5,3 °C at 2W/cm² and Δp =3,6 atm

Temperature along the module: (ΔT = 7.7 °C at 1.5W/cm², Δp =3,5 atm)

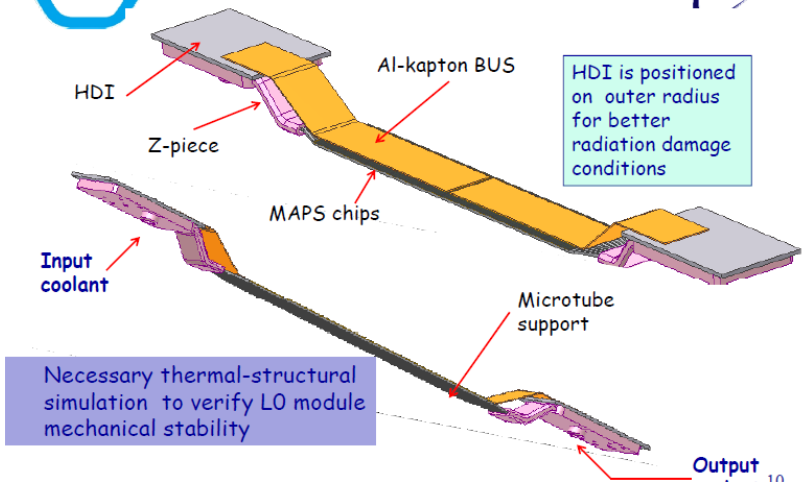
Further reduction in X_0 possible with optimization:

3) Development of microchannel base structure with L=550 µm and Dh=200 µm

In construction phase, first prototype, ready in 5 weeks (further reduction of X_0)



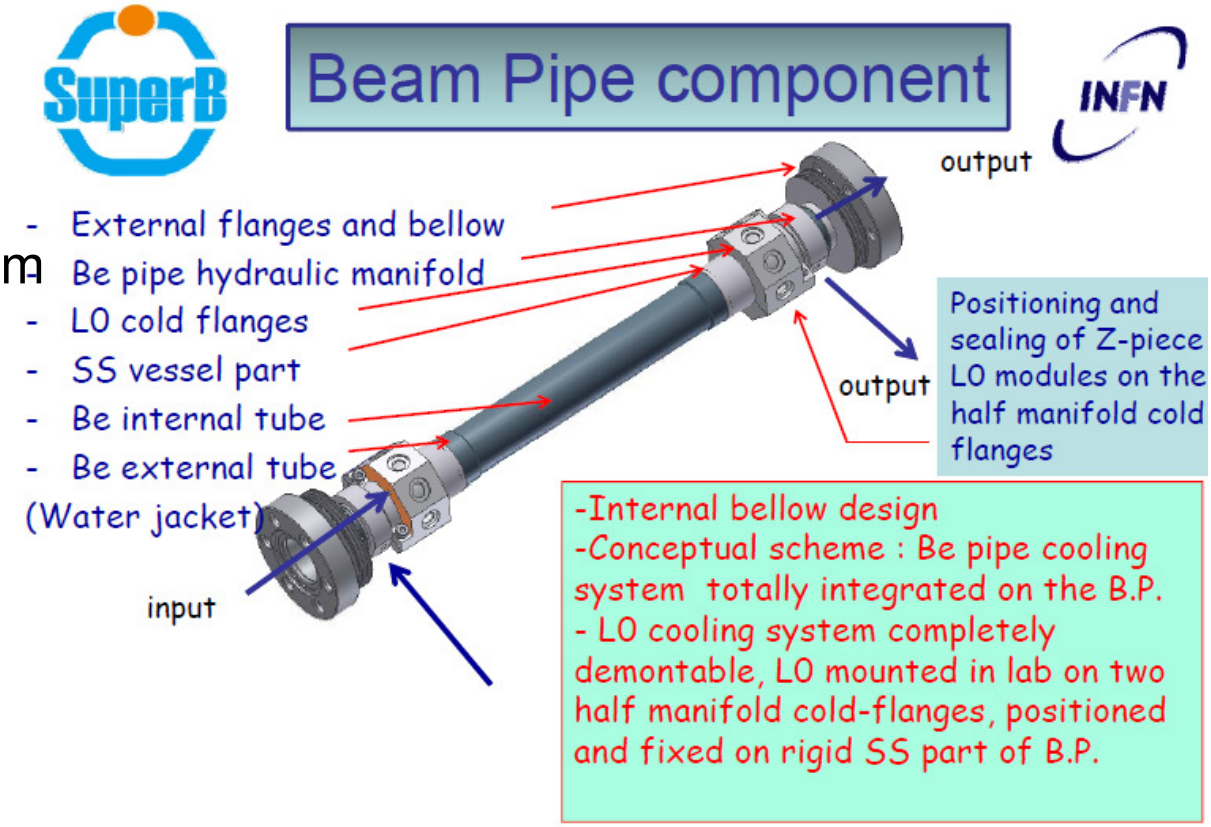
MAPS L0 module Design

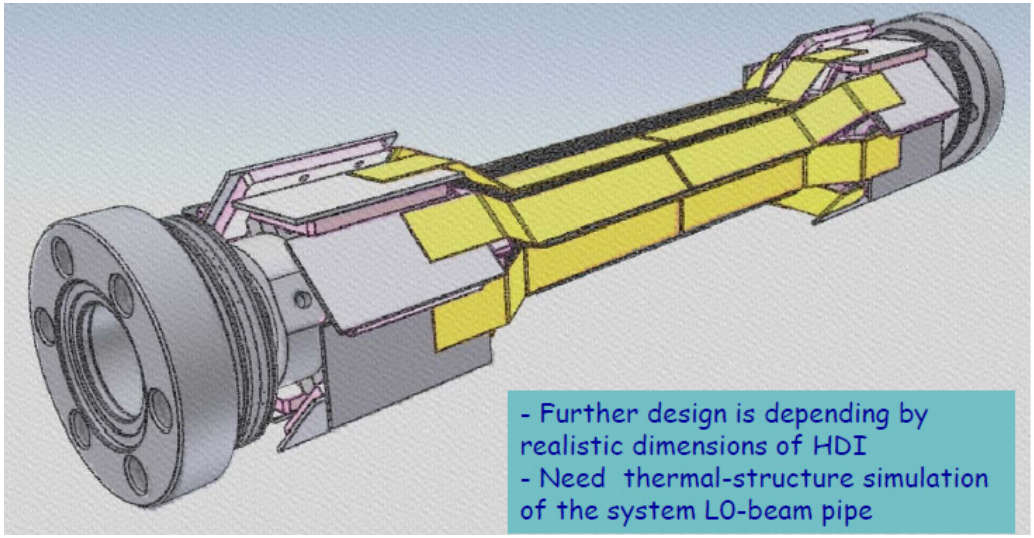


Necessary thermal-structural simulation to verify L0 module mechanical stability

Goal:

construct a full scale
L0 + Al beam-pipe system
to perform thermal tests
at the TFD lab.





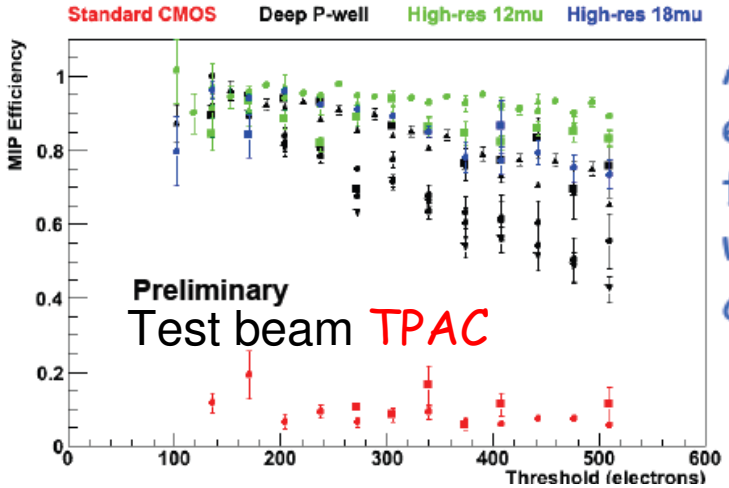
The reduction of Be beam pipe length is possible to match the request of 240 mm

Need adding work and effort to design quick demounting in the SuperB experiments

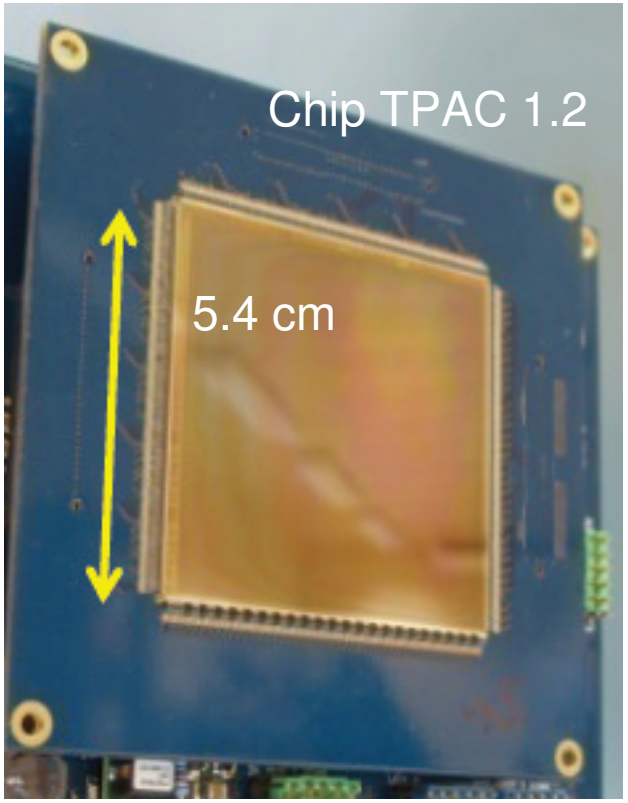
UK Activities

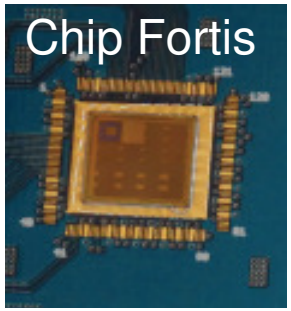
A. Bevan, M.Stanitzki, F.Wilson, S Coquereau,
J. Mistry, F. Gannaway
Plus working groups from SPiDer Collaboration and ATLAS upgrades

- Silicon
  - TPAC/Fortis/Cherwell Chips

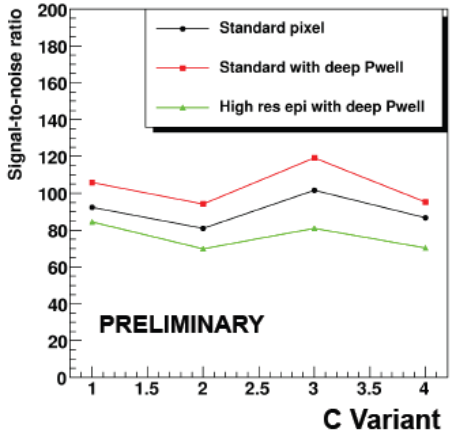


Adding high-resistivity epitaxial layer makes further improvement with resulting efficiency close to 100%



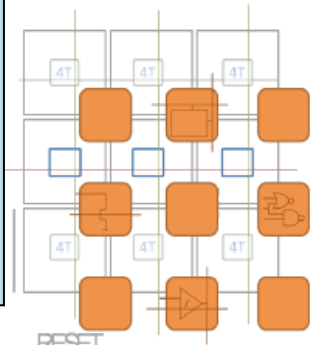


- Simple r.o. arch.
- Analog. output



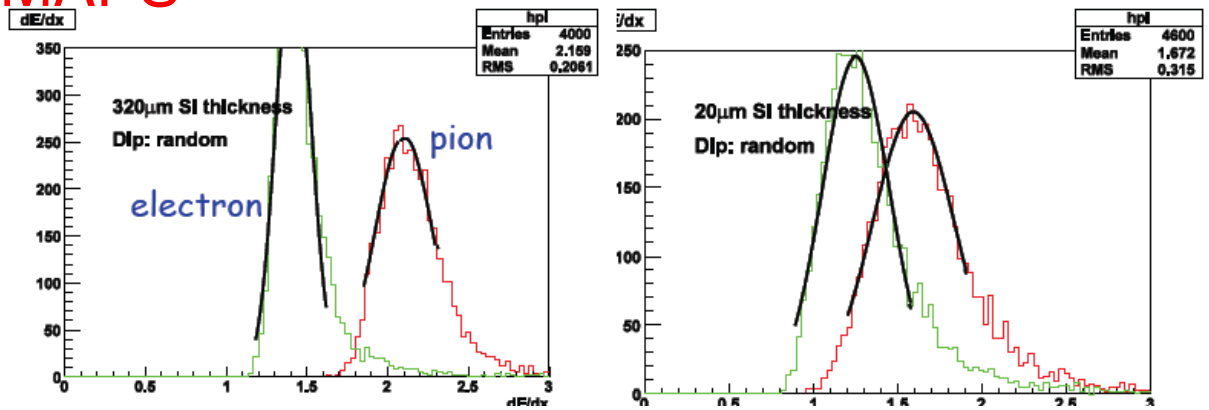
Irradiation campain
(X and Test-Beam) in progress
to asses the
Radiation hardness
of the 3 chips.
Results expected at the
next coll. meeting

Chip Cherwell
- INMAPS
- HiRes.
- 4T



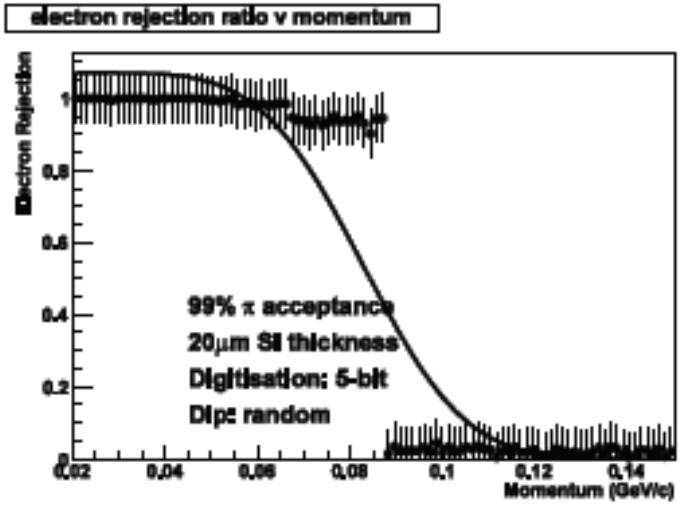
GEANT simulation of INMAPS

- dE/dx
  - Comparison 20μm v 320μm
  - digitisation
  - electron v pi



20μm Si has 80% worse dE/dx resolution compared to 320μm

Identify momentum threshold that achieves 99% pion acceptance

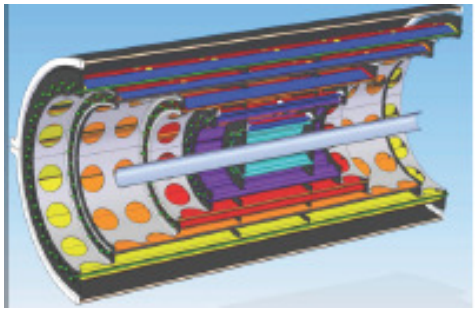


20 μm Si: momentum Cut-off 80 MeV/c with 5-bits in the dE/dx ADC

- Lampshade v. Long-barrel
  - Multiple scattering

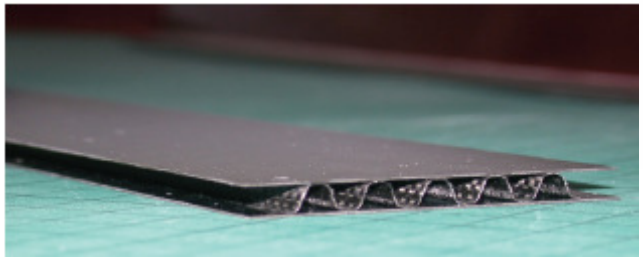
$\tau \rightarrow \mu\mu\mu$

FastSim simulation



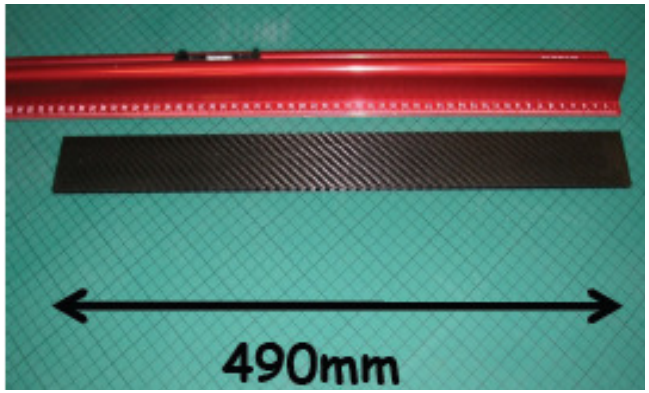
Efficiency: **No degradation due to high dip tracks seeing extra material in Long Barrel model**

- Support Structures
  - Improving initial ideas



Proposed
Staggered-lampshade

- Construction of 1st prototype
  - 1 ply Carbon Fibre (CFRP) weave + 1 ply corrugated + epoxy glue
  - Roughly 0.8% radiation length
  - Thickness 5.2 mm, length 490mm, width 50mm



Future Plans

- Characterize chip performance
  - Radiation hardness
  - Test beam and X-rays
  - Readout, noise etc...

Continue to develop carbon-fibre support ideas
- Improve flatness
- Continue to reduce material
- Introduce cooling pipes/CFRP
- FEA simulation
- Test thermal conductivity

Move to more physics-based studies using FastSim.

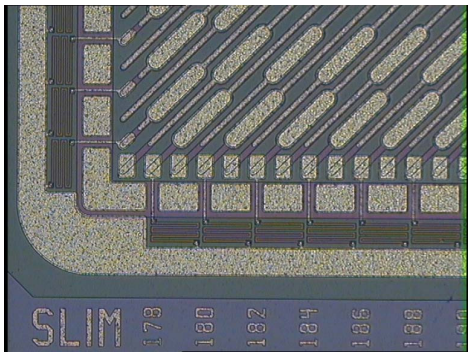
UK Comprehensive Spending Review (CSR) due in October: 25%-40% cuts in government spending.

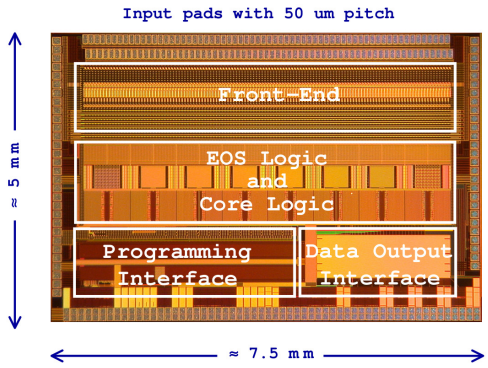
Update on Trieste Activities

Group is involved in strip(let) detectors DAQ, ROC &dE/dx, irradiations studies

News since Elba meeting:

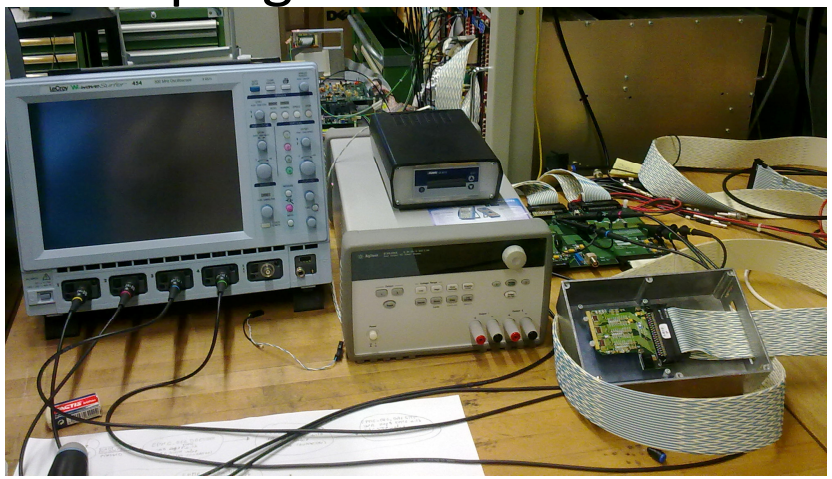
- New standalone FSSR2 DAQ is working (for lab use, replaces Pomone)
- Telescope spares construction ongoing.
- Ongoing discussions on FSSR2 alternatives.
- Starting studies (particle ID with SVT dE/dx)





New DAQ chain for FSSR2

- New DAQ developed based on V1795 CAEN board hosting 2 FPGAs, intermediate custom board, 2 (3+3)-FSSR2 hybrids, with a (reduced version) of SLIM5 FW.
- Chips are programmed and data is read through VME-USB bridge and a Labview based acquisition program.
  - Write and read back all registers
  - Correct initializations procedures
  - Able to acquire data
  - and to perform calibrations



- Some limitations due to small RAM (extend!)
- Not all functionalities still available

REVIEW TALK

SuperB factory Workshop — Frascati, Septembre 2010

Highly Pixelated Transparent Devices for Future Vertex Detectors

Marc Winter (IPHC-Strasbourg)

(on behalf of the MIMOSA, PLUME, Hadron Physics 2 & AIDA collaborations)

▷ more information on IPHC Web site: http://www.iphc.cnrs.fr/-CMOS-ILC-.html

CONTENTS

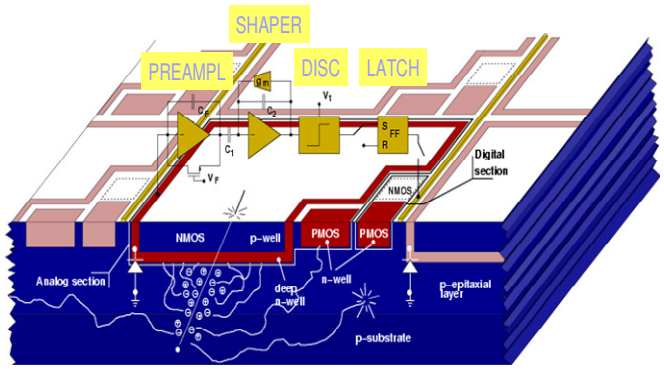
- **CMOS pixel sensors developed by IPHC-IRFU :** achievements & current applications
- **On-going R&D:** directions, goals, timelines, ...
- **Synergies with SuperB vertex detector issues**
- **Summary – Conclusions**

The R&D on DNW MAPS

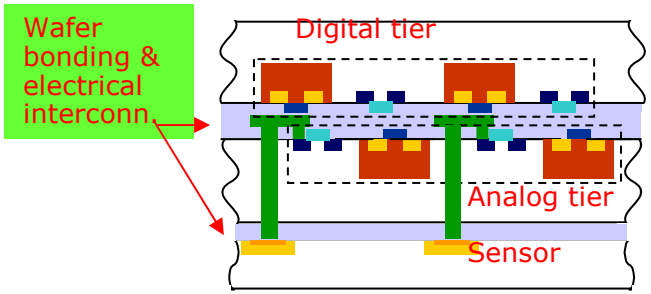
V.Re

2D MAPS and 3D pixels are the two most advanced options for a Layer0 upgrade:

- CMOS MAPS option:
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-INFN Collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams.

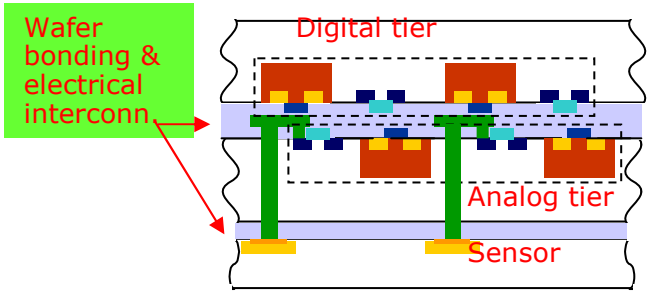


- Thin pixels with 3D Vertical Integration: **reduction of material and improved performance**
  - Two options are being pursued (VIPIX – INFN Collab.)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



The second 3D-IC run: VIPIX plans and designs
(Tezzaron/Chartered process)

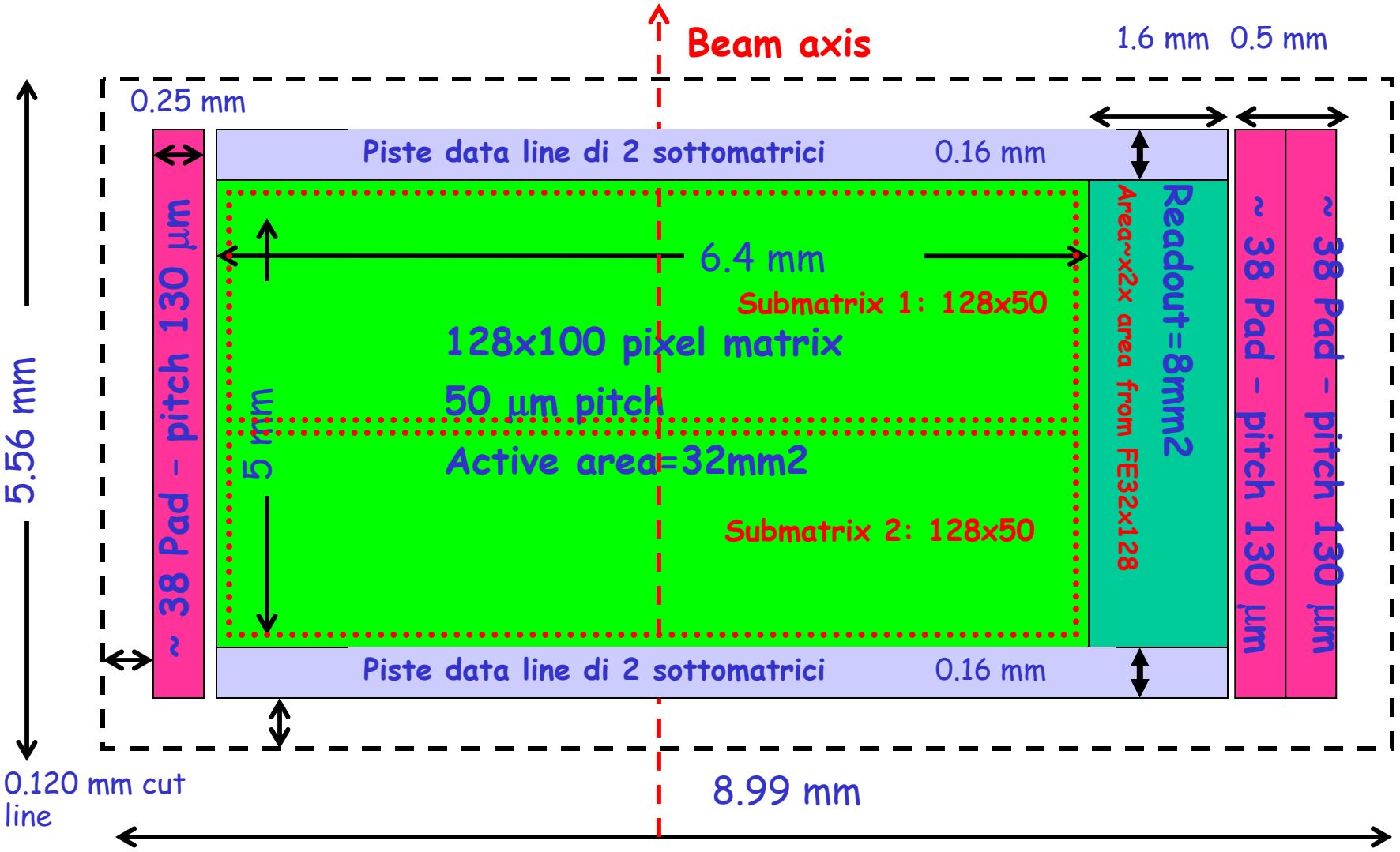
New VIPIX designs will cover an area of about 150 mm^2 of 3D stacked chips (300 mm^2 in terms of planar silicon). Submission deadline will be 1Q2011, to allow enough time for testing devices from the first run.



The following devices will be included by VIPIX in the second run, targeting SuperB SVT specifications:

- **"test beam grade" MAPS** : 100x128, 50 um pitch (~32 mm^2 active area) with high rate sparsified readout architecture
- **a 3D readout chip for high resistivity pixel sensors** (similar architecture) : 128x32, 50 um pitch (~10.3 mm^2 active area)

Vertically integrated MAPS in the second 3D-IC run: APSEL



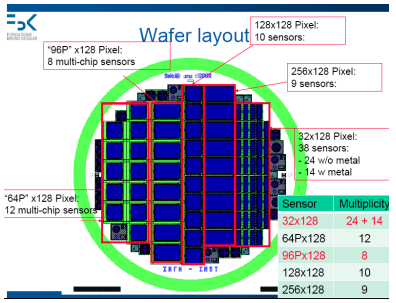
High resistivity pixels

- **Pixel sensors on high resistivity substrate (compared to MAPS) give much better radiation hardness, signal-to-noise ratio,…**

- Sensors are fabricated by FBK-IRST, following the specifications of the interconnection process
- A prototype pixel sensor matrix is ready and characterized

  N-on-N: P-spray isolation on n-side, p implant on the back side

  Wafer thickness: 200 μm (FZ, HR Si); 50x50 μm pitch.



Sensor	Multiplicity
32x128	24 + 14
64Px128	12
96Px128	8
128x128	10
256x128	9

Two alternatives for the interconnection process:

- Bump bonding with the IZM Berlin process

  → First test of the process with 2D 130 nm chip prototypes under way

- Vertical integration with T-Micro/Zycube (Japan): might offer lower cost and more flexibility with respect to Ziptronix

Why a 65 nm APSEL ?

- The demand for higher in-pixel functionalities along with the reduction of pixel cell size drives the interest of the designers community towards **sub-100 nm CMOS** processes in the design of mixed signal front-end electronics
- The properties of **Low-Power 65 nm CMOS:**
  - **Noise parameters appear stable**

    wrt previous CMOS generations
  - The comparison with data from previous

    CMOS generations confirms the

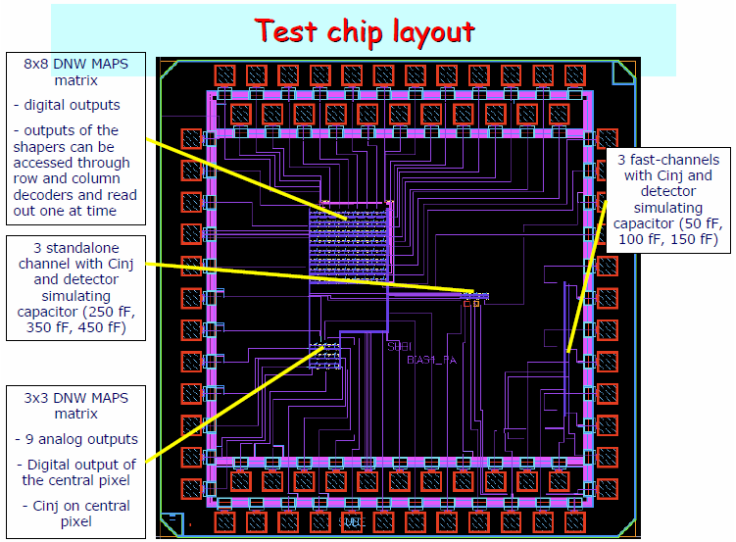
    high degree of tolerance to ionizing

    radiation typical of sub-100 nm technologies
  - **Submitted a prototype chip with**

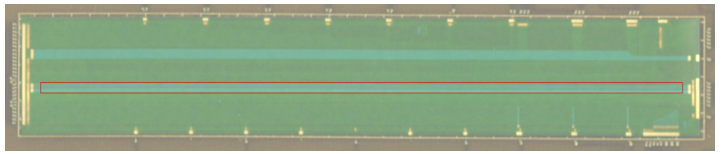
    mixed-signal readout circuits in

    a 65 nm CMOS process by

    IBM (10LPE/10RFE) → APSEL65

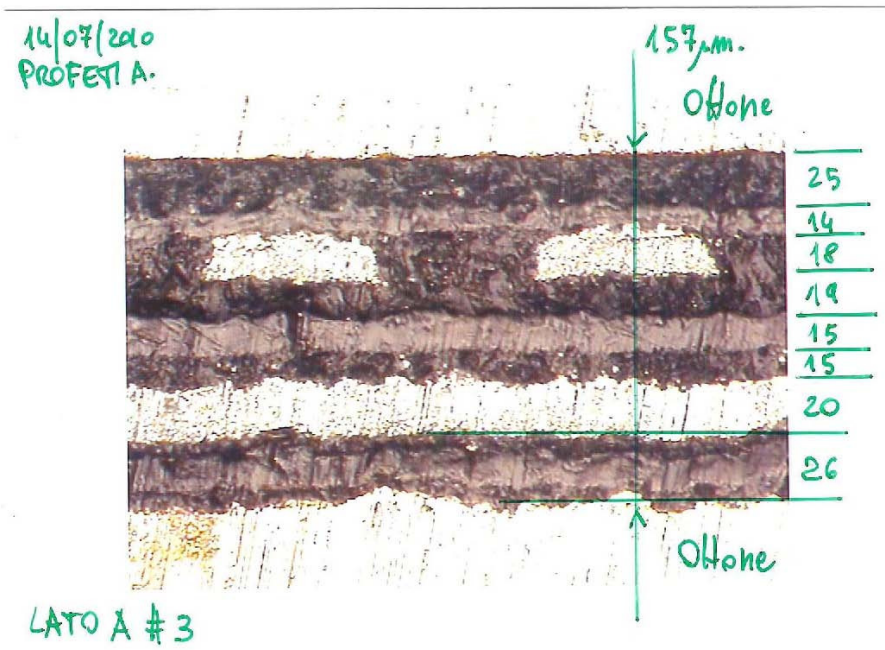


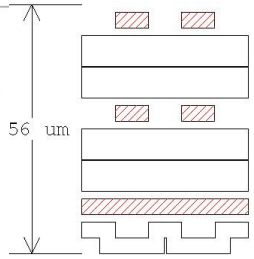
Update on pixel bus



Number of layers: 8
Total thickness = 156 um

Analysis of the stack-up (prototype)



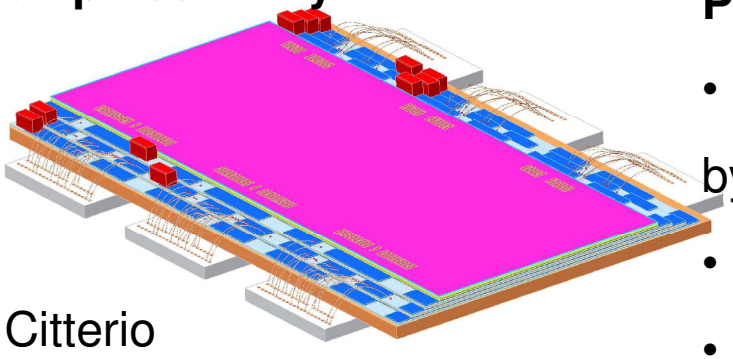


NN	Layer Name	Type	Usage	Thickness um
1	TOP-LAYER	Metal	Signal	13
2	Polyimide	Dielectric	Substrate	15
3	Glue	Dielectric	Substrate	5
4	INNER-LAYER	Metal	Signal	13
5	Polyimide	Dielectric	Substrate	40
6	Glue	Dielectric	Substrate	5
7	GROUND-PLANE	Metal	Plane	50
8	Polyimide	Dielectric	Solder Mask	15

Lessons learned:

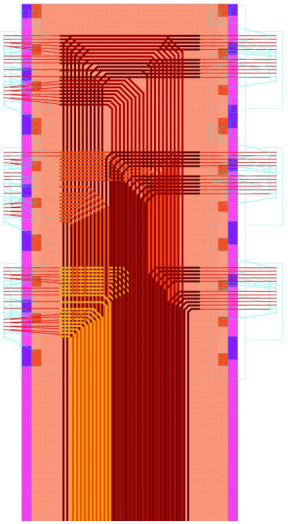
- Layer thickness must be carefully measured during stack-up
- Good practice: measure thickness at each step in production
- The kapton layer is always the same
- Aluminum signal lines slightly thicker than expected
- Trace widht ~ 75 um, some “undercut” due to etching. Trace width could be not uniform → impedance variation
- Not yet understood the extra crosstalk

The new bus for a 3-chip assembly



Production schedule:

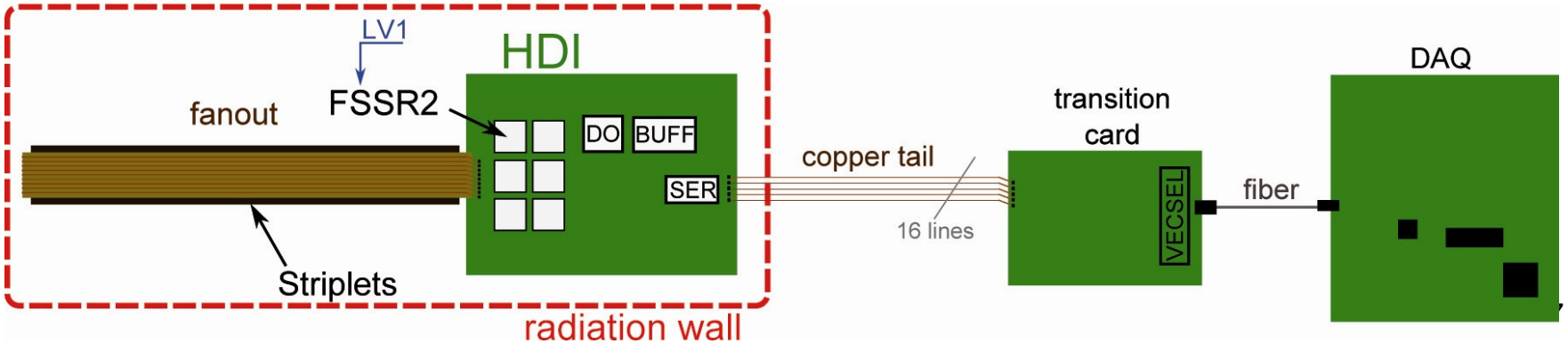
- Simulation of new layout completed by mid October
- Bonding layout should be reviewed
- BUS delivered after 6 months



M.Citterio

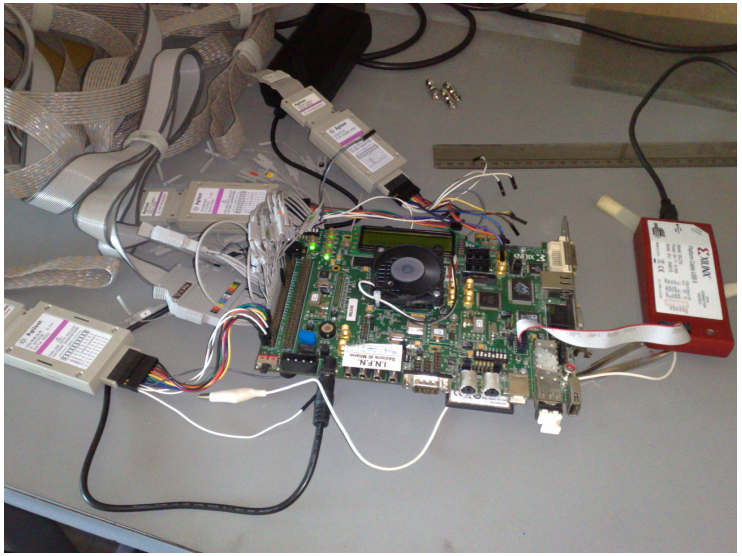
HDI, transition card development

- Transfer data from **layer0** front-end electronics to DAQ
  - to collect data and program FSSR2 (baseline) or MAPS (upgrade)
  - to store data for 20 µs by means of buffers (hypothesis)
  - to increase robustness using ECC codes and radiation hardening by design ASICs
  - to transfer data at high frequencies (up to 5 Gbps)
  - to re-use similar approach for others layers (with less contraints)



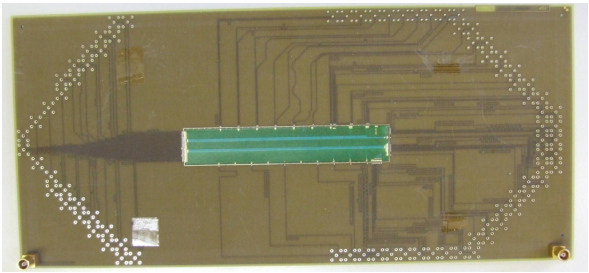
HDI prototype

- Developed a first prototype using a Virtex 5 FPGA, containing:
  - Differential receivers
  - De-serializer
  - Data organizer
- Extensive tests demonstrate that prototype works as expected



NEXT STEPS:

- Study data transmission using the prototype BUS for signal integrity measurements and simulation comparison



- Rad hard Serializer (LOC) 16:1, 5 GBps
  - Dallas chip expected in the coming weeks
  - LOC will be used instead of FPGA rocketIO

Conclusions

- The technologically mature SVT design as baseline for the TDR: L0 striplet + L1→5 Strip module

- A lot of activities are ongoing on all the items:
  - R&D on pixel solutions more robust against background and useful in a Layer0 of a 2nd generation
  - BKG simulation → r.o. architecture improvements
  - Test on Rad. Hardness
  - Mechanics & integration
  - R&D on pixel in vertical and 65 nm technologies
  - Pixel bus and HDI

- The SVT group is heavily working toward the TDR