UK Activities

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Plus working groups from SPiDer Collaboration and ATLAS upgrades

QMUL, RAL, Paris Sud 11

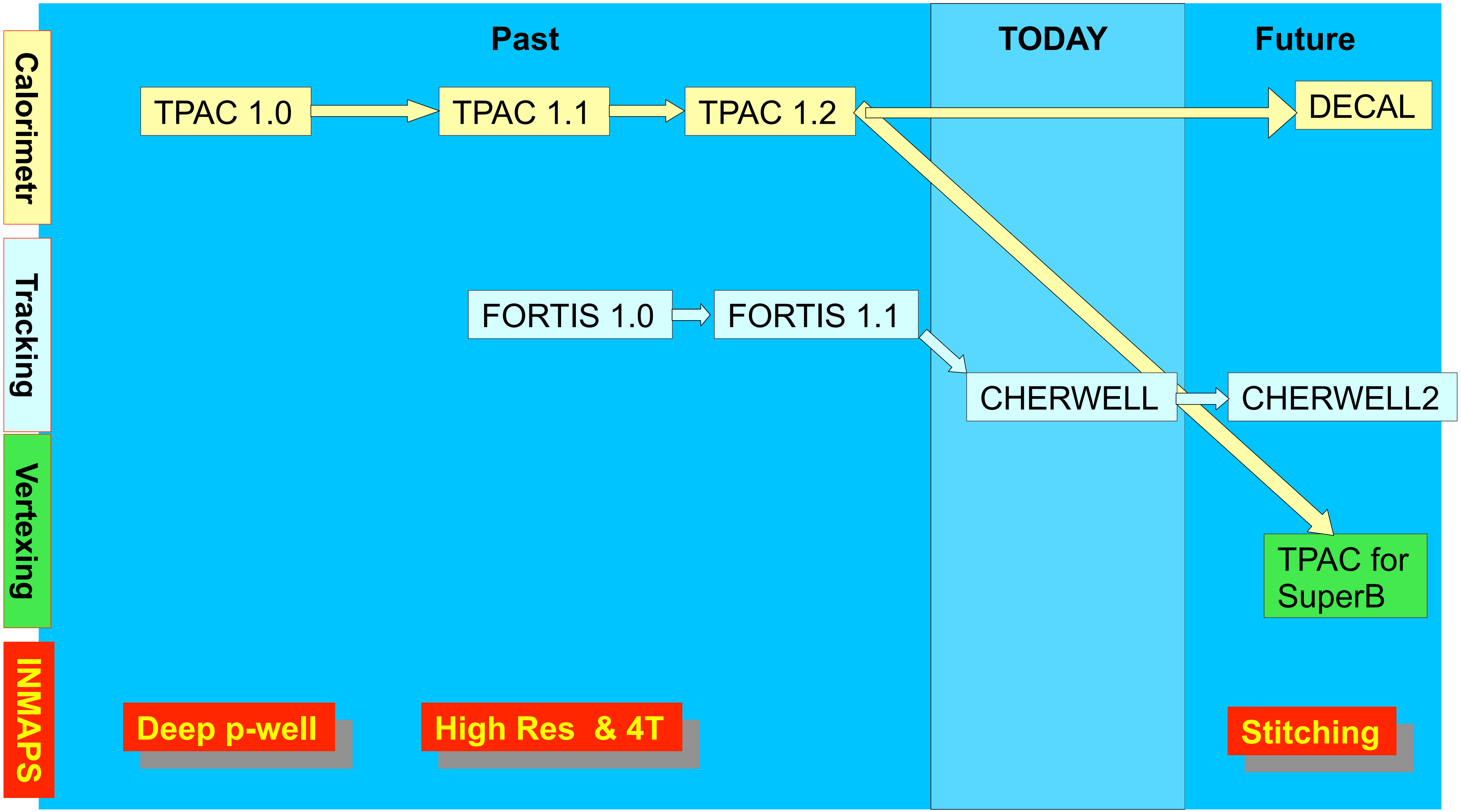
UK Activities

- Silicon
  - TPAC/Fortis/Cherwell Chips
- dE/dx
  - Comparison 20μm v 320μm
  - digitisation
  - electron v pi
- Lampshade v. Long-barrel
  - Multiple scattering
- Support Structures
  - Improving initial ideas

Most of this work has been done as part of other collaborations e.g.

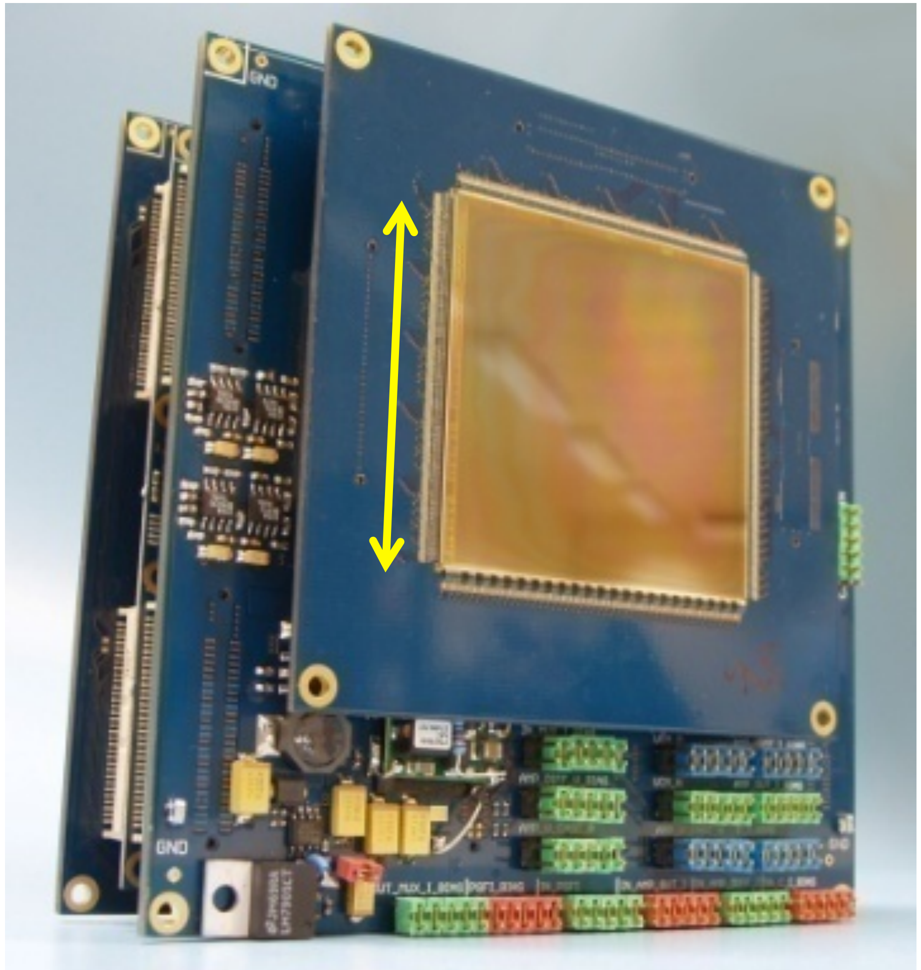
SPiDer and ATLAS upgrades

Sensor Overview



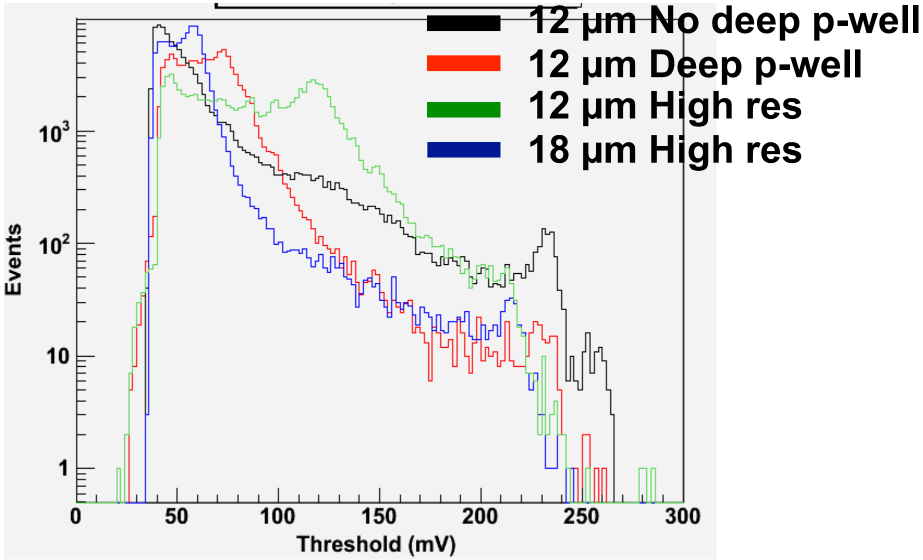
Stitched Sensors

- Standard CMOS limited to ~ 2.5 x 2.5 cm^2
- Technique relatively new to CMOS
  - Stitching offered by some foundries
  - Allows wafer-scale sensors
- Example Sensor
  - LAS (For imaging)
  - Designed at RAL
  - 5.4x5.4 cm^2

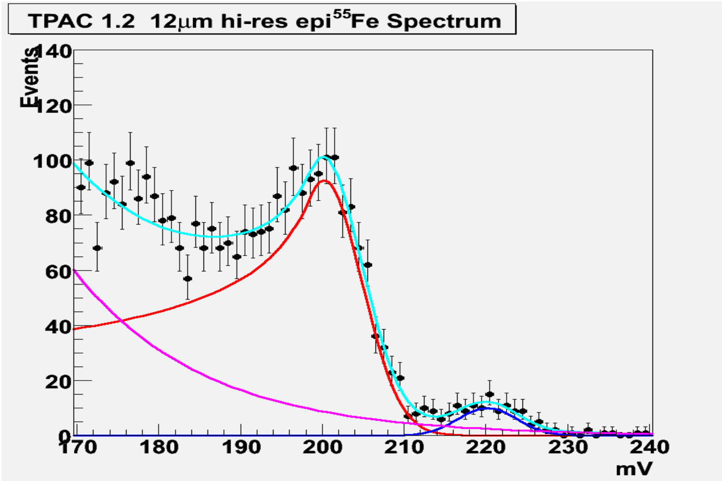


^{55}Fe Spectrum with TPAC 1.2

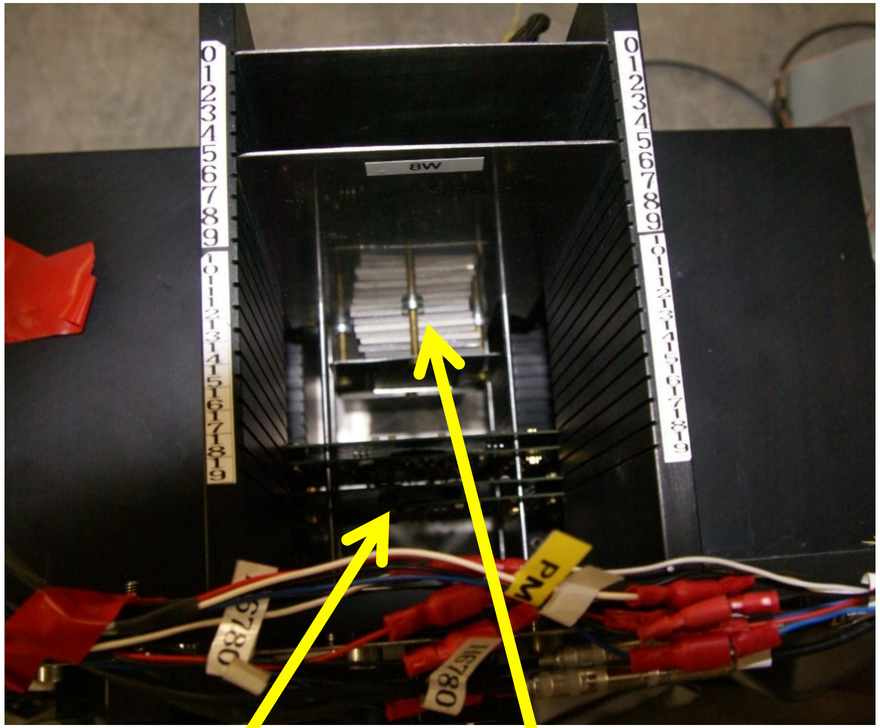
- Using test-pixels with analog out
- Powerful ^{55}Fe source
- Take 100k samples per sensor

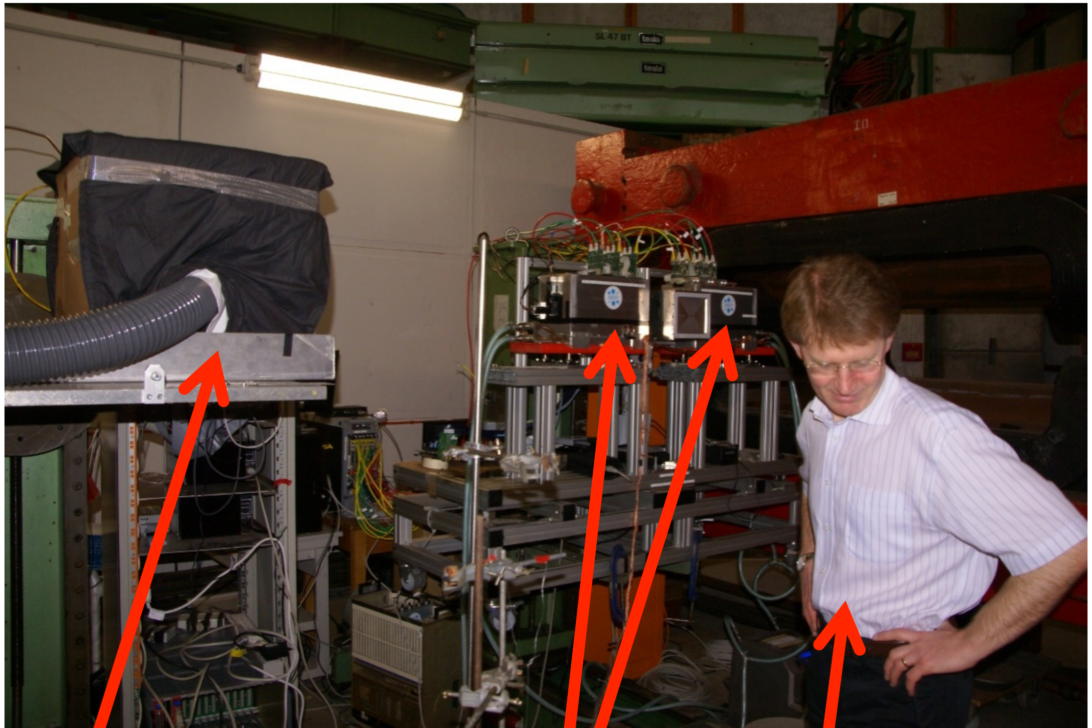


- ^{55}Fe source
  - Deep p-well
  - High -res
- Separation of K_α and K_β
- Hi-res sensor works



TPAC 1.2 Testbeam at DESY





4 TPAC sensors

Tungsten slab

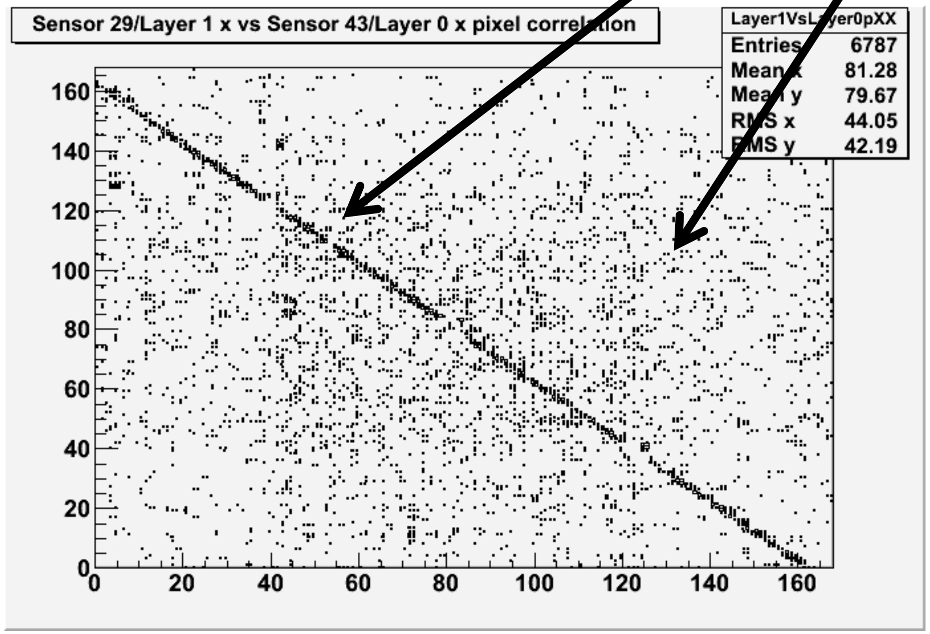
TPAC stack

EUDET Telescope

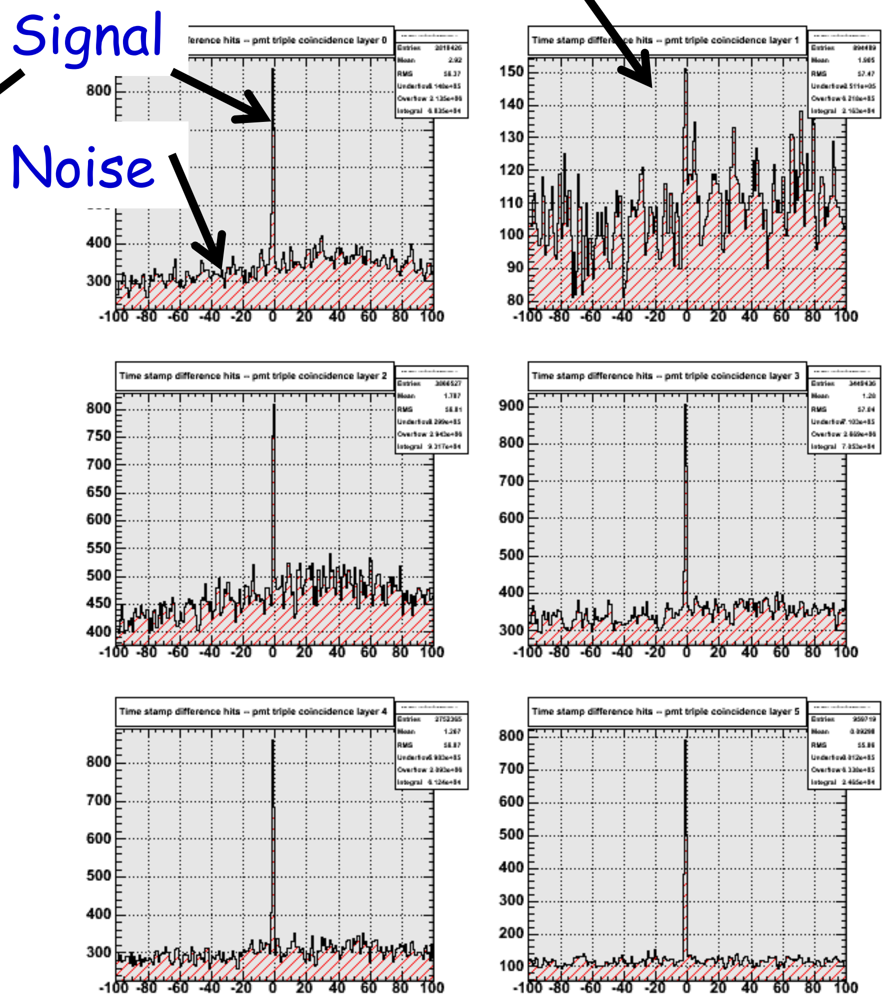
Nigel

TPAC 1.2 Testbeam

- Online plots
- 6 sensors (1 non deep p-well)



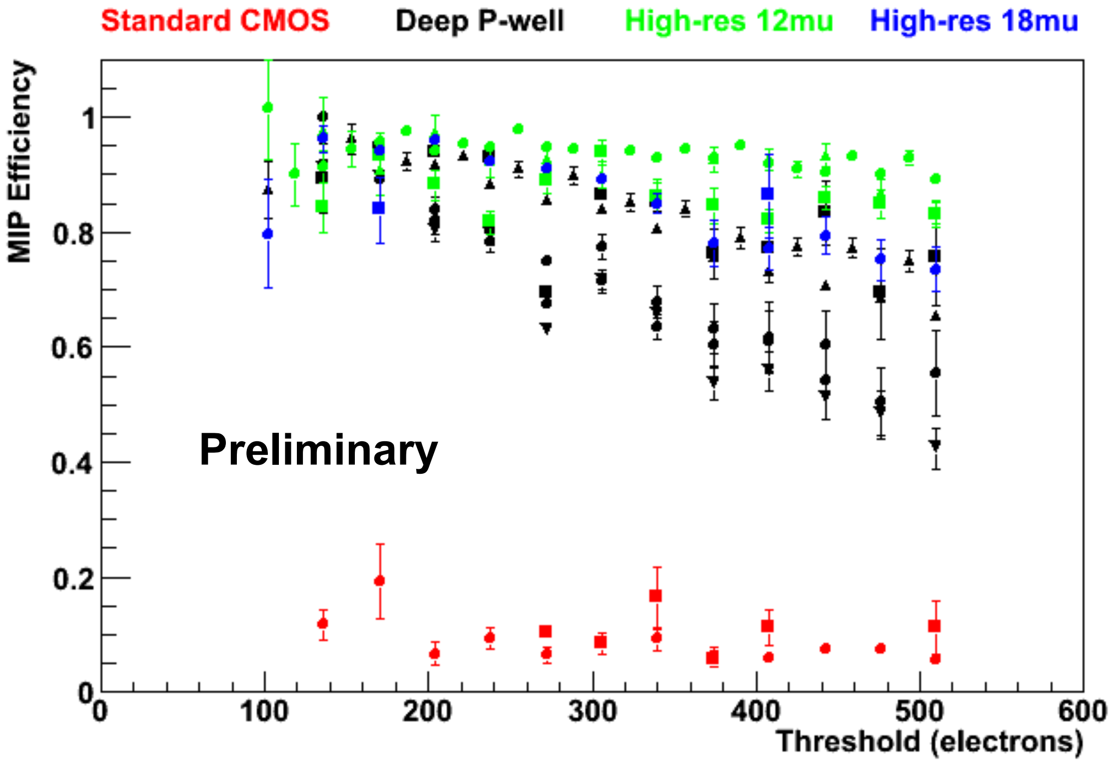
X-X correlation plot for two layers (back-to-back)



Hits in time with Scintillator hits

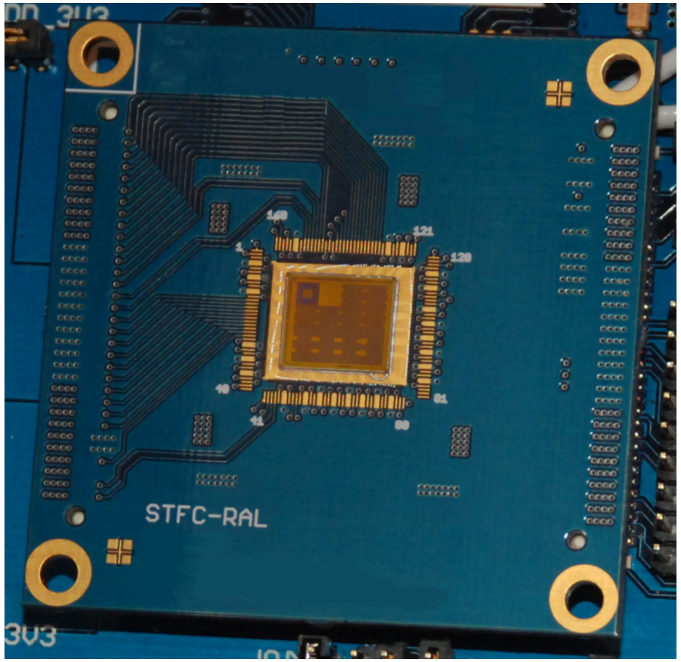
TPAC Testbeam Results

- No absorbers
- Due to use of in-pixel PMOS transistors, standard CMOS sensors have low efficiency
- Deep P-well shields N-wells and raises efficiency by factor ~5
- Adding high-resistivity epitaxial layer makes further improvement with resulting efficiency close to 100%



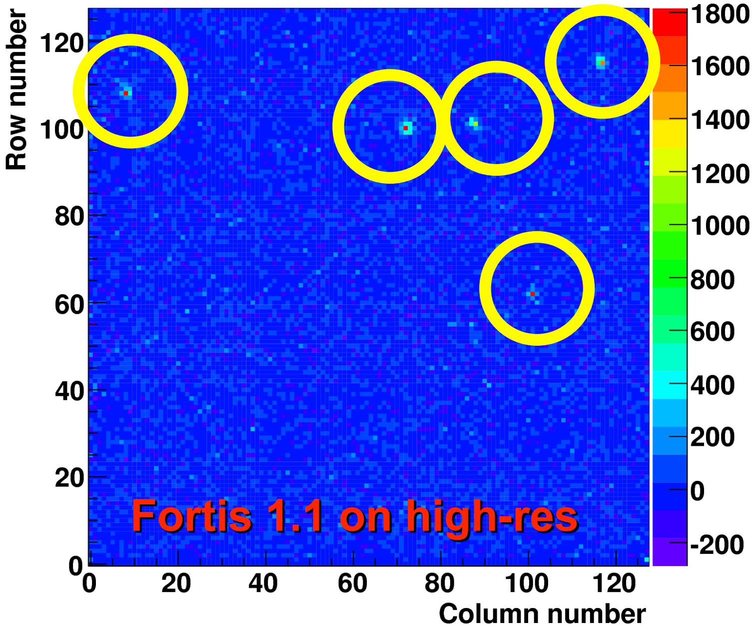
2) Fortis

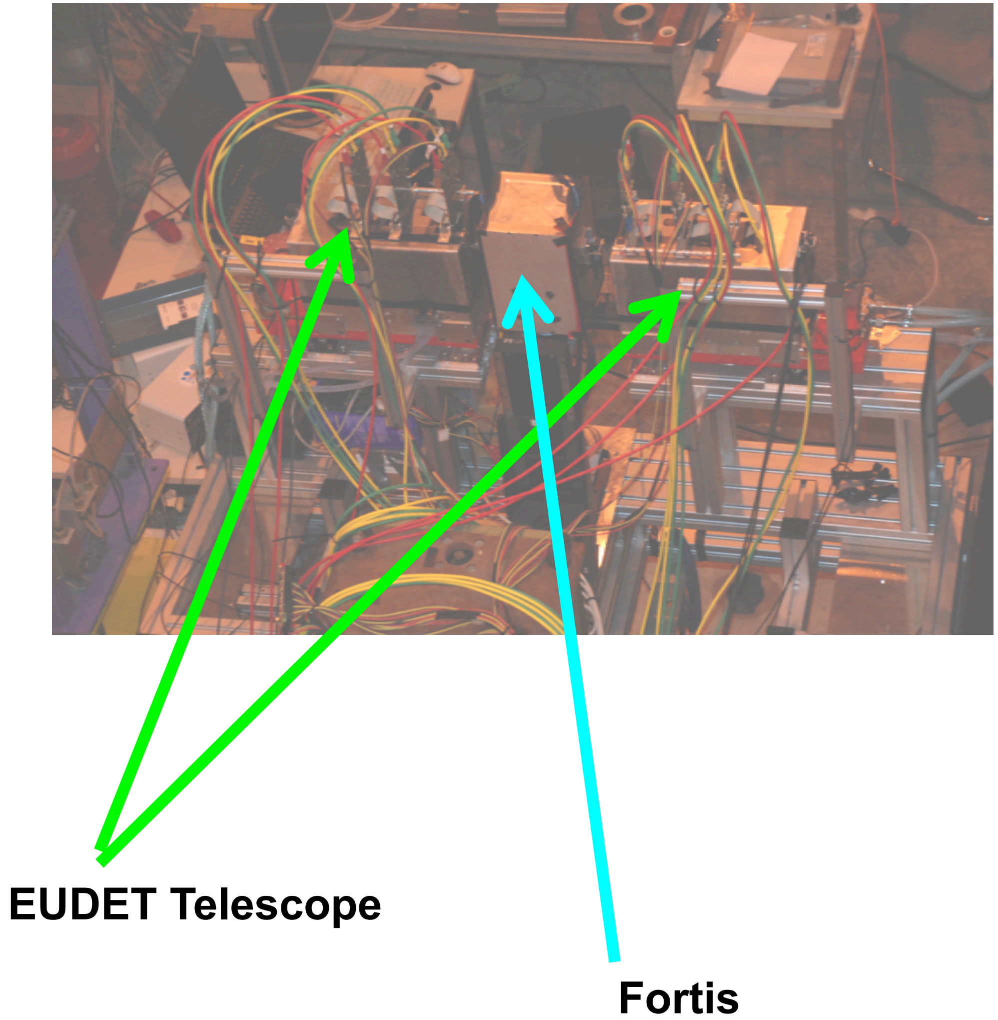
- Test sensor to evaluate 4T for tracking/vertexing
  - Simple readout architecture
  - Analog output
- 12/13 variants of pixels for Fortis 1.0/1.1
  - Size of source follower
  - size of the collecting diode
  - Pitch (6- 45 μm)
  - Combined diodes at floating diffusion node
- Made also on high-res substrate



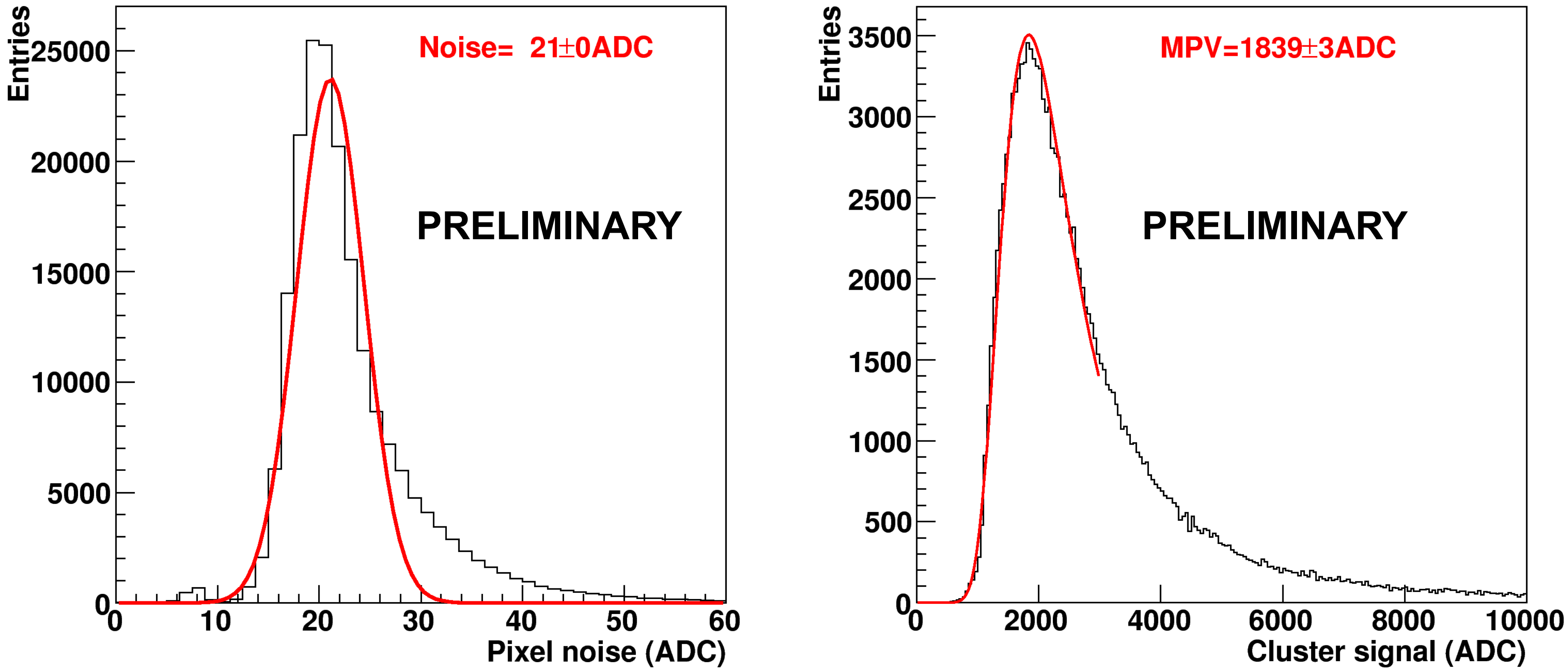
Fortis Testbeam at CERN

- Test at CERN SPS in June 2010
  - 120 GeV Pions
- Taking advantage of EUDET telescope





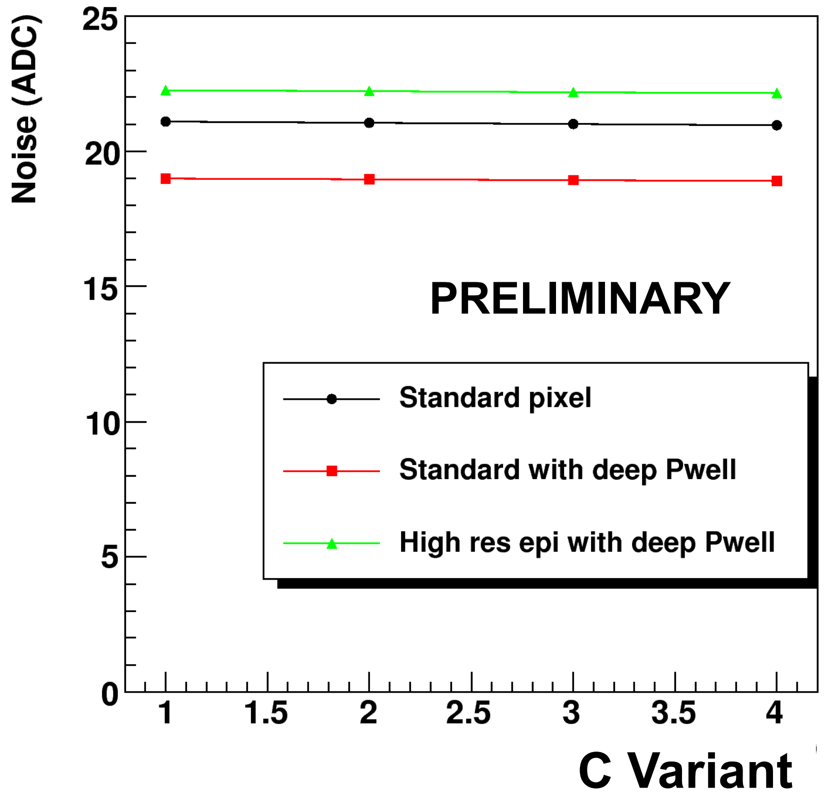
First Fortis Test beam results

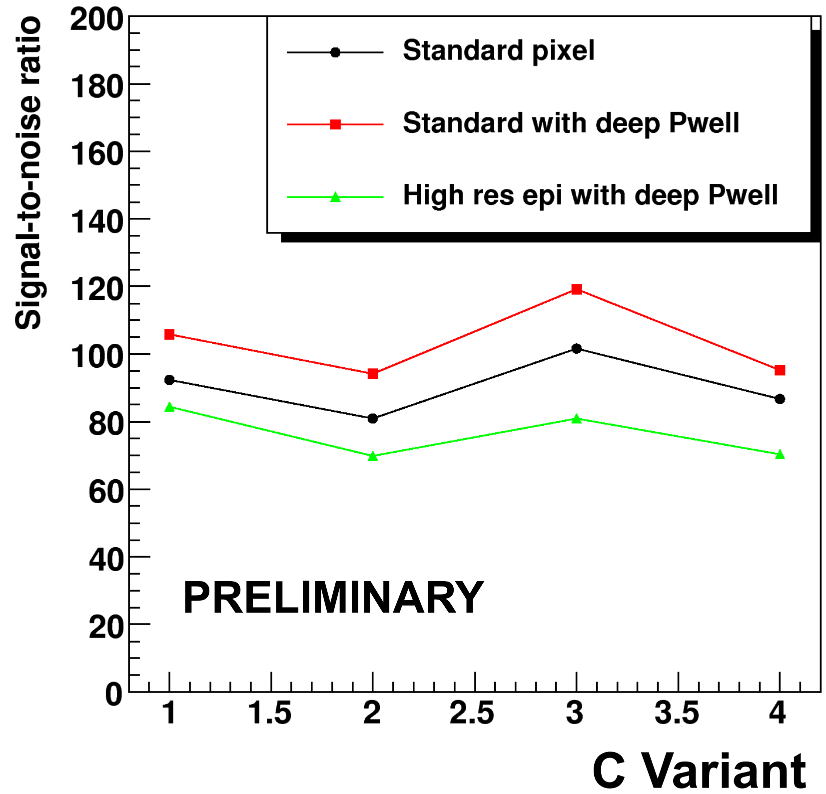


Standard CMOS C1 variant

C variants have 15 µm pitch and different source follower transistor variants

First Fortis Test beam results

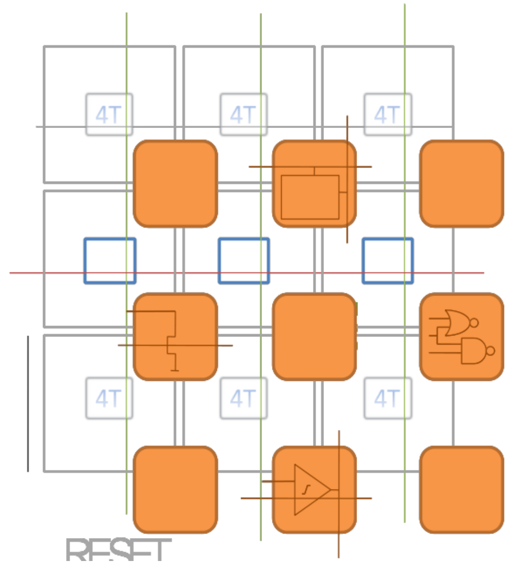


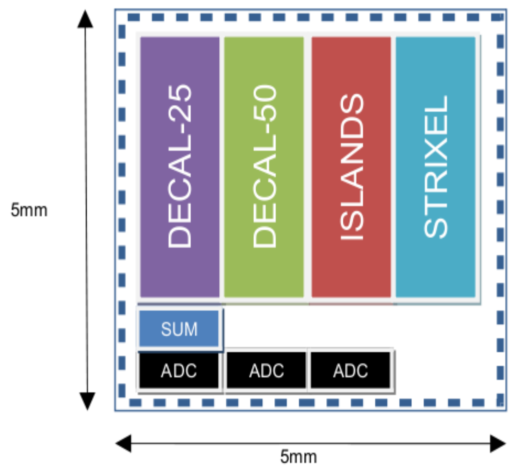


Pixel Variants C1-C4

3) CHERWELL

- Using 4T + INMAPS + high-res
- New ideas (2 variants)
  - Embedded electronics "Islands"
  - Strixels (share electronics for one column)
- DECAL-4T (2 variants)
  - Global Shutter (in-pixel storage)
  - Test pixel pitch and number of diodes
- Two iterations
  - CHERWELL as technology testbed
  - CHERWELL2 as final device



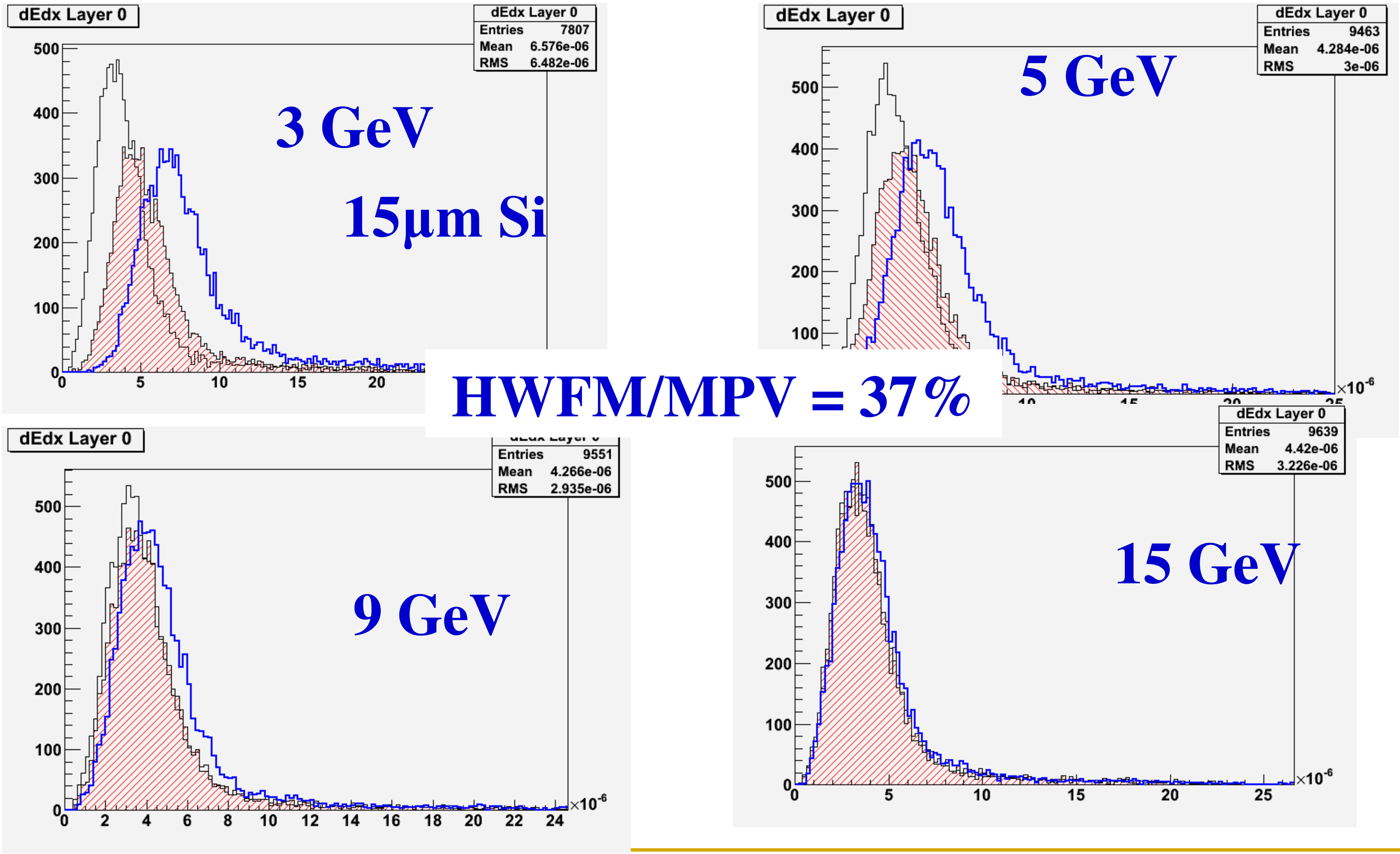


Chip Summary

- TPAC, Fortis and Cherwell chips in hand.
- Now have chip holder so can irradiate chips to test radiation hardness:
  - CERN test beam
  - X-ray
- SuperB UK is piggy-backing on SPiDeR and Atlas Upgrades.
- Should have some test results by December meeting

dE/dx Geant simulation

Simulating CMOS INMAPS sensors

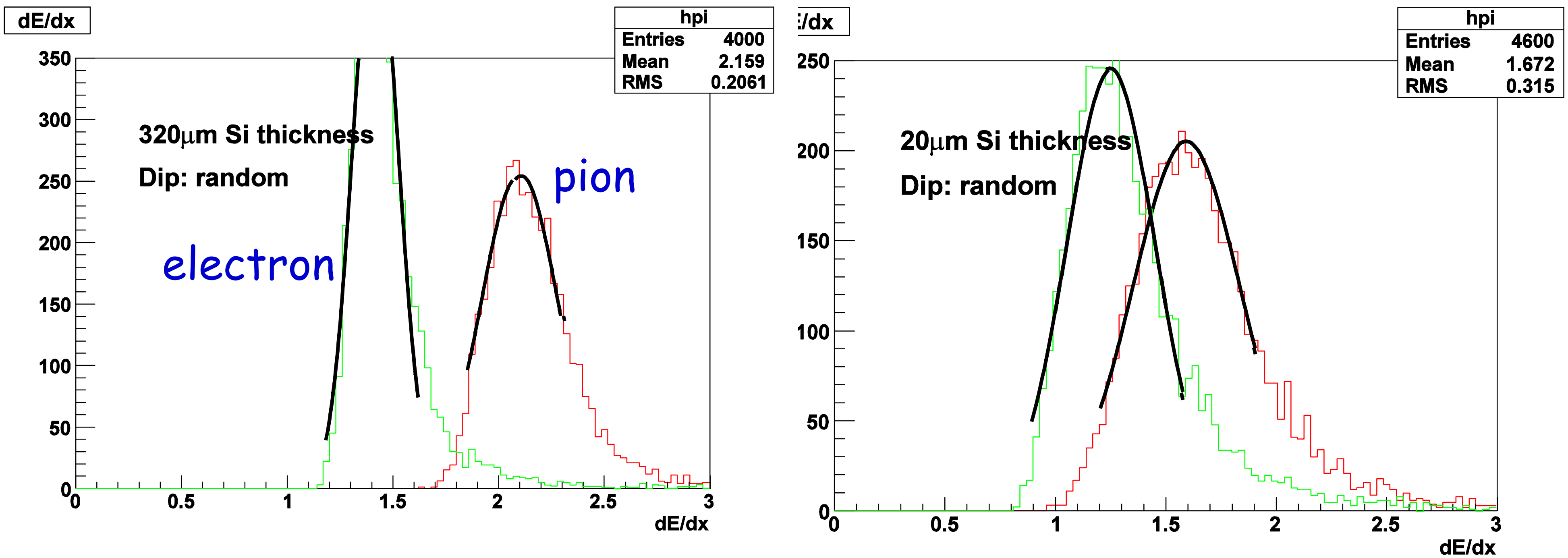


HWFM/MPV = 37%

dE/dx response model simulation

- Magnetic field
- Barrel layout
- Layer 1-4 arranged as at BaBar + Layer 0
- Maximum 10 samples
- Vary dip and Pt of tracks
- Compare
  - Silicon thickness 320um v. 20um
  - dE/dx distribution
  - Electron v. Pion rejection at low momentum
  - Digitisation

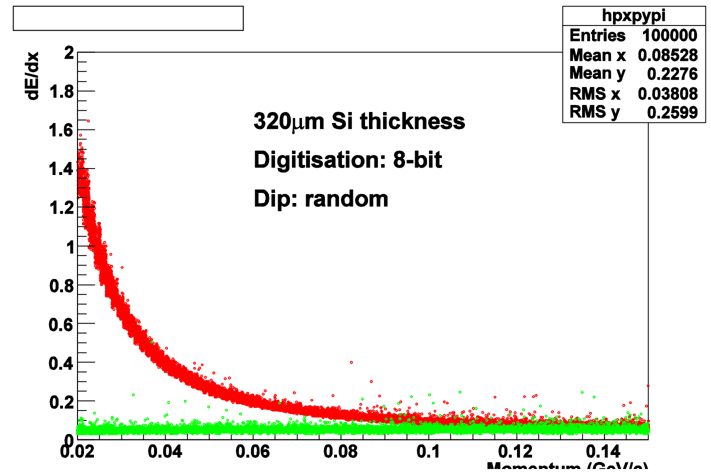
dE/dx Resolution

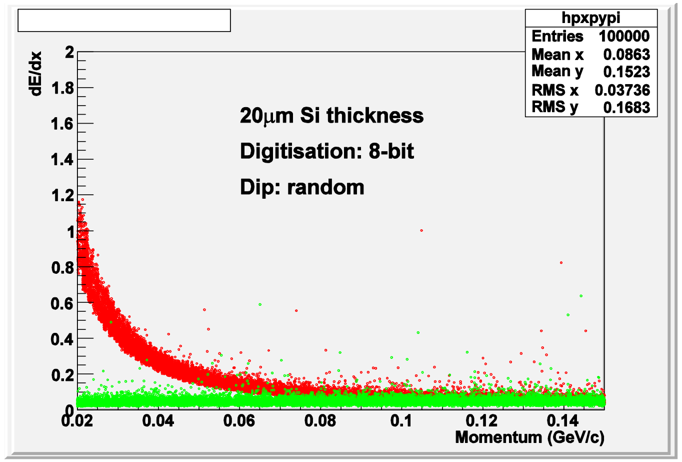


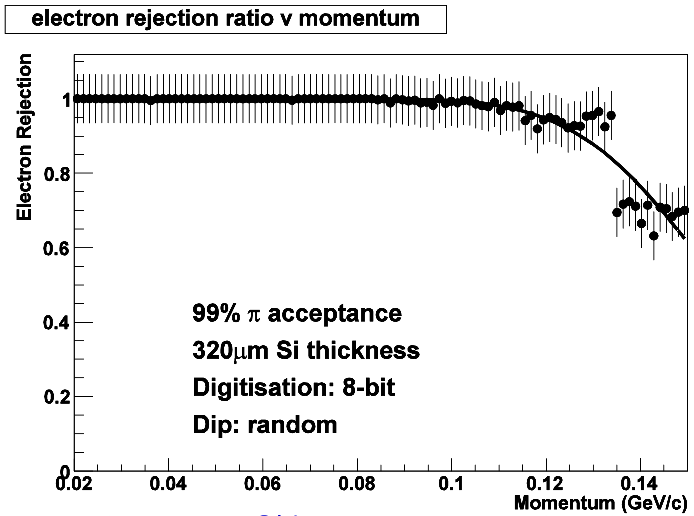
20μm Si has 80% worse dE/dx resolution compared to 320μm

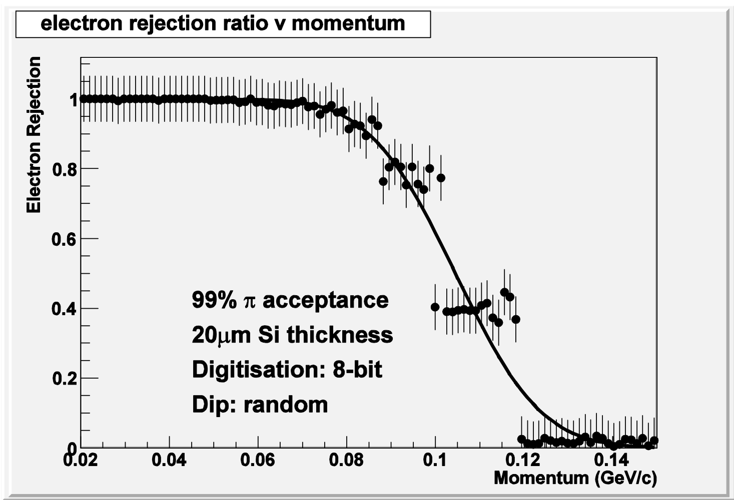
Electron rejection

Identify momentum threshold that achieves 99% pion acceptance



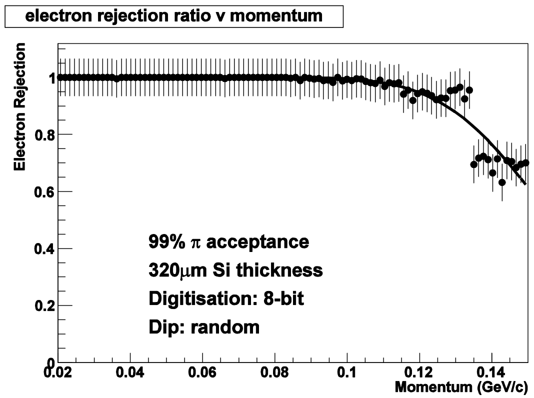


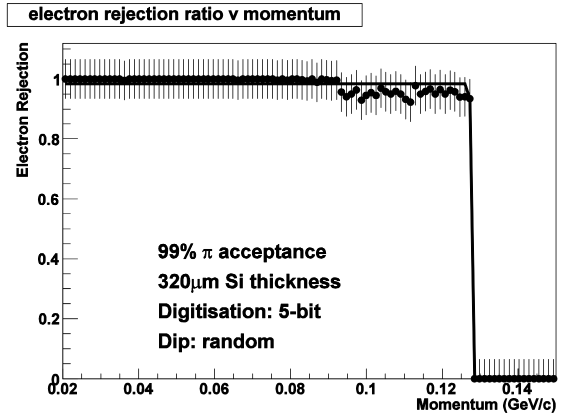




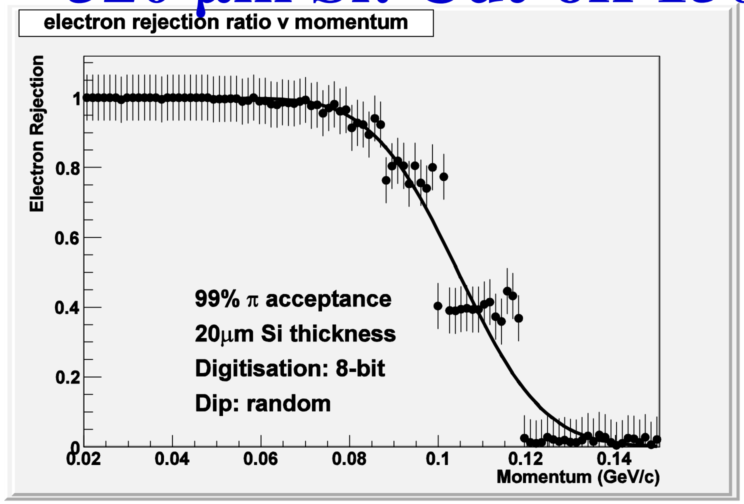
320μm Si: up to 150MeV **20μm Si: up to 100MeV**

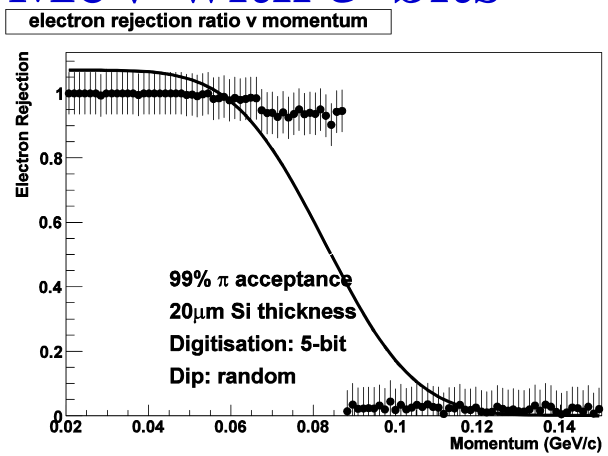
Digitisation





320 μm Si: Cut-off 150 →110 MeV with 5-bits



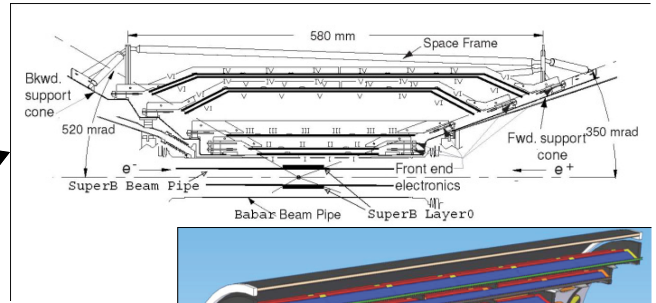


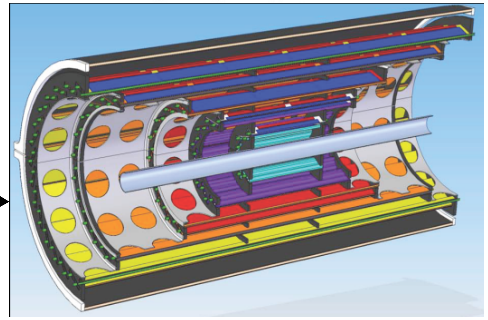
20 μm Si: Cut-off 100 → 80 MeV with 5-bits

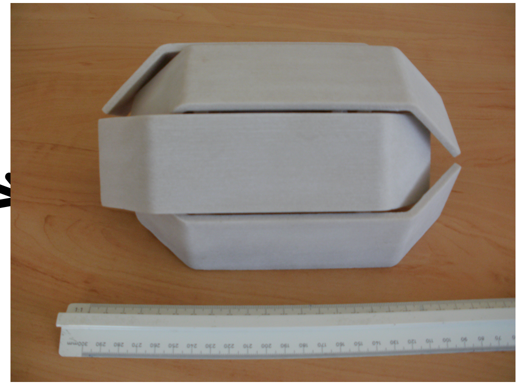
6-bits seems to do a reasonable job

Lampshade v. Long Barrel

- Does a long barrel design add extra scattering?
- $\tau \rightarrow \mu\mu\mu$
- FastSim simulation of:
  - BaBar
  - SuperB baseline (lampshade)
  - Long Barrel
  - Staggered Lampshade



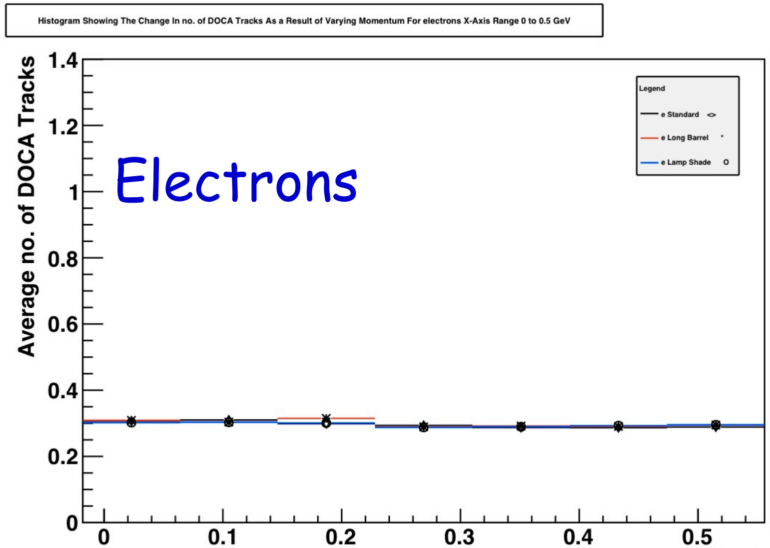




Vertex Model	$\tau \rightarrow \mu\mu\mu$ Efficiency (%)
BaBar	16.1%
SuperB baseline	19.9%
Long Barrel	20.5%
Lampshade	20.0%

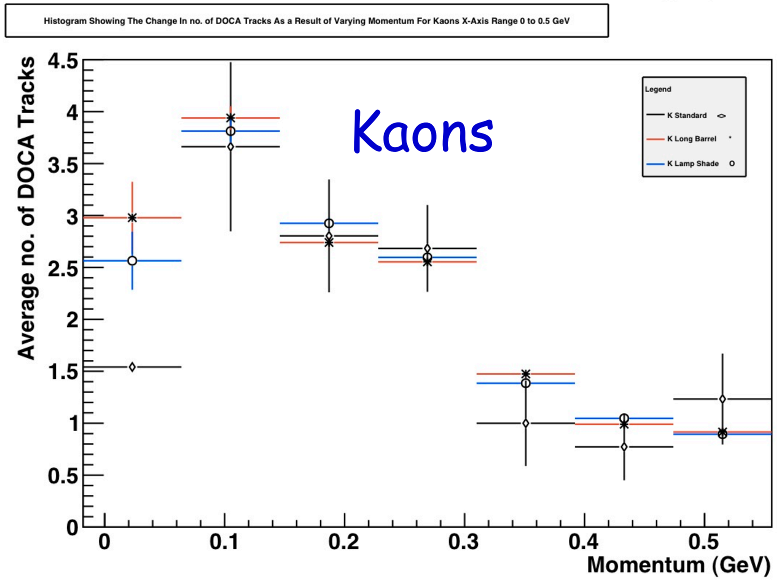
No degradation due to high dip tracks seeing extra material in Long Barrel model

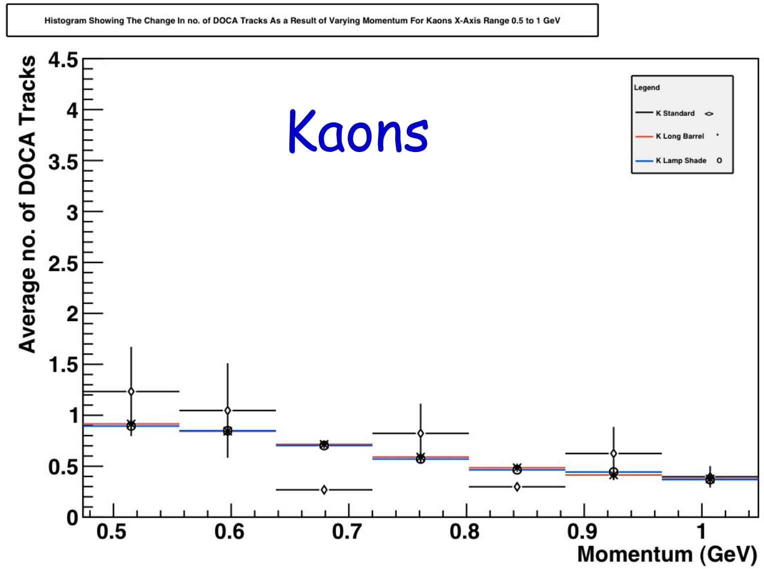
DOCAs from τ->μμμ



Black – Baseline
Red – Long Barrel
Blue - Lampshade

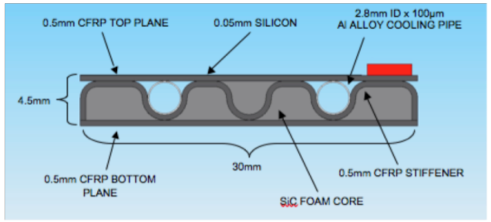
Results produced last week.
Still a lot to be understood.

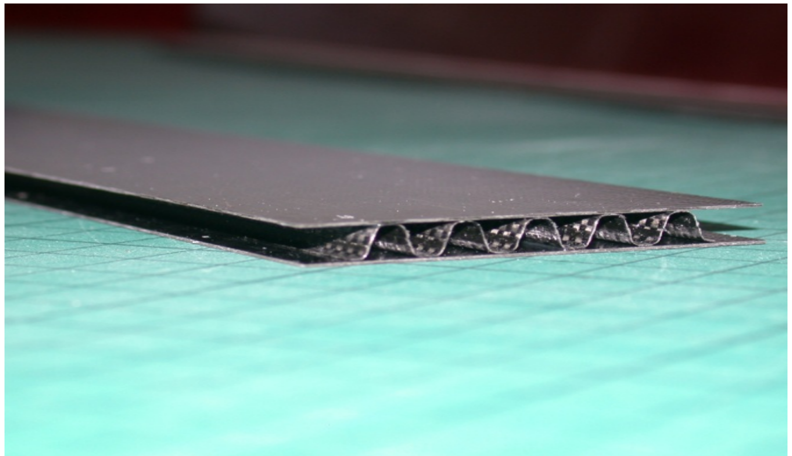


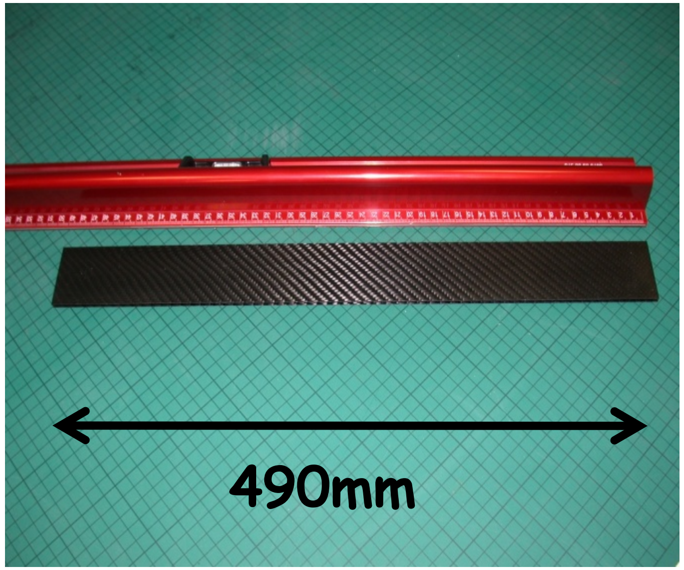


Support Structure

- We've shown an initial stave design but had too much material (1.1%).
- Construction of 1st prototype
  - 1 ply Carbon Fibre (CFRP) weave + 1 ply corrugated + epoxy glue
  - Roughly 0.8% radiation length
  - Thickness 5.2 mm, length 490mm, width 50mm
  - Sagitta 76μm,
  - Slightly bowed (150 μm)





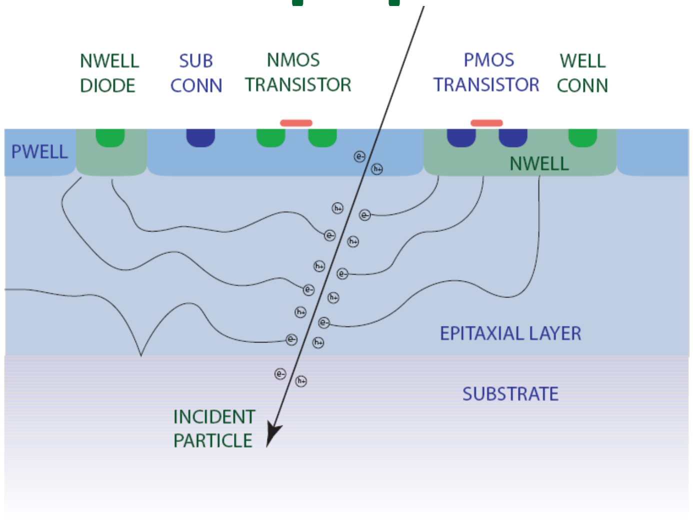


Future Plans

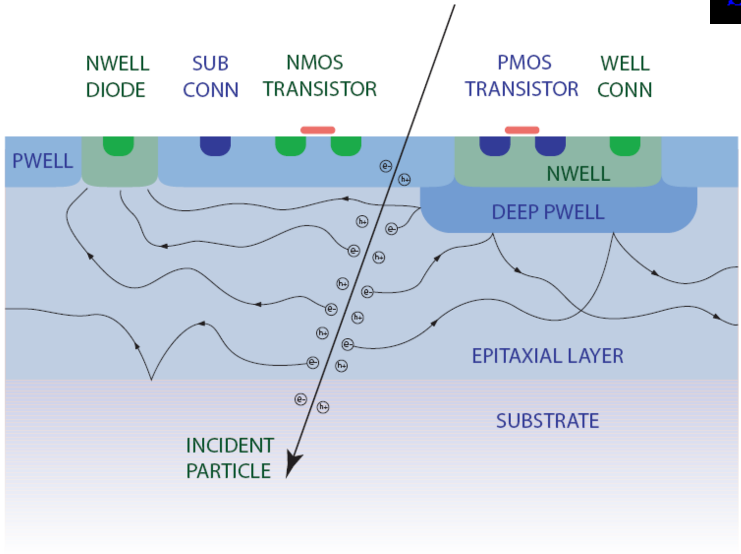
- Characterize chip performance
  - Radiation hardness
  - Test beam and X-rays
  - Readout, noise etc...
- Continue to develop carbon-fibre support ideas
  - Improve flatness
  - Continue to reduce material
  - Introduce cooling pipes/CFRP
  - FEA simulation
  - Test thermal conductivity
- Move to more physics-based studies using FastSim.
- UK Comprehensive Spending Review (CSR) due in October: 25%-40% cuts in government spending.

Backup

Deep p-well implants



Standard CMOS



INMAPS

Standard CMOS Process:

1. 180 nm
2. 6 metal layers
3. Precision passive components (R/C)
4. Low leakage diodes
5. 5/12/18 μm epitaxial layers

Added features for INMAPS

1. Deep p-well (eliminates parasitic collection)
2. High resistivity epitaxial layer (faster charge collection, reduced charge spread, radiation hardness)
3. 4T structures (low-noise, high gain)
4. Stitching (easier manufacturing)

3T versus 4T Pixels

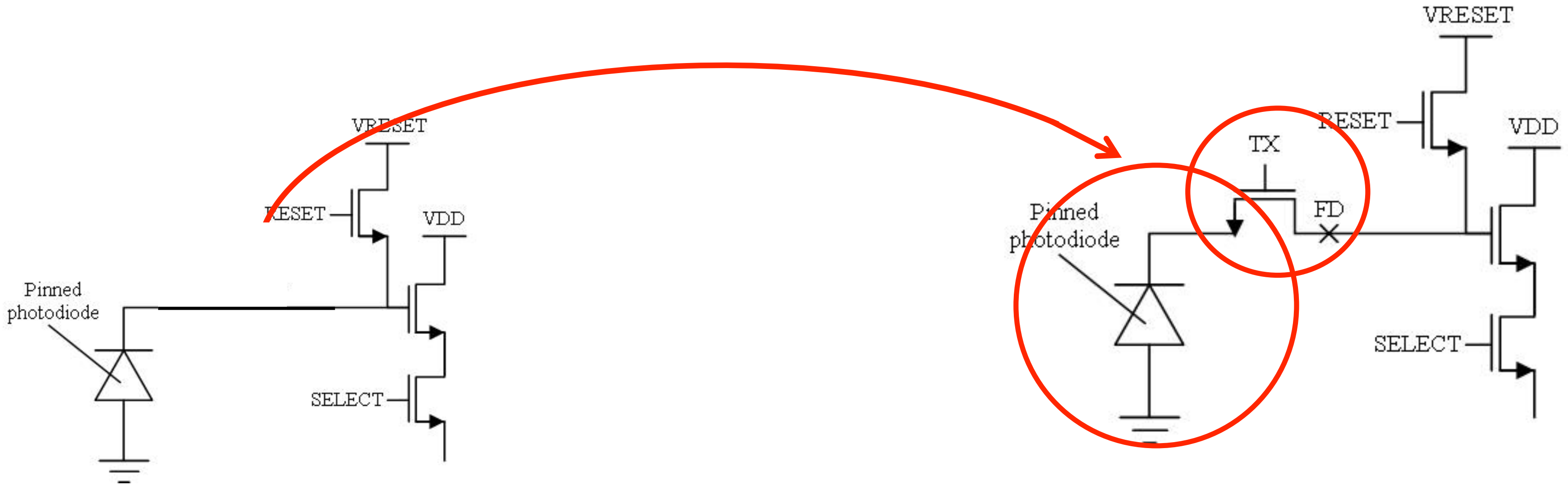
3T MAPS

Readout and charge collection area are the same

4T MAPS

3 additional elements

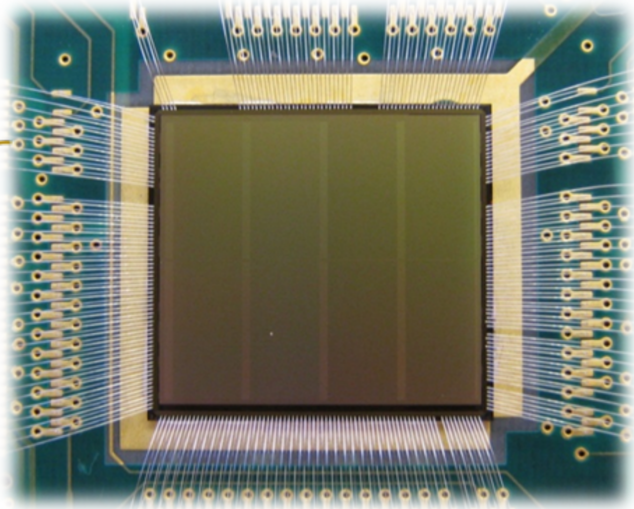
Readout and charge collection area are at different points

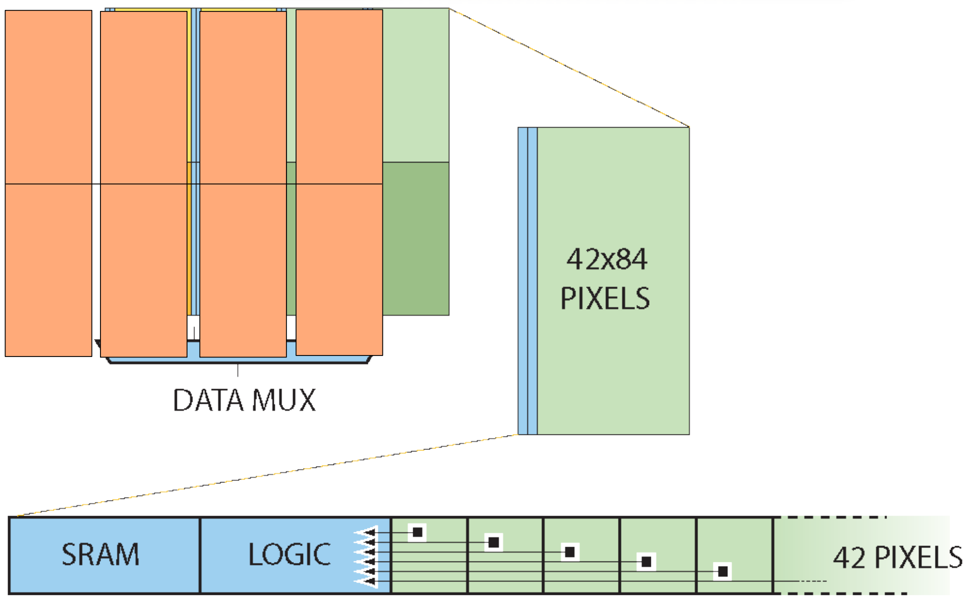


STFC Centre for Instrumentation funded Fortis 1.0/1.1 as a technology prototype

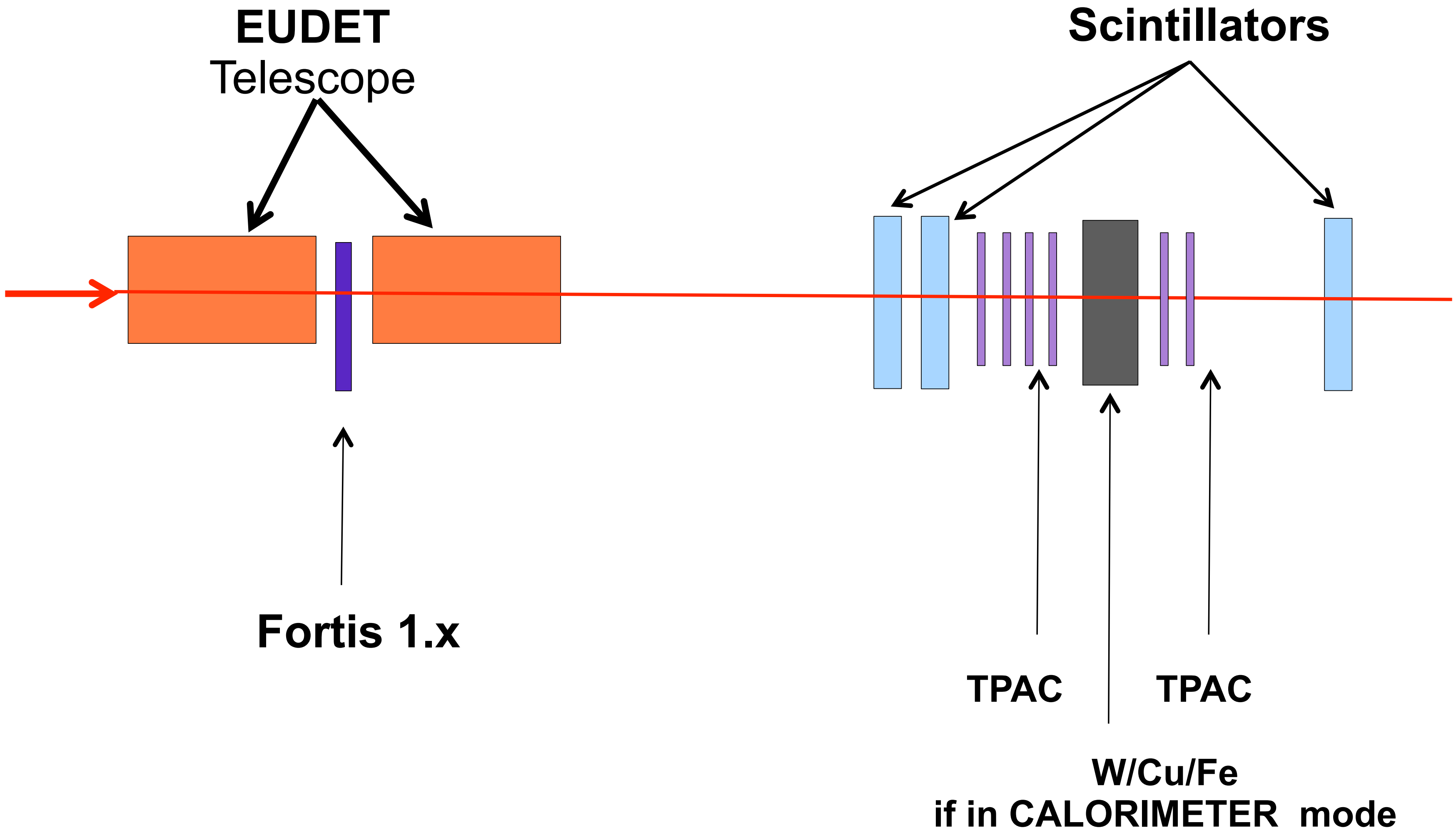
1) The TPAC 1.2 Sensor

- 8.2 million transistors
  - 28224 pixels , 50 x 50 μm
- Sensitive area 79.4 mm^2
  - of which 11.1% "dead" (logic)
- Four columns of logic + SRAM
  - Logic columns serve 42 pixels
  - Record hit locations & timestamps
  - Sparsification on chip
- Data readout
  - Slow (<5Mhz)
  - 30 bit parallel data output
- Developed for
  - Digital ECAL as Particle Counter
- Power 8.9 μW
- Noise 23 e-
- Gain 94 μV/e



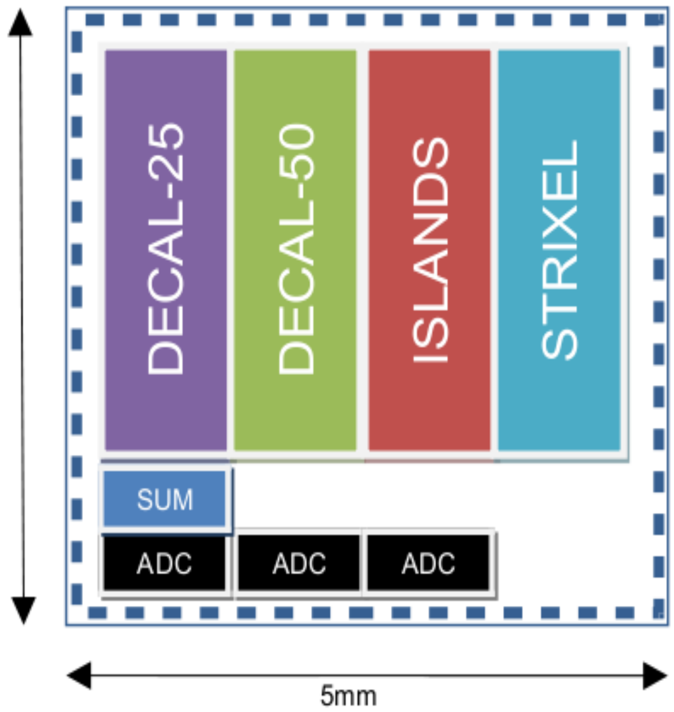


Common Testbeam setup



CHERWELL

- 4T-based chip
  - 5 x5 mm with 4 variants
  - Common backend with ADC's
- DECAL-4T (2 variants)
  - Global Shutter (in-pixel storage)
  - Test pixel pitch and number of diodes
- Islands & Strixels (2 variants)
  - In-pixel electronics
  - ADC folded in column (for Strixel)
- Devices received September



4) TPAC for SuperB

- Vertex detector requirements
  - DC beam (5 ns spacing)
  - taking a snapshot every ~ 500 ns
- Derivative of TPAC 1.x
  - Peak-Hold Circuit
  - Time stamping
  - ADC digitize on demand
- Early design stage