Highly Pixelated Transparent Devices for Future Vertex Detectors

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(on behalf of the MIMOSA, PLUME, Hadron Physics 2 & AIDA collaborations)

▷ more information on IPHC Web site: http://www.iphc.cnrs.fr/-CMOS-ILC-.html

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- CMOS pixel sensors developed by IPHC-IRFU: achievements & current applications
- On-going R&D: directions, goals, timelines, ...
- Synergies with SuperB vertex detector issues
- Summary – Conclusions
CMOS Pixel Sensors: State of the Art

- Prominent features of CMOS pixel sensors:
  - high granularity → excellent (micronic) spatial resolution
  - very thin (signal generated in 10-20 µm thin epitaxial layer)
  - signal processing µ-circuits integrated on sensor substrate

- Sensor organisation:
  - signal sensing and analog processing in pixel array
  - mixed and Digital circuitry integrated in chip periphery
  - read-out in rolling shutter mode
    (pixels grouped in columns read out in //)

- Main characteristics of MIMOSA sensor equipping EUDET BT:
  - 0.35 µm process with high-res. epitaxy (coll. with IRFU/Saclay)
  - column // architecture with in-pixel amplification and end-of-col. discrimination, followed by Ø
  - active area: 1152 columns of 576 pixels (21.2 × 10.6 mm²)
  - pitch: 18.4 µm → ~ 0.7 million pixels → σsp ≲ 4 µm
  - Tr.o. ≲ 100 µs (∼10⁴ frames/s) → suited to >10⁶ part./cm²/s
High-Resistivity CMOS Pixel Sensors

- M.i.p. detection with **LOW & HIGH** resistivity CMOS sensors combined in a Beam Telescope (BT)
  - 4 EUDET ref. sensors & 2 sensors under test
  - June 2010 at CERN-SPS (∼ 120 GeV pions)
  - sensor variants: standard epitaxy (14 µm thick) & high-resistivity epitaxy (10 & 15 µm thick)

- Preliminary conclusions:
  - det. eff. ∼ 100 % (SNR ∼ 40) for very low fake rate:
    - plateau until fake rate of few $10^{-6}$
  - single point resolution ≤ 4 µm
  - det.eff. still ∼ 100 % after exposure to fluence of $1\cdot10^{13} n_{eq}/cm^2$

⇒ Excellent detection performances with high-resistivity epitaxial layer despite moderate resistivity (400 Ω · cm) and poor depletion voltage (< 1 V)

⇒ Tolerance to $\gtrsim O(10^{14}) n_{eq}/cm^2$ seems within reach (study under way)
Direct Applications of MIMOSA-26

- Beam telescope of the FP6 project EUDET
  - 2 arms of 3 planes (plus 1-2 high resolution planes)
  - M-26 thinned to 50 μm
  - $\sigma_{\text{extrapol.}} \sim 1-2 \mu m$ EVEN with $e^-$ (3 GeV, DESY)
  - frame read-out frequency $O(10^4)$ Hz
  - running since '07 (demonstrator: analog outputs)
    at CERN-SPS & DESY (numerous users)

- Spin-offs:
  - Several BT copies: foreseen for detector R&D
  - BT for channelling studies, mass spectroscopy, etc.
  - CBM (FAIR): MVD demonstrator (2-sided layers) for CBM-MVD (HP-2 project)
  - FIRST (GSI): VD for hadrontherapy $\sigma$ measurements
The detector ladders are 50 μm thinned silicon, on a flex kapton/aluminum cable.

0.37% $X_0$/ladder

End view

8 cm radius

2.5 cm radius

20 cm

One of two half cylinders

Inner layer

Outer layer

Cantilevered support

coverage ±1

Total: 40 ladders

1st vertex detector equipped with CMOS pixel sensors → 1st data taking in 2012/13
Next Extensions of MIMOSA-26

- **Vertex Detector of the CBM expt / FAIR**
  - 2 double-sided stations operated in vacuum
  - 0.3–0.5 % $X_0$ per station
  - $\lesssim 5 \mu m$ single pt resolution
  - $\lesssim 10 \mu s$ r.o. time
  - several MRad & $> 10^{13} n_{eq}/cm^2/s$
  - data taking $\gtrsim 2016$ (SIS-100) ... 2020 (SIS-300)

- **ILD Vertex Detector (option):**
  - geometry : 3 double-sided or 5 single-sided layers
  - $\sim 0.2 % X_0$ total material budget per layer
  - $\sigma_{sp} \lesssim 3 \mu m$
  - r.o. time $\lesssim 25–100 \mu s$ (500 GeV)

- **Other applications under consideration**:  
  ALICE upgrades : ITS, FOCAL; VD/eIC, VD/CLIC, (HL-)LHC upgrades, etc.
Sensor Integration in Ultra Light Devices

- Double-sided ladders with time stamping:
  - expected added value of 2-sided ladders:
    - compactness, alignment, pointing accuracy (shallow angle), etc.
  - studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
  - Pixelated Ladder using Ultra-light Material Embedding
  - square pixels for single point resolution on beam side
  - elongated pixels for 4-5 times shorter r.o. time on other side
  - correlate hits generated by traversing particles
  - expected total material budget $\sim 0.2 - 0.3 \% X_0$

- Unsupported & flexible (?) ladders (Hadron Physics 2 / FP-7)
  - 30 $\mu$m thin CMOS sensors mounted on thin cable
    - and embedded in thin polyimide $\rightarrow$ suited to beam pipe?
  - expected total material budget $\lesssim 0.15 \% X_0$

- STAR-PIXEL ladder:
  - total material budget $\sim 0.37 \% X_0$
    - $\Rightarrow$ may become $\lesssim 0.3 \% X_0$ with Al traces
Investigating Large Area Sensors

- Prototype multireticule sensor for large area stations:
  - 3072 × 3072 pixels (16 μm pitch)
    - 5 × 5 cm² sensitive area
  - requires combining several reticules
    - stitching process  
    - establish proof of principle
  - double-sided read-out of 1536 rows in 250–300 μs
    - Large Area Telescope for AIDA project
      (EU-FP7 approved recently)
  - windowing of ≲ 1 × 5 cm² (collim. beam)
    - ≲ 50–60 μs r.o. time
  - 50-100 μm pitch variants under discussion

- Submission expected end of 2011 or early 2012:
  - bonus: avoid paving "large" areas with reticule size sensors
    - dead zones, material, connectics/complexity
  - synergy with tracker layers and forward disk projects on collider & fixed target experiments
  - 6 sensors will compose a beam telescope at CERN (AIDA project deliverable)
    - few ns time stamping resolution associated to each hit by TLU (scintillator)
R&D Road Map for Mid-Term : 2D Sensors

2011:
- 2-sided read-out in < 15 $\mu s$ for 200 columns of 200 pixels
- 50 $\mu m$ pitch viability (det. efficiency, $\sigma_{sp}$)
- exploration of $\leq 0.18 \mu m$ CMOS technologies

2012:
- validation of 35 $\mu m$ pitch pixel array connected to column level ADC
- validation of stitching $\Rightarrow$ large surface sensors
- validation of 2-sided ladder concept with 0.4% $X_0$
- validation of unsupported 0.15% $X_0$ ladder concept
- exploration of $\leq 0.18 \mu m$ CMOS technologies

2013:
- switch to 0.18 $\mu m$ technology $\Rightarrow$ expect $\sim 10 \mu s$ r.o. time, $O(10)$ MRad tolerance
- validation of 2-sided ladder concept with 0.3% $X_0$
- exploration of $< 0.18 \mu m$ CMOS technologies
3D Integration Techno. allow integrating high density signal processing $\mu$circuits inside small pixels

3DIT are expected to be particularly beneficial for CMOS sensors:
- combine different fabrication processes
- alleviate constraints on transistor type inside pixel

Split signal collection & processing functionnalities using optimal technology in each tier:
- Tier-1: epitaxy (depleted or not), deep N-well?
- Tier-2: analog, low $I_{\text{leak}}$, process (nb of ML)
- Tier-3 (& -4): digital VDSM process (nb of ML),
  $\Rightarrow$ fast laser (VOCSEL) driver, etc.

The path to nominal exploitation of CMOS pixel potential:
- fully depleted 10-20 $\mu$m thick epitaxy $\Rightarrow$ $\lesssim$ 5 ns collection time, rad. hardness $>$ Hybrid Pix. Sensors ???
- FEE with $\leq$ 10 ns time resolution $\Rightarrow$ solution for CLIC & HL-LHC specifications ???

Devf of CAIRN $\equiv$ CMOS Active pixel sensors with vertically Integrated Read-out and Networking functionnalities
  $\leftarrow$ 1st set of 4 chips submitted to foundry in Spring 2009 (within 3DIC)
3D Sensor: Towards a High Resistivity Sensing Tier

• Combine 0.13\(\mu m\) 2-tier process with 0.35\(\mu m\) high-resistivity EPI process

DBI ≡ Direct Bond Interconnect: low temperature CMOS compatible direct oxide bonding with scalable interconnect for highest density 3D interconnections (\(\leq 1\ \mu m\) pitch, \(> 10^8/cm^2\) possible)

Tier-1:

◇ fully depleted ⇒ fast charge collection (\(\sim 5\) ns) ⇒ radiation tolerant
◇ for small pitch, charge contained in only few pixels
◇ sufficient S/N ratio defined by the 1st stage
◇ "charge amplification" (\(>\) factor 10) by capacitive coupling of the 1st to the 2nd stage

Tier-2:

◇ single stage, high gain, folded cascode based charge amplifier, with current source in the feedback loop
  ⇒ shaping time \(\sim 200\) ns for the sake of time resolution
◇ small offset, continuous discriminator

Tier-3:

◇ matrix of 256×256 pixels ⇒ 2 \(\mu s\) read-out time

• 1st prototype (with 1-bit ADC) submitted in Spring ’09 ⇒ still expected back ...
CMOS sensors with fast pipeline digital r.o. \(\implies\) minimise power consumption:

- Subdivide sensitive area in "small" arrays running individually in rolling shutter mode
- Adapt the number of rows to required frame r.o. time
  \(\implies\) few \(\mu s\) r.o. time achievable
- Design fitting \(20 \times 20 \, \mu m^2\):
  - Tier-1: sensor & pre-amplifier \((G \sim 500 \, \mu V/e^-)\)
  - Tier-2: 4-bit pixel-level ADC with offset cancellation circuitry \((LSB \sim N) \lesssim 2 \, \mu m\) resolution
  - Tier-3: fast pipeline read-out with integrated data sparsification

1st prototype (with 1-bit ADC) submitted in Spring ’09 \(\implies\) still expected back...
R&D Road Map for Long-Term : 3D Sensors

• 2011-2012 :
  ※ proof of principle of heterogeneous CMOS sensor concept:
    connection of 0.35 $\mu m$ high-res sensing tier to 0.13 $\mu m$ 2-tier r.o. chip (within AIDA)
  ※ exploration of $\lesssim 0.1$ $\mu m$ CMOS technologies
  ※ exploration of connection and thinning techniques

• 2013-2014 :
  ※ validation of architecture allowing for $\lesssim O(\mu s)$ r.o. time
  ※ R&D on radiation tolerance
  ※ exploration of $\lesssim 0.1$ $\mu m$ CMOS technologies
  ※ exploration of connection and thinning techniques

• 2015-2016 :
  ※ validation of 1st full size thin and fast sensor adapted to experimental specifications (e.g. CBM-MVD)
  ※ start designing dedicated sensors exploiting the concept developed
Towards Light Pixelated Systems adapted to a SuperB Factory

- Synergies with SuperB oriented devts: sensors and pixelated systems

- Exploit concept of double-sided ladders to fill space between SVT & beam pipe:
  ✗ 1 or 2 layers (replacing SVT inner layer) ?
  ✗ complete with unsupported ladder on beam pipe? (optimistic !)

- Synergy with the development of 3 generations of sensors:
  ✗ 1st generation: 2D sensor in 0.35 μm high-res techno. (prototyping completed ≲ 2013)
    ▶ MIMOSA-26 like architecture with 50 μm pitch with 10–15 μs r.o. time
  ✗ 2nd generation: 2D sensor in 0.18 μm triple well, high-res, techno. (prototyping completed ≲ 2015)
    ▶ new architecture expected to allow for a few μs r.o. time and > 10 MRad tolerance
  ✗ 3rd generation: 3D sensor combing 0.18 μm high-res sensitive tier with ≤ 0.13 μm 2-tier r.o. chip
    (prototyping completed ≲ 2017)
    ▶ architecture expected to allow for < 1 μs r.o. time and very high data flow
CMOS sensor technology is mature for high performance vertexing but its full potential is still far from being exploited (despite improvement generated by high-res epitaxial layer processes).

- explore $\leq 0.18 \mu m$, high-res, multi-well manufacturing technologies

CMOS pixels equipping a double-sided ladder seem to provide an attractive perspective for the SuperB vertex detector innermost layer(s?)

R&D at IPHC addresses 3 sensor generations, featuring increasing performance levels

- may be worth assessing the merit of each of them for the SuperB program

3D chips are the most promising, but there is a long way to go

- keep pushing 2D sensor approach to its best

R&D at IPHC may bring valuable contributions to the Layer-0 project

- exploit the synergy with INFN
Reminder: Main Features of CMOS Sensors

- P-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    \[ Q \sim 80 \text{ e-h} / \mu m \implies \text{signal} \lesssim 1000 \text{ e}^- \]
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode with help of reflection on boundaries with p-well and substrate (high doping)

- Prominent advantages of CMOS sensors:
  - granularity: pixels of \( \lesssim 10 \times 10 \, \mu m^2 \) \( \Rightarrow \) high spatial resolution
  - low mat. budget: sensitive volume \( \sim 10 - 20 \, \mu m \) \( \Rightarrow \) total thickness \( \lesssim 50 \, \mu m \)
  - signal processing \( \mu \)circuits integrated in the sensors \( \Rightarrow \) compacity, high data throughput, flexibility, etc.
  - other attractive aspects: cost, multi-project run frequency, \( T_{room} \) operation, etc.

▷▷▷ Thinning down to \( \sim 30 \, \mu m \) permitted
The Trend for Ultra-Light Pixelated Devices

- Trend of subatomic physics experiments for highly granular and thin pixel devices

- Central motivation:
  - high performance reconstruction of (displaced) charm vertices
  - high performance multi-jet final state flavour tagging \((t\bar{t}, t\bar{t}H, AH, ...)\)

- Flagship of this trend: International Linear Collider (ILC) → Letters of Intent delivered in 2009
  ↞ Detector Baseline Document \((\approx TDR)\) to be delivered by 2012
  ※ also: Heavy Ion experiments, CLIC, LHC upgrades, ..., hadrontherapy, ...

→ Figure of merit: \(\sigma_{ip} = a \oplus b/p \cdot \sin^{3/2} \theta\)
  ※ \(a\) governs high momentum
  ※ \(b\) governs low momentum (\(~30\%\) particles \(<1\text{ GeV/c}\))

<table>
<thead>
<tr>
<th>Accelerator</th>
<th>(a) ((\mu m))</th>
<th>(b) ((\mu m \cdot GeV))</th>
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</thead>
<tbody>
<tr>
<td>LEP</td>
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<td>70</td>
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<td>SLD</td>
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<tr>
<td>ILC</td>
<td>(&lt;5)</td>
<td>(&lt;10)</td>
</tr>
</tbody>
</table>

![Figure showing coupling constant to Higgs Boson, \(g_\chi\)](image-url)

Mass [GeV] vs. Coupling constant to Higgs Boson, \(g_\chi\)
Impact of $1 \cdot 10^{13} n_{eq}/cm^2$ on detection performances at $T_{op} \sim 0^\circ C$

### Preliminary conclusions:

- Det. eff. $\sim 100\%$ for very low fake rate: HR-15 plateau until fake rate of few $10^{-6}$
- Single point resolution $\lesssim 4 \mu m$
- Det. eff. of HR-15 still $\sim 100\%$ after exposure to $1 \cdot 10^{13} n_{eq}/cm^2$

⇒ Striking evidence for performance improvement with HR epitaxy (in particular 15 $\mu m$ thick)
Cold Baryonic Matter (CBM) experiment at FAIR:

- Micro-Vertex Detector (MVD) made of 2 of 3 stations located behind fixed target
- double-sided stations equipped with CMOS pixel sensors
- operation a negative temperature in vacuum
- each station accounts for \( \lesssim 0.5\% X_0 \)
- sensor architecture close to ILC version

Most demanding requirements:

- ultimately (\( \sim 2020 \)): 3D sensor
  \( \lesssim 10 \mu s, > 10^{14} n_{eq}/cm^2, \gtrsim 30 \) MRad
- intermediate steps: 2D sensors
  \( \lesssim 30-40 \mu s, > 10^{13} n_{eq}/cm^2, \gtrsim 3 \) MRad
- 1st sensor for SIS-100 (data taking \( \sim 2016 \))
AIDA ≡ EU FP-7 Integrated Infrastructure project: approved → starts Feb. 2011

On-beam (CERN-SPS) test infrastructure:

- Large Area beam Telescope (LAT) → 5×5 cm² stitched sensors
- Alignment Investigation Devices (AID):
  - box hosting pairs of ladders (e.g. PLUME) and unsupported pixelated systems (SERWIETE)
  - box front panel contains removable target

Work program topics ▶▶▶ relevant for numerous high resolution devices:

- alignment capabilities: dedicated equipment and particle tracks
- vertex reconstruction accuracy
- track reconstruction with different devices (high spatial resolution combined with fast detectors)
LePIX: monolithic detectors in advanced CMOS

- Submission for fabrication just finalized
  - Several issues: ESD, special layers and mask generation, guard rings
  - Still need to discuss some outstanding fabrication issues with IBM
- 7 chips submitted:
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission
- Will require very significant testing effort for which we need to prepare (measurement setup, test cards…)

W. Snoeys, CERN-ESE-ME, 2010