Highly Pixelated Transparent Devices for Future Vertex Detectors

Marc Winter (IPHC-Strasbourg)

(on behalf of the MIMOSA, PLUME, Hadron Physics 2 & AIDA collaborations)

▷ more information on IPHC Web site: **http://www.iphc.cnrs.fr/-CMOS-ILC-.html**

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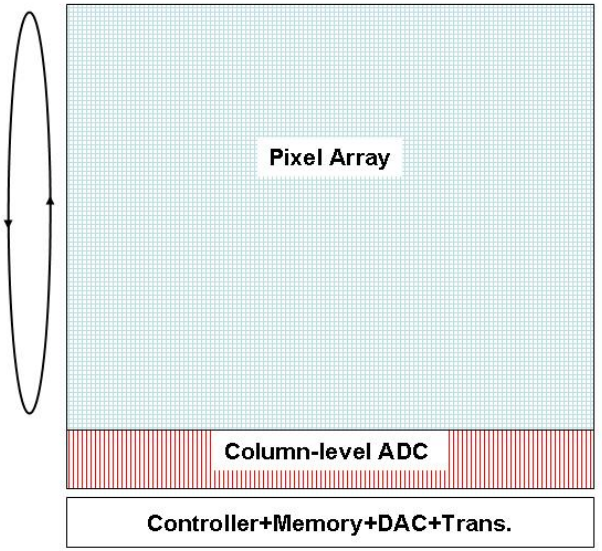
- **CMOS pixel sensors developed by IPHC-IRFU :** achievements & current applications
- **On-going R&D:** directions, goals, timelines, ...
- **Synergies with SuperB vertex detector issues**
- **Summary – Conclusions**

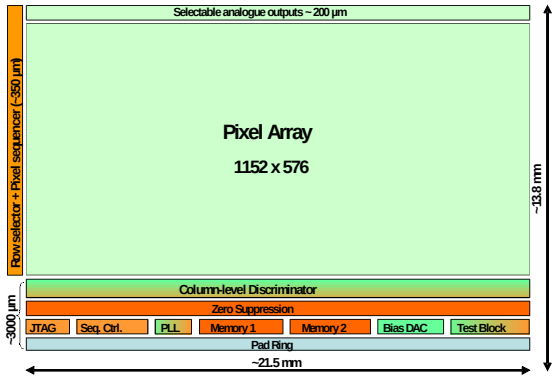
CMOS Pixel Sensors: State of the Art

- **Prominent features of CMOS pixel sensors:**
  - ⁂ high granularity $\Rightarrow$ excellent (micronic) spatial resolution
  - ⁂ very thin (signal generated in 10-20 μm thin epitaxial layer)
  - ⁂ signal processing μ-circuits integrated on sensor substrate



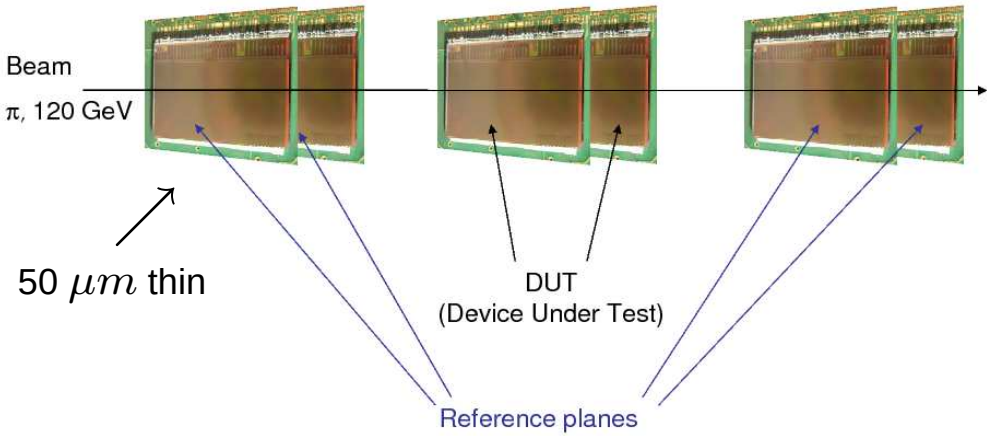
- **Sensor organisation:**
  - ⁂ signal sensing and analog processing in pixel array
  - ⁂ mixed and Digital circuitry integrated in chip periphery
  - ⁂ read-out in rolling shutter mode
    (pixels grouped in columns read out in //)

- **Main characteristics of MIMOSA sensor equipping EUDET BT:**
  - ⁂ 0.35 μm process with high-res. epitaxy (coll. with IRFU/Saclay)
  - ⁂ column // architecture with in-pixel amplification
    and end-of-col. discrimination, followed by $\emptyset$
  - ⁂ active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - ⁂ pitch: 18.4 $\mu m \rightarrowtail \sim$ 0.7 million pixels $\Rightarrow$ $\sigma_{sp} \lesssim 4\ \mu m$
  - ⁂ $T_{r.o.} \lesssim 100\ \mu s$ ($\sim 10^4$ frames/s) $\Rightarrow$ suited to $>10^6$ part./cm^2/s



High-Resistivity CMOS Pixel Sensors

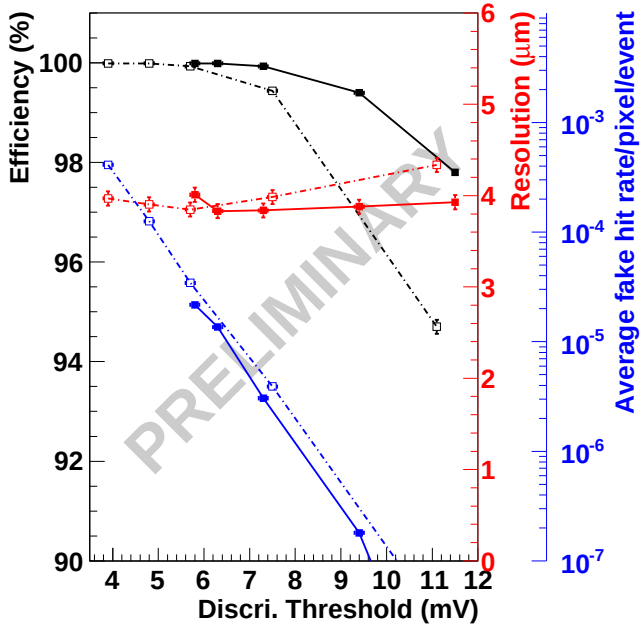
- **M.i.p. detection with LOW & HIGH resistivity CMOS sensors combined in a Beam Telescope (BT)**
  - ⁕ 4 EUDET ref. sensors & 2 sensors under test
  - ⁕ June 2010 at CERN-SPS ($\sim$ 120 GeV pions)
  - ⁕ sensor variants : standard epitaxy (14 μm thick)
    & high-resistivity epitaxy (10 & 15 μm thick)



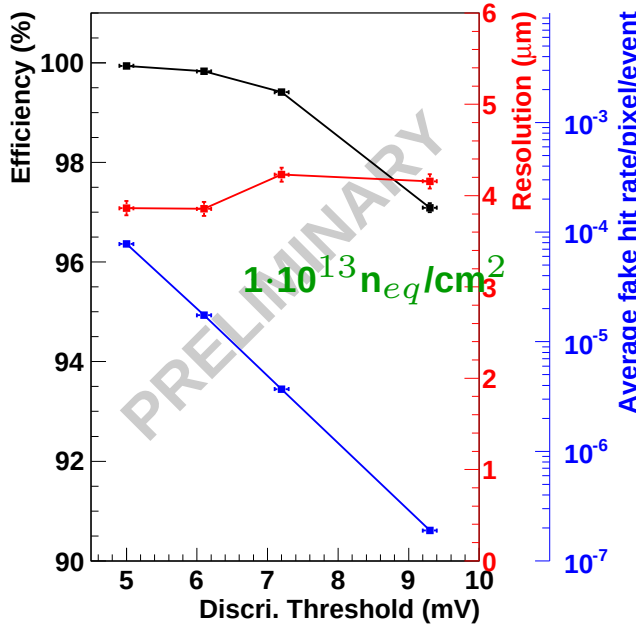
- **Preliminary conclusions:**
  - ⁕ det. eff. $\sim$ 100 % (SNR $\sim$ 40) for very low fake rate:
    - ▷ plateau until fake rate of few 10^{-6}
  - ⁕ single point resolution $\lesssim 4\ \mu m$
  - ⁕ det.eff. still $\sim$ 100 % after exposure
    to fluence of $1{\cdot}10^{13}$ n_{eq}/cm^2

⇒ **Excellent detection performances**
with high-resistivity epitaxial layer
despite moderate resistivity ($400\ \Omega \cdot cm$)
and poor depletion voltage (< 1 V)

Mi26 HR-15 and HR-10 Efficiency, Fake rate and Resolution



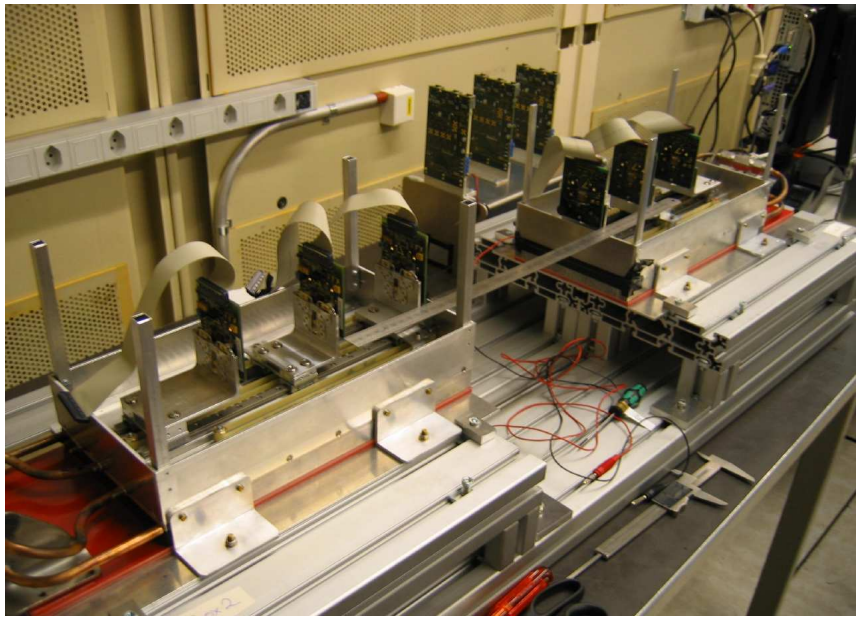
Mi26 HR-15 Efficiency, Fake rate and Resolution
for a chip irradiated with a $1.10^{13}N_{eq}$ dose at T_{op} ~ 0° C



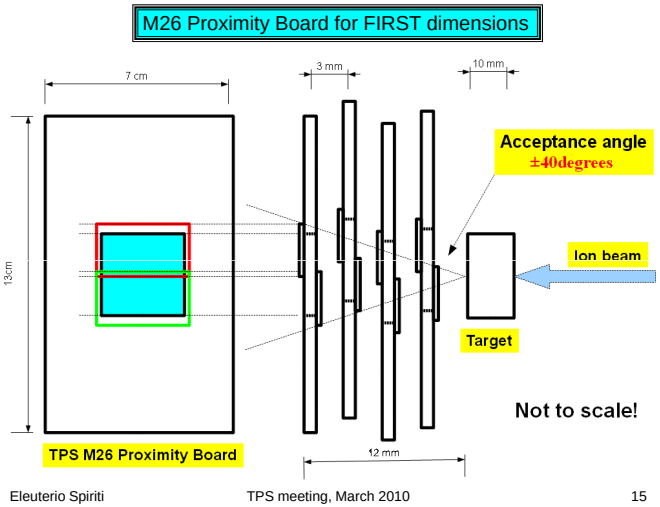
⇒ **Tolerance to $\gtrsim$ O(10^{14}) n_{eq}/cm^2 seems within reach (study under way)**

Direct Applications of MIMOSA-26

- **Beam telescope of the FP6 project EUDET**
  - 2 arms of 3 planes (plus 1-2 high resolution planes)
  - M-26 thinned to 50 μm
  - $\sigma_{extrapol.} \sim$ 1-2 μm EVEN with e^- (3 GeV, DESY)
  - frame read-out frequency O(10^4) Hz
  - running since '07 (demonstrator: analog outputs)
    at CERN-SPS & DESY (numerous users)

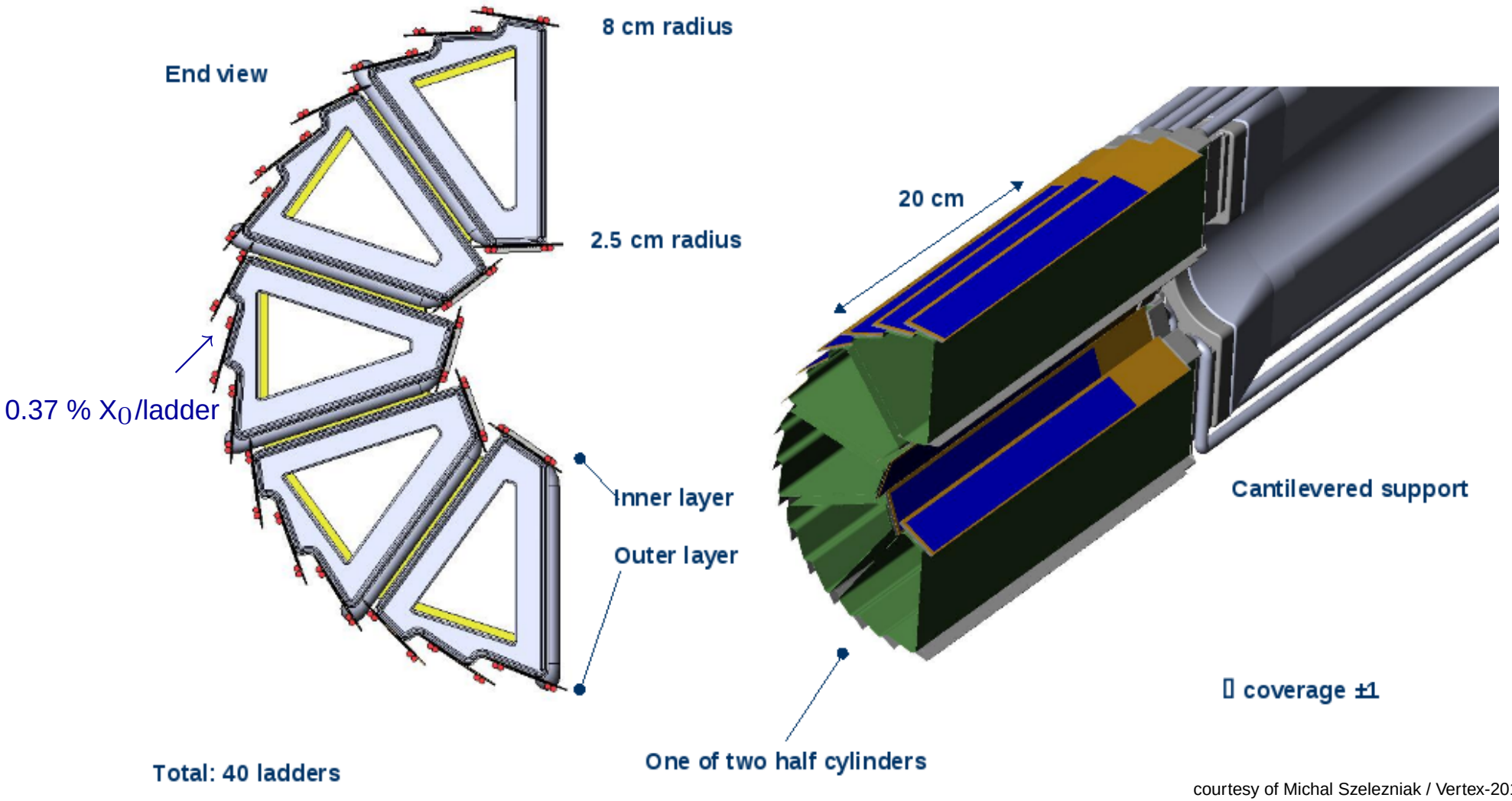


- **Spin-offs :**
  - **Several BT copies :** foreseen for detector R&D
  - **BT** for channelling studies, mass spectroscopy, etc.
  - **CBM (FAIR) :** MVD demonstrator (2-sided layers) for CBM-MVD (HP-2 project)
  - **FIRST (GSI) :** VD for hadrontherapy σ measurements ▷▷▷



Application of CMOS sensors to the STAR-PIXEL

The detector ladders are 50 µm thinned silicon, on a flex kapton/aluminum cable.

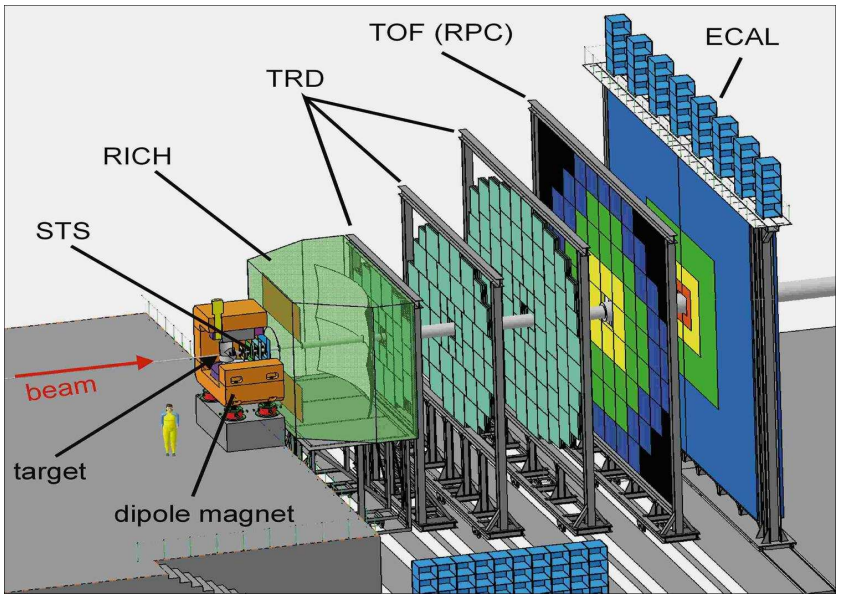


courtesy of Michal Szelezniak / Vertex-2010

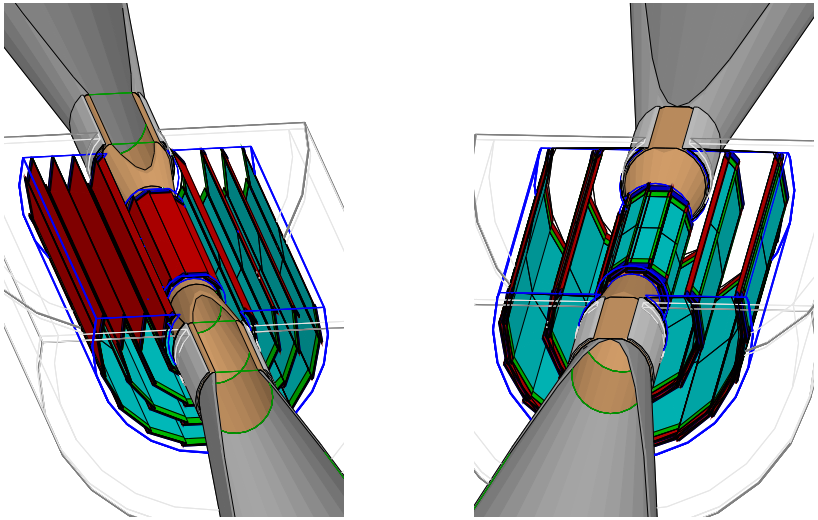
▷▷▷ **1st vertex detector equipped with CMOS pixel sensors ⟶ 1st data taking in 2012/13**

Next Extensions of MIMOSA-26

- **Vertex Detector of the CBM expt / FAIR**
  - 2 double-sided stations operated in vacuum
  - 0.3–0.5 % X_0 per station
  - $\lesssim$ 5 μm single pt resolution
  - $\lesssim$ 10 μs r.o. time
  - several MRad & $> 10^{13}$ $n_{eq}/cm^2/s$
  - data taking $\gtrsim$ 2016 (SIS-100) ... 2020 (SIS-300)



- **ILD Vertex Detector** (option) **:**
  - geometry : 3 double-sided or 5 single-sided layers
  - $\sim$ 0.2 % X_0 total material budget per layer
  - $\sigma_{sp} \lesssim 3\ \mu m$
  - r.o. time $\lesssim$ 25–100 μs (500 GeV)

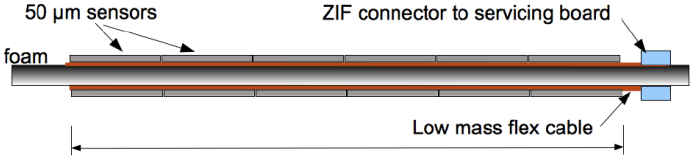


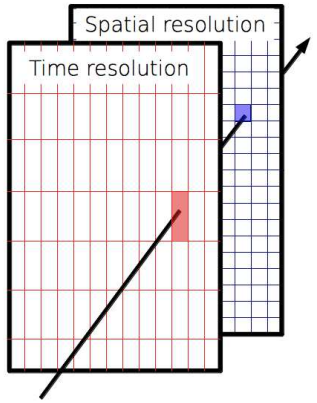
- **Other applications under consideration :**

  ALICE upgrades : ITS, FOCAL; VD/eIC, VD/CLIC, (HL-)LHC upgrades, etc.

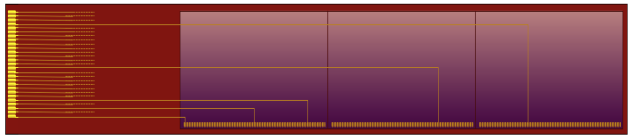
Sensor Integration in Ultra Light Devices

- **Double-sided ladders with time stamping :**
  - ⁂ expected added value of 2-sided ladders:
    compactness, alignment, pointing accuracy (shallow angle), etc.
  - ⁂ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    $\hookrightarrow$ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⁂ square pixels for single point resolution on beam side
  - ⁂ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⁂ correlate hits generated by traversing particles
  - ⁂ expected total material budget $\sim$ 0.2 - 0.3 % X_0

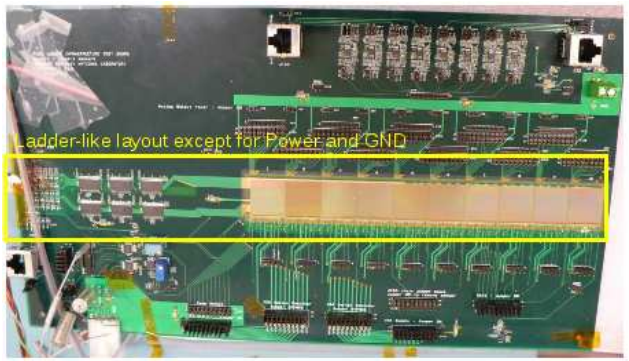




- **Unsupported & flexible (?) ladders (Hadron Physics 2 / FP-7)**
  - ⁂ 30 μm thin CMOS sensors mounted on thin cable
    and embedded in thin polyimide $\rightarrowtail$ suited to beam pipe ?
  - ⁂ expected total material budget $\lesssim$ 0.15 % X_0

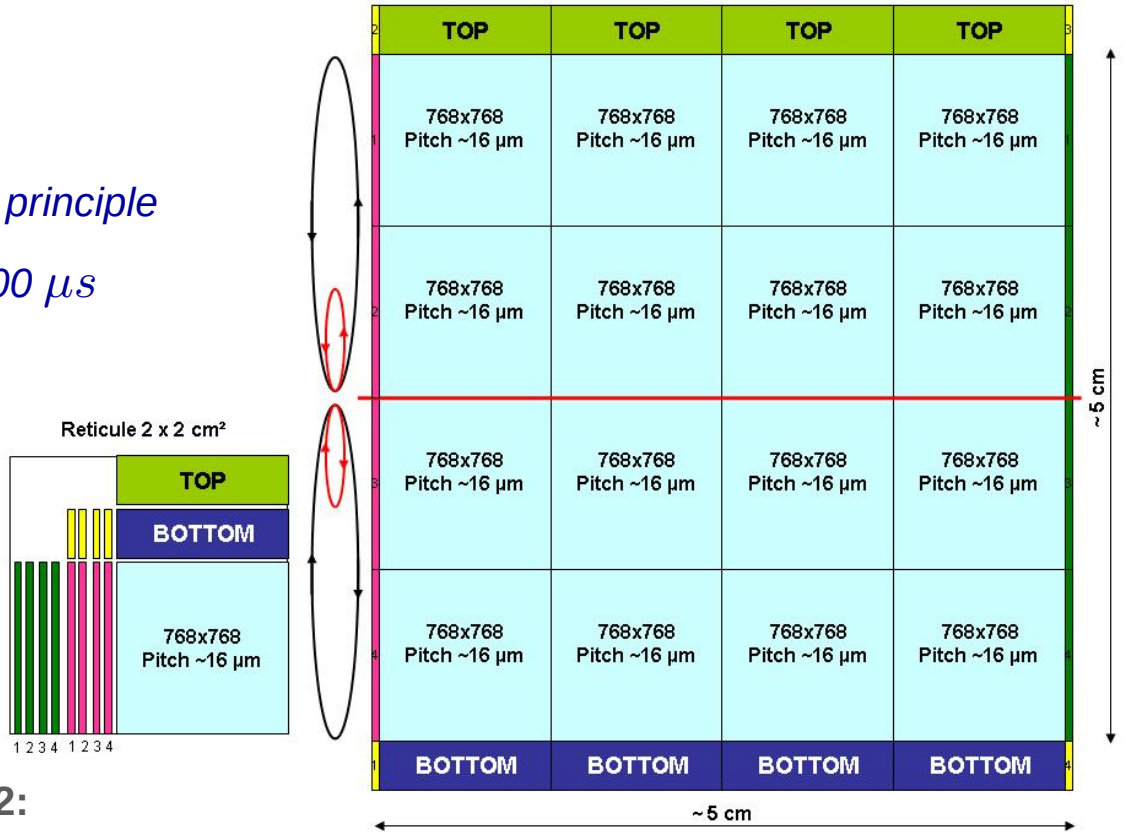


- **STAR-PIXEL ladder:**
  - ⁂ total material budget $\sim$ 0.37 % X_0
    $\Rightarrow$ may become $\lesssim$ 0.3 % X_0 with Al traces



Investigating Large Area Sensors

- **Prototype multireticule sensor for large area stations:**
  - ⁕ *3072×3072 pixels (16 μm pitch)*
    - ⇛ *5×5 cm^2 sensitive area*
  - ⁕ *requires combining several reticules*
    - ⇛ *stitching process* ⇛ *establish proof of principle*
  - ⁕ *double-sided read-out of 1536 rows in 250–300 μs*
    - ⇛ *Large Area Telescope for AIDA project*
      (EU-FP7 approved recently)
  - ⁕ *windowing of $\lesssim$ 1×5 cm^2 (collim. beam)*
    - ⇛ *$\lesssim$ 50–60 μs r.o. time*
  - ⁕ *50-100 μm pitch variants under discussion*



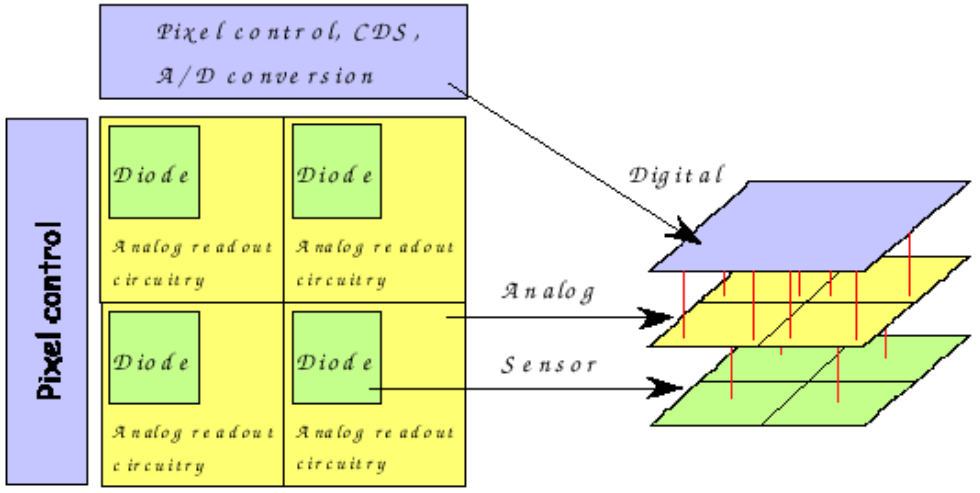
- **Submission expected end fo 2011 or early 2012:**
  - ⁕ bonus: avoid paving ”large” areas with reticule size sensors
    - ⇛ dead zones, material, connectics/complexity
  - ⁕ synergy with tracker layers and forward disk projects on collider & fixed target experiments
  - ⁕ 6 sensors will compose a beam telescope at CERN (AIDA project deliverable)
    - ▷ few ns time stamping resolution associated to each hit by TLU (scintillator)

R&D Road Map for Mid-Term : 2D Sensors

- **2011 :**
  - 2-sided read-out in $<$ 15 μs for 200 columns of 200 pixels
  - 50 μm pitch viability (det. efficiency, σ_{sp})
  - exploration of $\leq$ 0.18 μm CMOS technologies
- **2012 :**
  - validation of 35 μm pitch pixel array connected to column level ADC
  - validation of stitching $\Rightarrow$ large surface sensors
  - validation of 2-sided ladder concept with 0.4% X_0
  - validation of unsupported 0.15% X_0 ladder concept
  - exploration of $\leq$ 0.18 μm CMOS technologies
- **2013 :**
  - switch to 0.18 μm technology $\Rightarrow$ expect $\sim$ 10 μs r.o. time, O(10) MRad tolerance
  - validation of 2-sided ladder concept with 0.3% X_0
  - exploration of $<$ 0.18 μm CMOS technologies

3DIT to achieve Ultimate CMOS Sensor Performances

- **3D Integration Techno.** allow integrating high density signal processing μcircuits inside small pixels
- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - ⁂ combine different fabrication processes
  - ⁂ alleviate constraints on transistor type inside pixel
- **Split signal collection & processing functionnalities using optimal technology in each tier :**
  - ⁂ Tier-1 : epitaxy (depleted or not), deep N-well ?
  - ⁂ Tier-2 : analog, low I_{leak}, process (nb of ML)
  - ⁂ Tier-3 (& -4) : digital VDSM process (nb of ML),
    $\rightarrowtail$ fast laser (VOCSEL) driver, etc.

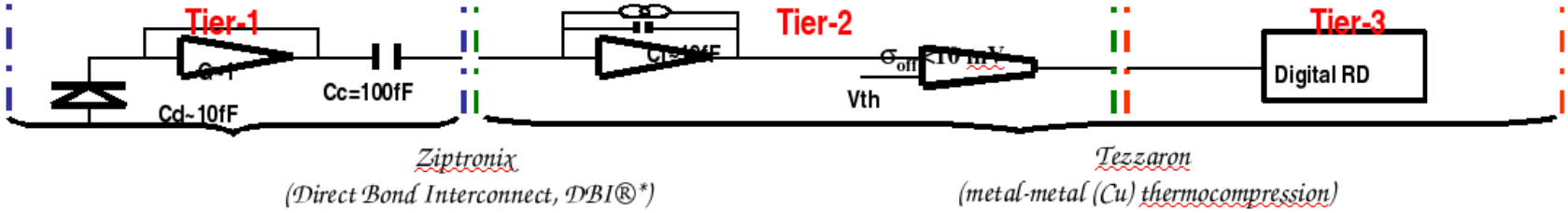


Conventional MAPS 4 Pixel Layout 3D 4 Pixel Layout

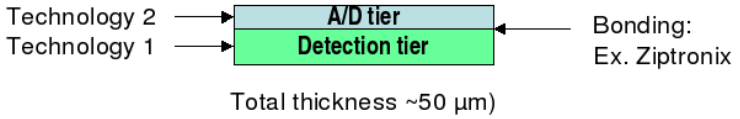
- **The path to nominal exploitation of CMOS pixel potential :**
  - ⁂ fully depleted 10-20 μm thick epitaxy $\Rrightarrow$ $\lesssim$ 5 ns collection time, rad. hardness $>$ Hybrid Pix. Sensors ???
  - ⁂ FEE with $\leq$ 10 ns time resolution $\rightarrowtail$ solution for CLIC & HL-LHC specifications ???
- **Devt of** CAIRN $\equiv$ **C**MOS **A**ctive pixel sensors with vertically **I**ntegrated **R**ead-out and **N**etworking functionnalities
  $\hookrightarrow$ 1st set of 4 chips submitted to foundry in Spring 2009 (within 3DIC)

3D Sensor: Towards a High Resistivity Sensing Tier

- **Combine 0.13μm 2-tier process with 0.35μm high-resistivity EPI process**



- DBI ≡ Direct Bond Interconnect : low temperature CMOS compatible direct oxide bonding with scalable interconnect for highest density 3D interconnections ($\leq$ 1 μm pitch, $>$ 10^8/cm^2 possible)



✳ **Tier-1 :**

- ◇ fully depleted $\Rrightarrow$ fast charge collection ($\sim$ 5 ns) $\longrightarrow$ radiation tolerant
- ◇ for small pitch, charge contained in only few pixels
- ◇ sufficient S/N ratio defined by the 1st stage
- ◇ "charge amplification" ($>$ factor 10) by capacitive coupling of the 1st to the 2nd stage

✳ **Tier-2 :**

- ◇ single stage, high gain, folded cascode based charge amplifier, with current source in the feedback loop
  $\Rrightarrow$ shaping time $\sim$ 200 ns for the sake of time resolution
- ◇ small offset, continous discriminator

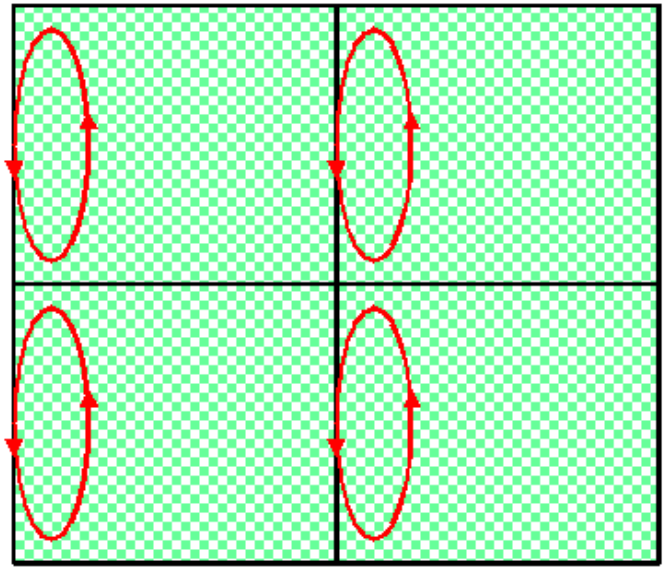
✳ **Tier-3 :**

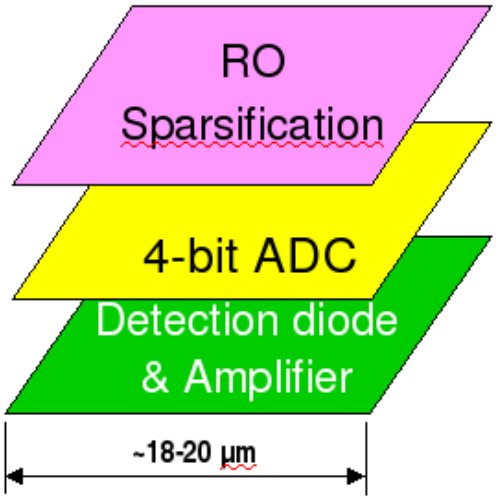
- ◇ matrix of 256$\times$256 pixels $\Rrightarrow$ 2 μs read-out time

- **1st prototype (with 1-bit ADC) submitted in Spring '09 $\longrightarrow$ still expected back ...**

Fast 3D Sensor with Reduced Power Consumption

- **CMOS sensors with fast pipeline digital r.o. $\Rrightarrow$ minimise power consumption :**
  - ⁕ Subdivide sensitive area in ”small” arrays running individually in rolling shutter mode
  - ⁕ Adapt the number of raws to required frame r.o. time
    - $\Rrightarrow$ few μs r.o. time achievable
  - ⁕ Design fitting 20$\times$20 μm^2 :
    - ◇ Tier-1: sensor & pre-amplifier (G $\sim$ 500 $\mu V/e^-$)
    - ◇ Tier-2: 4-bit pixel-level ADC with offset cancellation circuitry (LSB $\sim$ N) $\lesssim$ 2 μm resolution
    - ◇ Tier-3: fast pipeline read-out with integrated data sparsification





- **1st prototype (with 1-bit ADC) submitted in Spring ’09 $\rightarrowtail$ still expected back ...**

R&D Road Map for Long-Term : 3D Sensors

- **2011-2012 :**
  - proof of principle of heterogeneous CMOS sensor concept:
    connection of 0.35 μm high-res sensing tier to 0.13 μm 2-tier r.o. chip (within AIDA)
  - exploration of $\lesssim$ 0.1 μm CMOS technologies
  - exploration of connection and thinning techniques
- **2013-2014 :**
  - validation of architecture allowing for $\lesssim$ O(μs) r.o. time
  - R&D on radiation tolerance
  - exploration of $\lesssim$ 0.1 μm CMOS technologies
  - exploration of connection and thinning techniques
- **2015-2016 :**
  - validation of 1st full size thin and fast sensor adapted to experimental specifications (e.g. CBM-MVD)
  - start designing dedicated sensors exploiting the concept developed

- Towards Light Pixelated Systems adapted to a SuperB Factory

- **Synergies with SuperB oriented devts : sensors and pixelated systems**

- **Exploit concept of double-sided ladders to fill space between SVT & beam pipe:**
  - ⁂ 1 or 2 layers (replacing SVT inner layer) ?
  - ⁂ complete with unsupported ladder on beam pipe ? (optimistic !)

- **Synergy with the development of 3 generations of sensors :**
  - ⁂ 1st generation : 2D sensor in 0.35 μm high-res techno. (prototyping completed $\lesssim$ 2013)
    - ▷ MIMOSA-26 like architecture with 50 μm pitch with 10–15 μs r.o. time
  - ⁂ 2nd generation : 2D sensor in 0.18 μm triple well, high-res, techno. (prototyping completed $\lesssim$ 2015)
    - ▷ new architecture expected to allow for a few μs r.o. time and $>$ 10 MRad tolerance
  - ⁂ 3rd generation : 3D sensor combing 0.18 μm high-res sensitive tier with $\leq$ 0.13 μm 2-tier r.o. chip (prototyping completed $\lesssim$ 2017)
    - ▷ architecture expected to allow for $<$ 1 μs r.o. time and very high data flow

SUMMARY

- **CMOS sensor technology is mature for high performance vertexing but its full potential is still far from being exploited (despite improvement generated by high-res epitaxial layer processes)**
  - $\Rightarrow$ explore $\leq$ 0.18 μm, high-res, multi-well manufacturing technologies

- **CMOS pixels equipping a double-sided ladder seem to provide an attractive perspective for the SuperB vertex detector innermost layer(s?)**

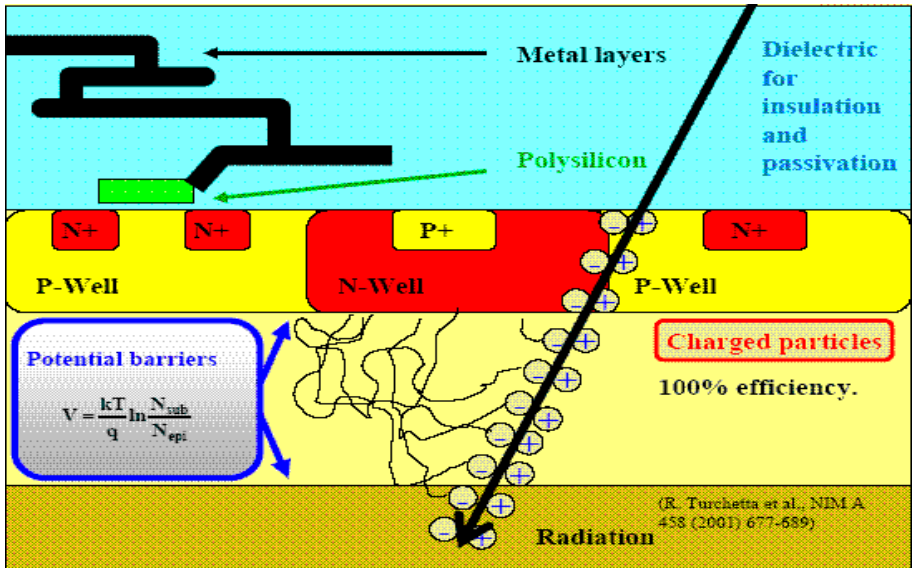
- **R&D at IPHC addresses 3 sensor generations, featuring increasing performance levels**
  - $\Rightarrow$ may be worth assessing the merit of each of them for the SuperB program

- **3D chips are the most promising, but there is a long way to go**
  - $\Rightarrow$ keep pushing 2D sensor approach to its best

- **R&D at IPHC may bring valuable contributions to the Layer-0 project**
  - $\Rightarrow$ exploit the synergy with INFN

Reminder: Main Features of CMOS Sensors

- P-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000$ e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)



- Prominent advantages of CMOS sensors:
  - ◇ granularity: pixels of $\lesssim 10 \times 10$ $\mu m^2 \Rrightarrow$ high spatial resolution
  - ◇ low mat. budget: sensitive volume $\sim$ 10 - 20 $\mu m \Rrightarrow$ total thickness $\lesssim 50$ μm
  - ◇ signal processing μcircuits integrated in the sensors $\Rrightarrow$ compacity, high data throughput, flexibility, etc.
  - ◇ other attractive aspects: cost, multi-project run frequency, T_{room} operation, etc.

$\triangleright \triangleright \triangleright$ Thinning down to ~ 30 μm permitted

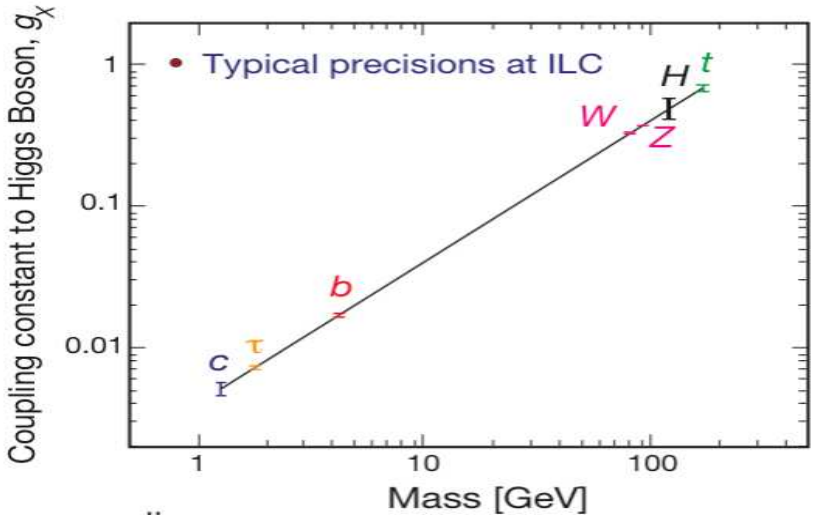
The Trend for Ultra-Light Pixelated Devices

- **Trend of subatomic physics experiments for highly granular and thin pixel devices**
- **Central motivation :**
  - ⁂ high performance reconstruction of (displaced) charm vertices
  - ⁂ high performance multi-jet final state flavour tagging ($t\bar{t}$, $t\bar{t}H$, AH, ...)
- **Flagship of this trend : International Linear Collider (ILC)** $\longmapsto$ Letters of Intent delivered in 2009
  $\hookrightarrow$ Detector Baseline Document ($\simeq$ TDR) to be delivered by 2012
  - ⁂ also: Heavy Ion experiments, CLIC, LHC upgrades, ..., hadrontherapy, ...

$\hookrightarrow$ Figure of merit : $\sigma_{\mathbf{ip}} = \mathbf{a} \oplus \mathbf{b}/\mathbf{p} \cdot \sin^{\mathbf{3/2}} \theta$

⁂ $\mathbf{a}$ governs high momentum ⁂ $\mathbf{b}$ governs low momentum ($\sim$ 30 % particles $<$ 1 GeV/c)

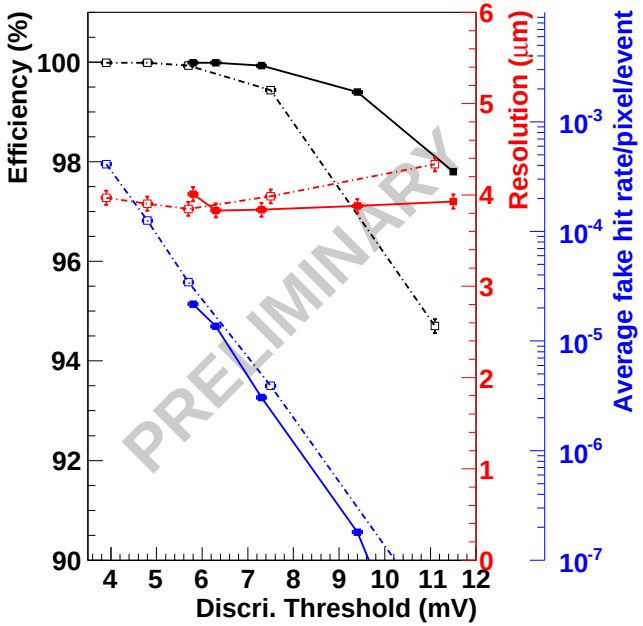
Accelerator	$\mathbf{a}$ (μm)	$\mathbf{b}$ ($\mu m \cdot GeV$)
LEP	*25*	*70*
SLD	*8*	*33*
LHC	*12*	*70*
RHIC-II	12	19
ILC	< 5	< 10



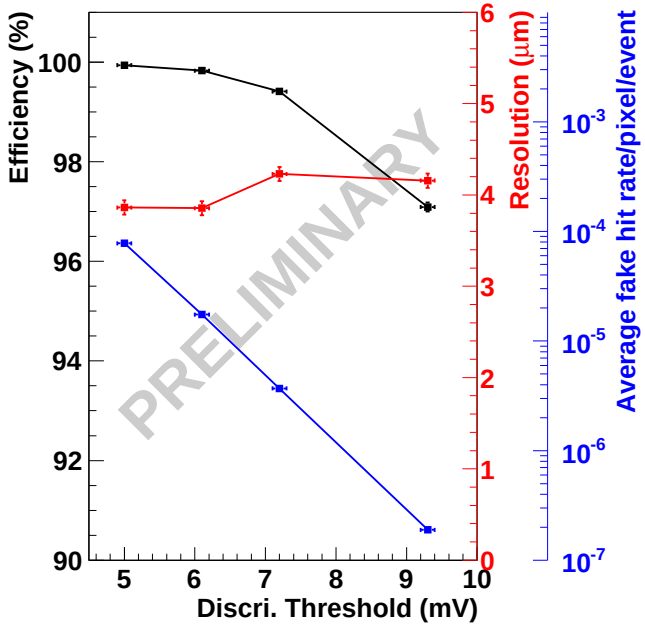
Back-Up: MIMOSA Sensors Performances

▷▷▷ Impact of $1{\cdot}10^{13}$ n_{eq}/cm^2 on detection performances at $T_{op} \sim 0^{\circ}C$

Mi26 HR-15 and HR-10 Efficiency, Fake rate and Resolution



Mi26 HR-15 Efficiency, Fake rate and Resolution
for a chip irradiated with a $1.10^{13}N_{eq}$ dose at T_{op} ~ 0° C



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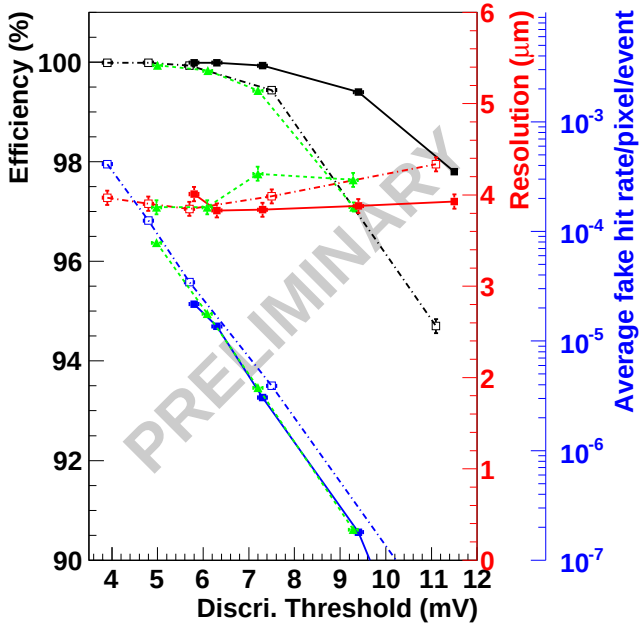


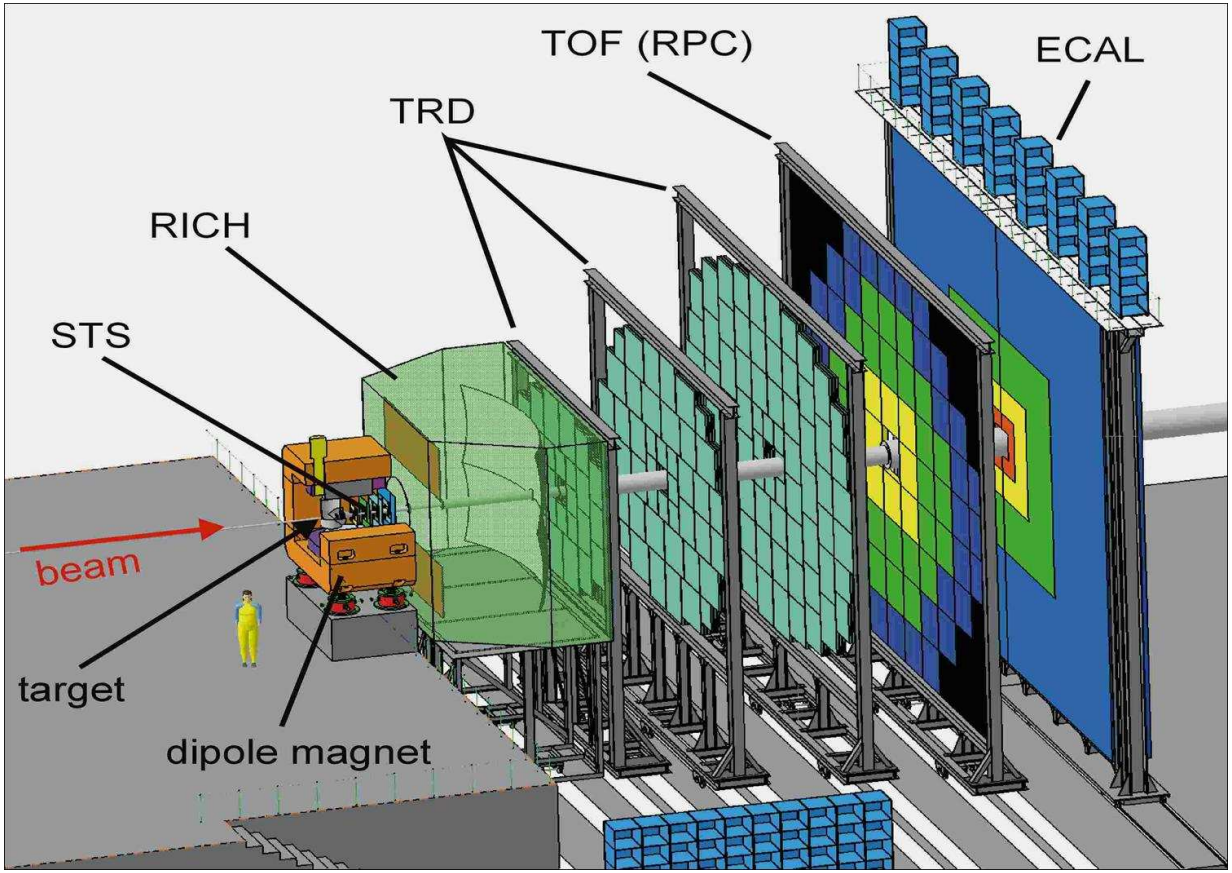
- **Preliminary conclusions:**
  - ⁂ det. eff. $\sim$ 100 % for very low fake rate: HR-15 ▷ plateau until fake rate of few 10^{-6}
  - ⁂ single point resolution $\lesssim 4\ \mu m$
  - ⁂ det.eff. of HR-15 still $\sim$ 100 % after exposure to $1{\cdot}10^{13}$ n_{eq}/cm^2

⇒ **Striking evidence for performance improvment with HR epitaxy (in particular 15 μm thick)**

Back-Up : Application of CMOS Sensors to CBM Experiment

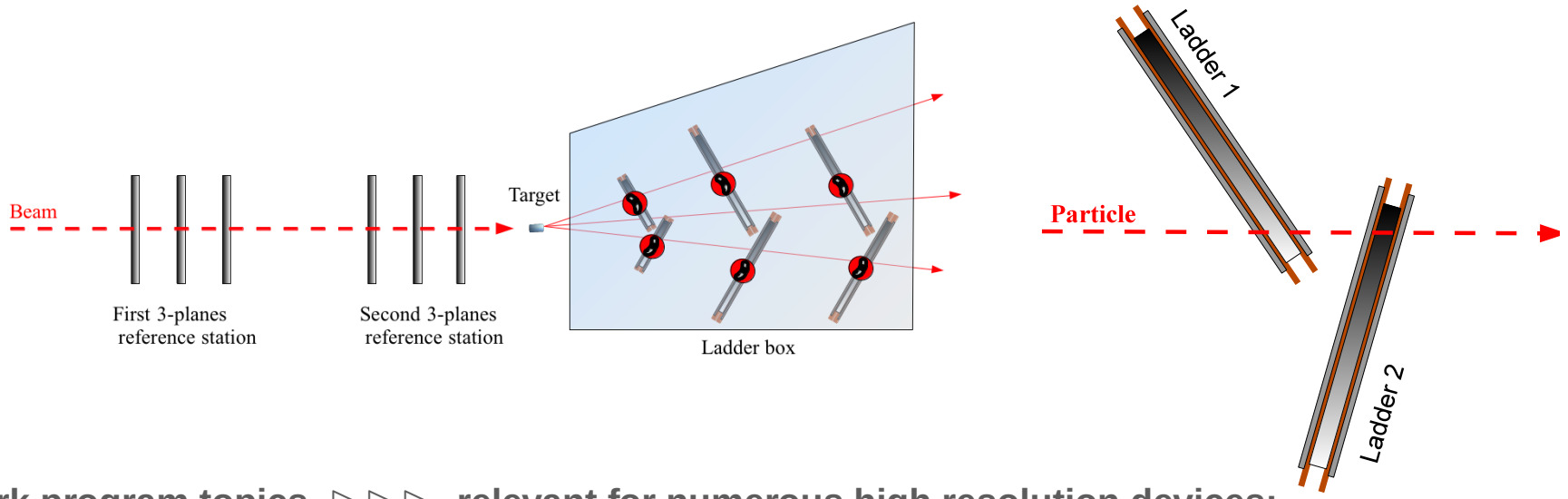
- **Cold Baryonic Matter (CBM) experiment at FAIR:**
  - Micro-Vertex Detector (MVD) made of 2 of 3 stations located behind fixed target
  - double-sided stations equipped with CMOS pixel sensors)
  - operation a negative temperature in vacuum
  - each station accounts for $\lesssim$ 0.5 % X_0
  - sensor architecture close to ILC version

- **Most demanding requirements :**
  - ultimately ($\sim$ 2020): 3D sensor
    $\lesssim$ 10 μs, $>$ 10^{14} n_{eq}/cm^2, $\gtrsim$ 30 MRad
  - intermediate steps: 2D sensors
    $\lesssim$ 30-40 μs, $>$ 10^{13} n_{eq}/cm^2, $\gtrsim$ 3 MRad
  - 1st sensor for SIS-100 (data taking $\sim$ 2016)



Back-Up: VTX Oriented Infrastructures in AIDA

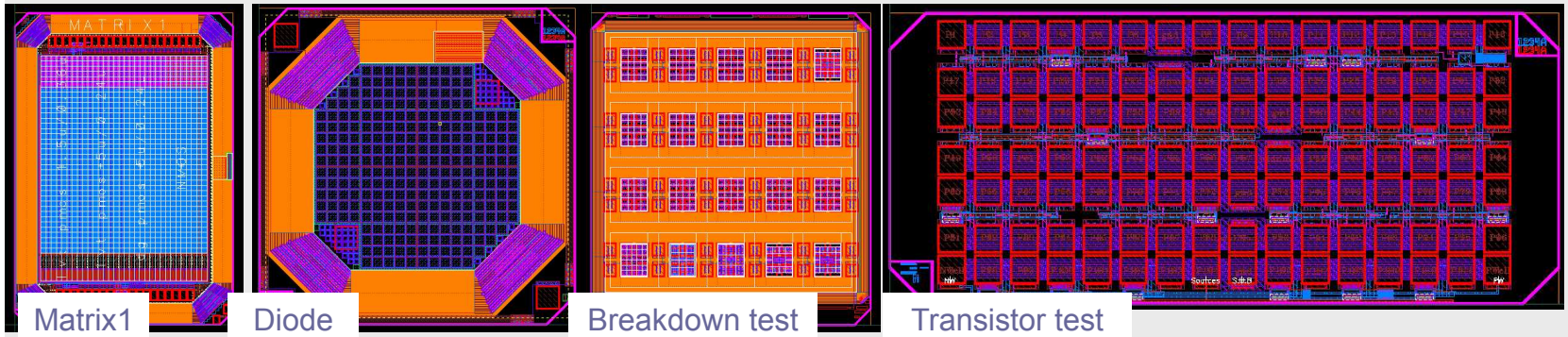
- AIDA $\equiv$ EU FP-7 Integrated Infrastructure project : approved $\rightarrowtail$ starts Feb. 2011
- **On-beam (CERN-SPS) test infrastructure:**
  - Large Area beam Telescope (LAT) $\longrightarrow$ 5×5 cm^2 stitched sensors
  - Alignment Investigation Devices (AID):
    - box hosting pairs of ladders (e.g. PLUME) and unsupported pixelated systems (SERWIETE)
    - box front panel contains removable target



- **Work program topics $\triangleright\triangleright\triangleright$ relevant for numerous high resolution devices:**
  - alignment capabilities: dedicated equipment and particle tracks
  - vertex reconstruction accuracy
  - track reconstruction with different devices (high spatial resolution combined with fast detectors)

LePIX: monolithic detectors in advanced CMOS

- Submission for fabrication just finalized
  - Several issues: ESD, special layers and mask generation, guard rings
  - Still need to discuss some outstanding fabrication issues with IBM
- 7 chips submitted :
  - 4 test matrices
  - 1 diode for radiation tolerance
  - 1 breakdown test structure
  - 1 transistor test: already submitted once in test submission
- Will require very significant testing effort for which we need to prepare (measurement setup, test cards…)



Matrix1 Diode Breakdown test Transistor test

W. Snoeys, CERN-ESE-ME, 2010