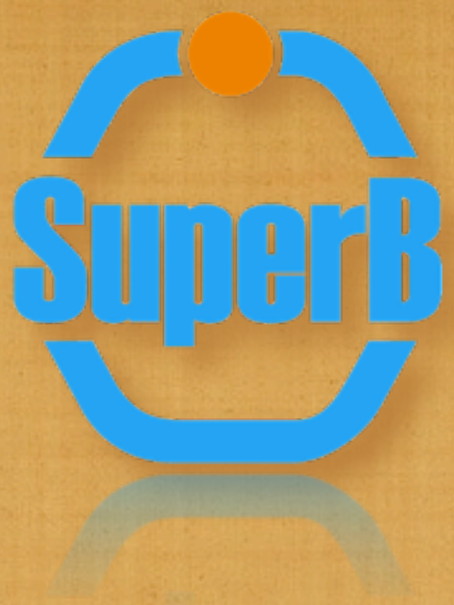



# Detector Status

Francesco Forti, INFN and University of PISA

SuperB Workshop XIV

Frascati, 27/9 - 1/10, 2010


# Outline

## White Paper

## Budget

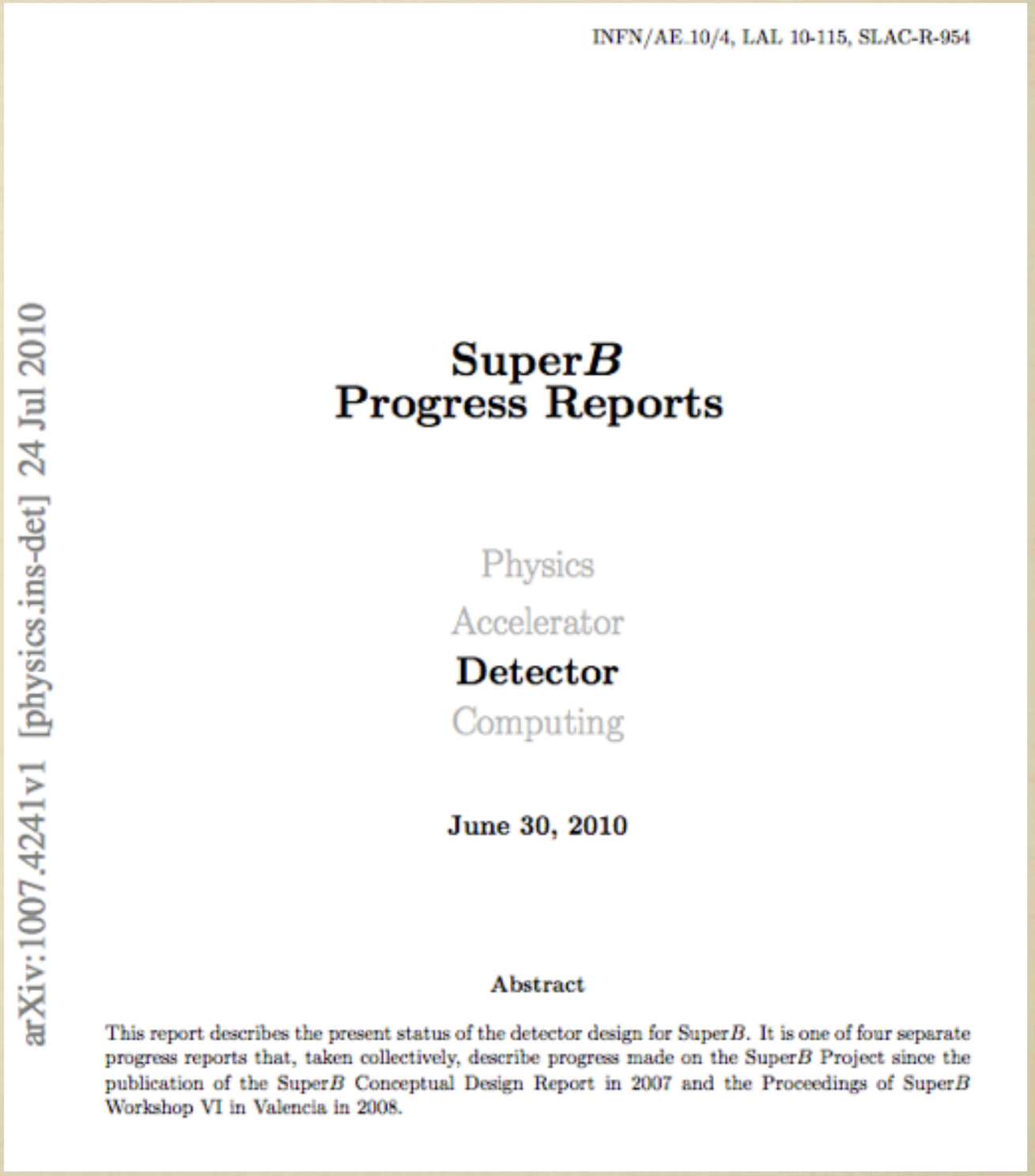
## Geometry

## Subsystems

## Workshop

# White paper is finished

- Too many people to thank to list
- Detector Progress Report: arxiv.org/abs/1007.4241
- 230 signatures
- 40 Institutions
- 9 nations:
  - Italy, Norway, US, Canada, Ukraine, France, Russia, UK, Israel



INFN/AE.10/4, LAL 10-115, SLAC-R-954



SuperB
Progress Reports

Physics
Accelerator
**Detector**
Computing

**June 30, 2010**

**Abstract**

This report describes the present status of the detector design for SuperB. It is one of four separate progress reports that, taken collectively, describe progress made on the SuperB Project since the publication of the SuperB Conceptual Design Report in 2007 and the Proceedings of SuperB Workshop VI in Valencia in 2008.

# White Paper Budget

## CDR Budget

| Item | EDIA mm | Labor mm | M&S kEuro | Rep.Val. kEuro |
|---|---|---|---|---|
| Detector | 3391 | 1873 | 40747 | 46471 |

| WBS | Item | EDIA mm | Labor mm | M&S kEuro | Rep.Val. kEuro |
|---|---|---|---|---|---|
| 1 | SuperB detector | 4037 | 2422 | 52953 | 48922 |
| 1.0 | Interaction region | 21 | 12 | 860 | 0 |
| 1.1 | Tracker (SVT + Strip + MAPS) | 408 | 442 | 6444 | 0 |
| 1.2 | DCH | 165 | 139 | 3421 | 0 |
| 1.3 | PID | 116 | 236 | 5820 | 7138 |
| 1.4 | EMC | 219 | 360 | 12147 | 31574 |
| 1.5 | IFR | 37 | 184 | 1374 | 0 |
| 1.6 | Magnet | 93 | 59 | 3767 | 10210 |
| 1.7 | Electronics | 994 | 342 | 9234 | 0 |
| 1.8 | Online System | 912 | 24 | 2074 | 0 |
| 1.9 | Installation and integration | 353 | 624 | 7596 | 0 |
| 1.A | Project Management | 720 | 0 | 216 | 0 |

# Detector Geometry

- Detector Geometry Working Group done precious evaluation work
  - Matteo Rama, Achille Stocchi
- To be completed with higher statistics

## Detector Geometry Selection Taskforces

| | | |
|---|---|---|
| 6 Layer SVT | LO Striplets @ 1.6cm if background is acceptable as default. MAPS Option. Retain 5 Layer outer detector. | |
| SVT – DCH transition radius | ~> than 20 cm determined by beam element cryostats to allow easy installation | |
| Backward EMC | Inexpensive Veto device bringing 8-10% sensitivity improvements for B→$\tau\,\nu$. Low momentum PID via TOF? Technical Issues? | Bill Wisniewsky |
| Forward PID | Physics gains about 5% in B→K(*)$\nu\nu$. Somewhat larger gains for higher multiplicities<br>Open technical options/interactions with EMC | Hassan Jawahery |
| Absorber in IFR | Optimized layout. Plan to reuse yoke. Still need to resolve engineering questions. | |

## Start meeting this week

# Detector Geometry Selection Task Forces

**Charge to the SuperB Detector Geometry Selection Task Forces.**

**BR+FF, July 23, 2010**

Several of the options described for the SuperB detector in the Conceptual Design Report of 2007 have now been resolved. However, as indicated in the Detector Progress Report of June 30, 2010, two major options remain that have a large impact on the overall detector system geometry, and therefore prevent us from defining final subsystem envelopes. Specifically, these open options are:

1. whether to include a hadronic PID detector in the forward region, and
2. whether to include an EMC in the backward region

As we believe it is crucial to be able to define these regions soon, and in any case before the TDR, we have decided to appoint two Geometry Selection Task Forces (one for the forward region and one for the backward region) to broadly investigate all issues involved, and provide recommendations to the Techboard for final decisions.

These Task Force committees are called (1) The Forward Geometry Selection Task Force, led by Hassan Jawahery, and (2) The Backward Geometry Selection Task Force, led by Bill Wisniewski. The full memberships of the task forces are given below:

**Forward Geometry Selection Task Force:**
Hassan Jawahery, Chair
Matteo Rama
Brian Meadows
Pasquale Lubrano
Chris Hearty

**Backward Geometry Selection Task Force:**
Bill Wisniewski, Chair
Achille Stocchi
Steve Robertson
Gianluigi Cibinetto
Dave Aston

The committees should make their recommendations based on a wise balance between all competing factors. These factors include, but are not limited to:

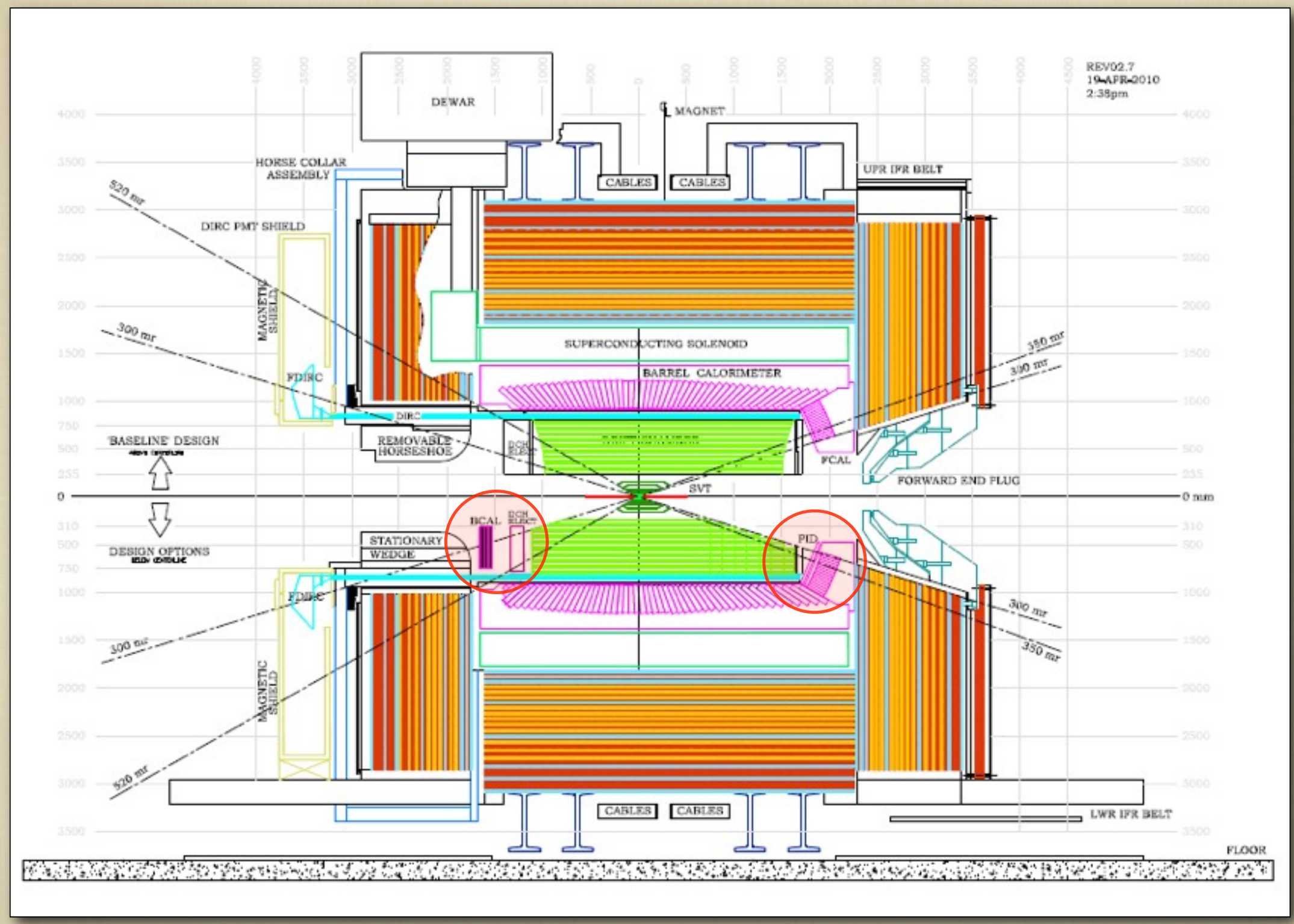
1. an evaluation of the physics impact of the inclusion of the device;
2. the impact of the material of the device on the performance of other subdetectors;
3. an evaluation of the technical performance of suggested devices, their maturity, the related risks, and the need for further R&D;
4. the impact on the overall detector structure and assembly procedures,
5. the cost of the device,
6. the manpower needed to build and operate the device, and
7. the strengths of the proponent groups.

The committees are expected to work closely with all interested parties. These will include (1) the Detector Geometry Working Group (DGWG) which has studied many of the physics tradeoffs associated with these open options, and will be able to provide higher statistics studies by the end of the summer; (2) the proponents for the differing technical solutions; (3) the sub-system leaders, and (4) the assembly, integration and management teams for the detector.

The precise methods that the committee chooses to employ in its review are within its purview. However, we would expect that the committees will request written material, hold review meetings with detector proponents, and, perhaps set specific review criteria for the proponents. These processes, including materials and reviews, are expected to be open to all SuperB members.

The selection task forces will present progress reports at Techboard meetings. Although the Tech Board is charged with the final decisions, the Task Forces should provide explicit recommendations to the Techboard, including their assessment of the physics impacts, costs, and risks of their preferred choice.

# Detector Geometry Options



# R&D and Engineeering Summary

| Sys | R&D | Engineering |
|---|---|---|
| SVT | Layer 0 thin pixels<br>Low mass mechanical support | Silicon strip layers<br>Readout architecture |
| DCH | High speed waveform digitizing<br>Cluster counting | CF mechanical structure<br>Gas speed, cell size |
| Barrel PID | Photon detection for quartz bars | Standoff box replacement |
| Forw PID | Time of flight option<br>Focusing RICH option | Mechanical integration.<br>Electronics |
| EMC | LYSO characterization<br>Light detection, Other crystals<br>Prototype Module Test | Readout electronics<br>Forward EMC mechanical support |
| IFR | SiPM performance<br>Prototype Module Test | Location of photo-detectors<br>Absorber thickness definition |
| ETD | High speed data link<br>Radiation hard devices | Trigger strategy<br>Bhabha rejection |

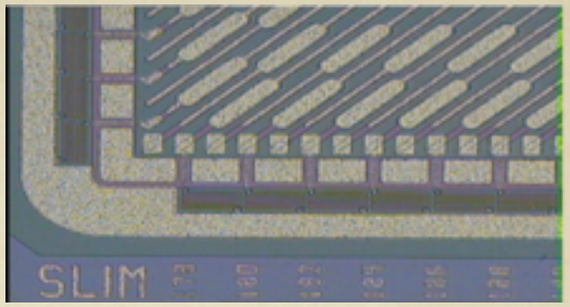
Giuliana Rizzo

SVT

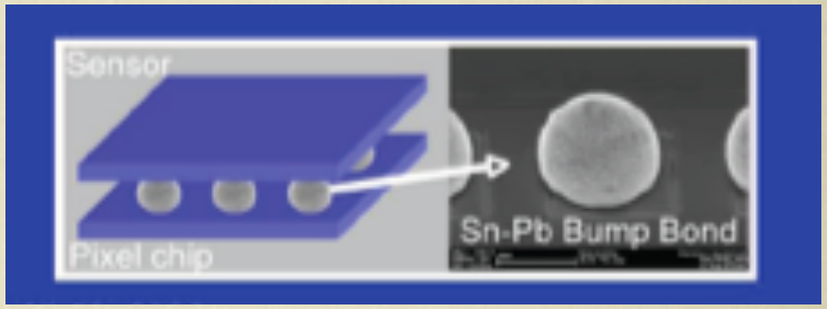
# SuperB SVT Layer 0 technology options

Complexity

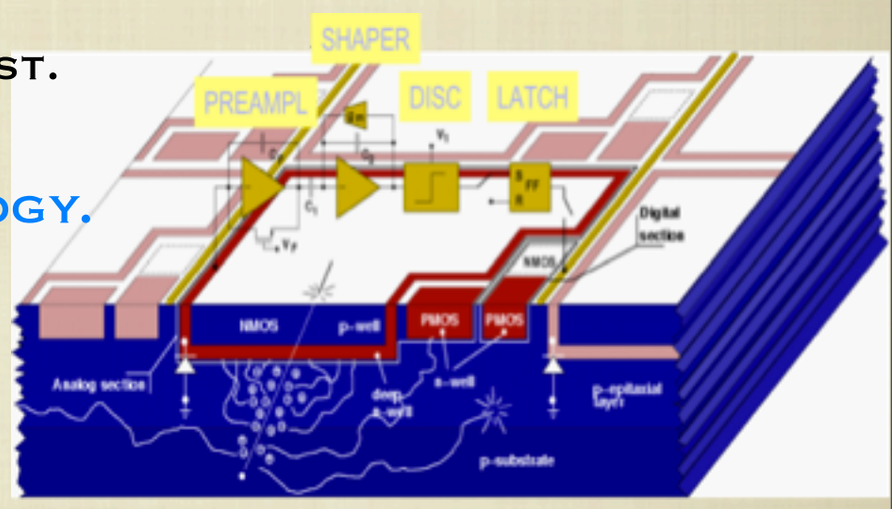
- **Striplets option:** mature technology, not so robust against background occupancy.
  - Marginal with back. track rate higher than ~ 5 MHz/cm²
  - Moderate R&D needed on module interconnection/mechanics/FE chip (FSSR2 or new chip)



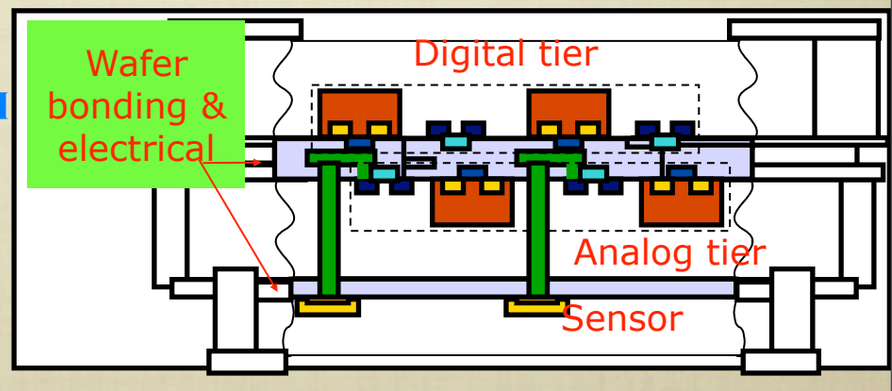

- **Hybrid Pixel option:** viable, although marginal.
  - Reduction of total material needed!
  - Reduction in the front-end pitch to 50x50 μm² with data push readout (developed for DNW MAPS)
    - FE prototype chip (4k pixel, ST 130 nm) now under test.




- **CMOS MAPS option:** new & challenging technology.
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm² with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams.

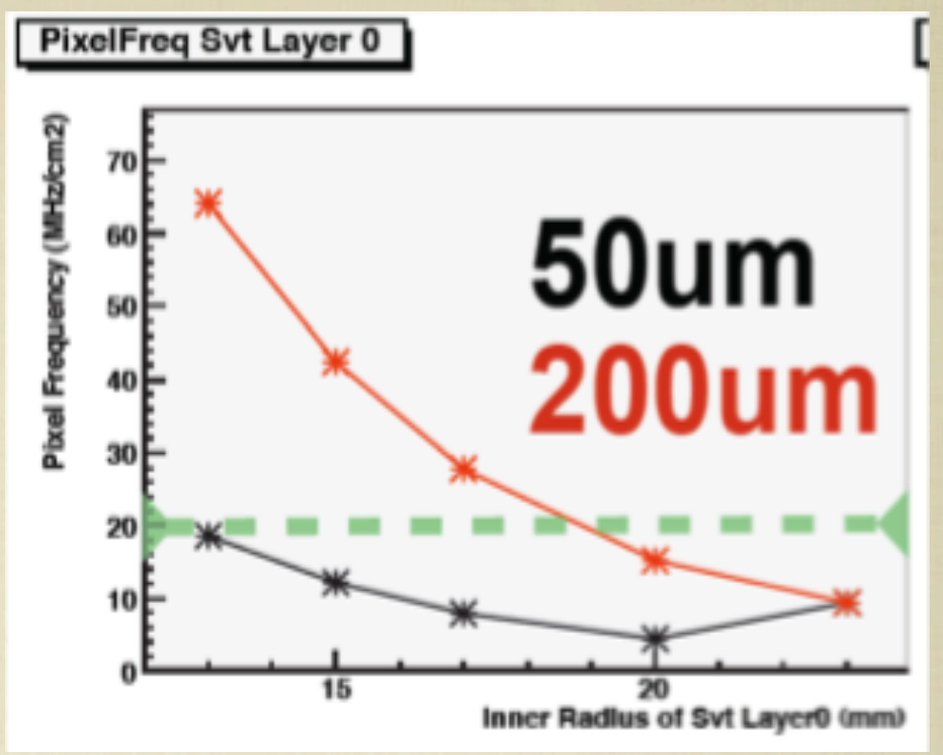



- **Thin pixels with Vertical Integration:** reduction of material and improved performance.
  - Two options are being pursued (VIPIX-Collaboration)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



# Readout chip for striplets/strips

- Recent update on back. Hit rate vs sensor thickness pushed the requirements on readout speed for striplets.
- Previous candidate chip (FSSR2) probably not fast enough (Verilog simulation ongoing)
  - Evaluate possible modification of digital part (FNAL) & use of alternative existing chip
  - Analog part should also be fast: sh. Time ~ 25 ns.
- New chip development might be needed!




- Readout needs for the external layers evaluated (L_strip=37 cm):
  - long shaping time ~0.4-1 us needed to get reasonable S/N. (20-26)
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- Started to investigate alternative options for long strip readout chip. Probably need to have triggered architecture.

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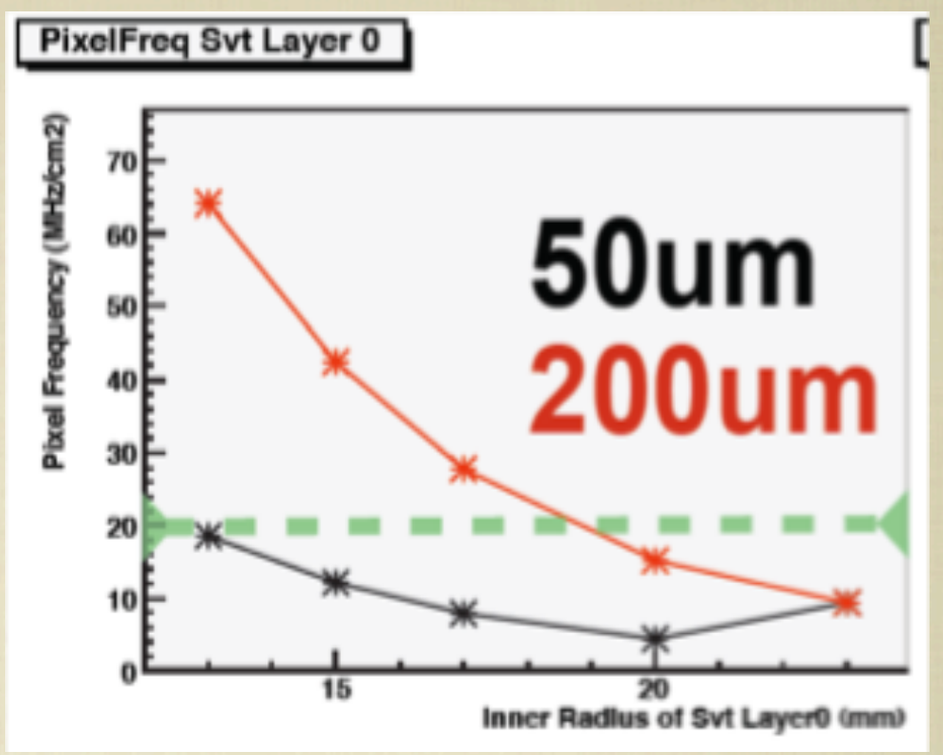


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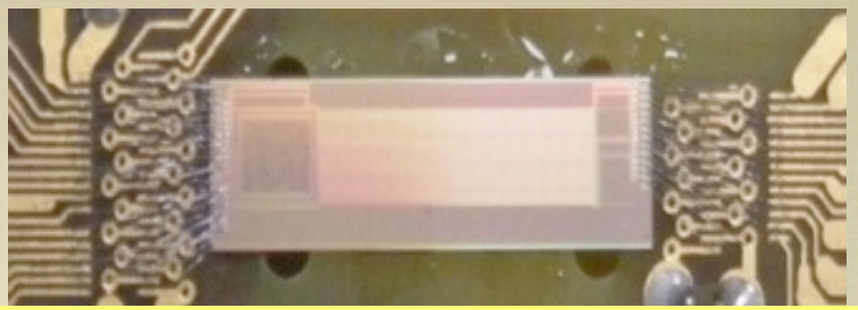
- Analog cell design should be redesigned for striplets and strips (PV)
- If need to design a new chip the involvement of new groups is mandatory for the digital part (Fermilab?)

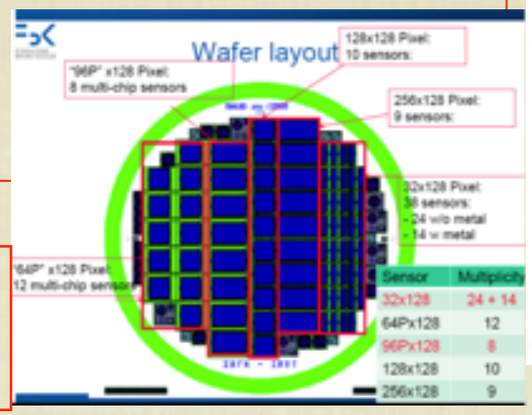
# R&D on pixels



- Front-end chip for hybrid pixel produced & tested before sensor interconnection
  - Data push readout architecture (100 MHz/cm2) VHDL readout efficiency > 98% @ 60 MHz
- Pixel sensor matrix (FBK)
  - tested with good quality

FE chip first results 32x128, 50 um pitch

| | post layout simul. | CHIP1 | CHIP2 | CHIP3 |
|---|---|---|---|---|
| baseline (mV) | 180 | 205.6 ± 0.5 | 211.2 ± 0.5 | 208.7 ± 0.5 |
| threshold dispersion (e-) | 350 | 490 ± 50 | 500 ± 50 | 450 ± 50 |
| ENC (e-) | 120 | 69 ± 2 | 59 ± 3 | 55 ± 2 |
| gain (mV/fC) | 45 | 41.6 ± 0.3 | 40.4 ± 0.3 | 39.3 ± 0.3 |



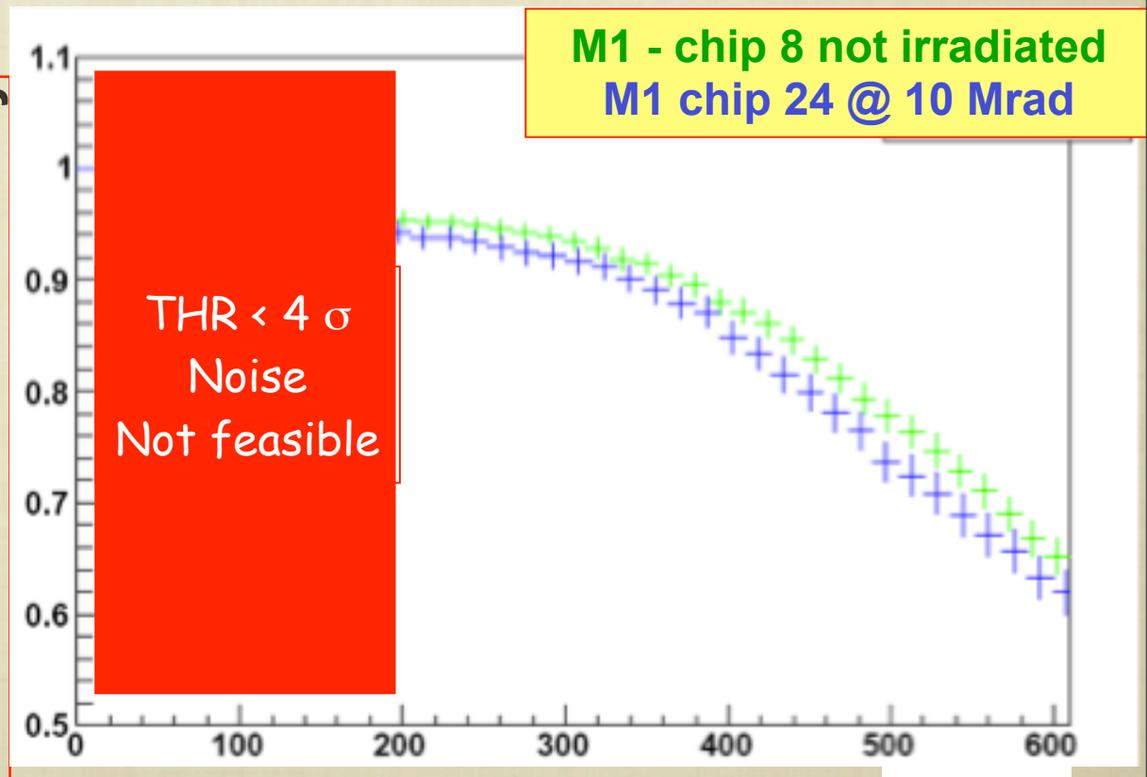

Bump-bonding @ IZM Berlin

test in lab.in Autumn

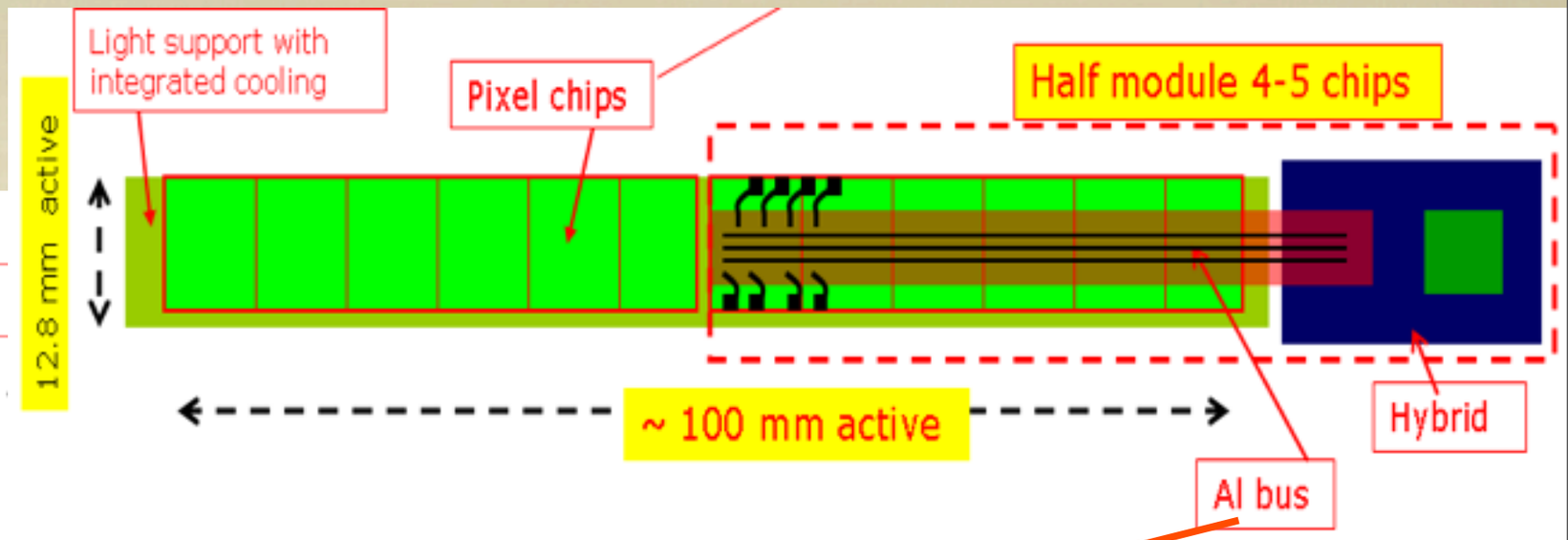
## CMOS MAPS (SLIM5&VIPIX):

- Single layer DNW MAPS well advanced:
  - 4k pixel matrix with data push readout succesfully tested with beams in 2008
  - New cell and irradiated DNW MAPS (10Mrad) tested with beams in 2009
- Improvements (collection efficiency & readout performance) with 3D MAPS:
  - vertical integration of 2 CMOS layers
  - First prototypes available in Sept
- Neutron irradiation performed

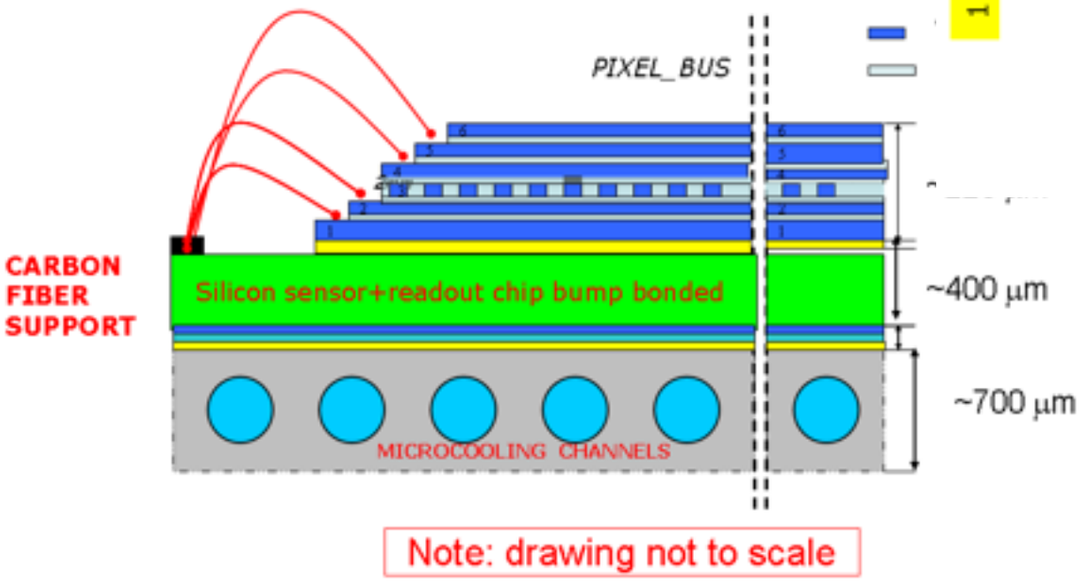
M1 - chip 8 not irradiated
M1 chip 24 @ 10 Mrad



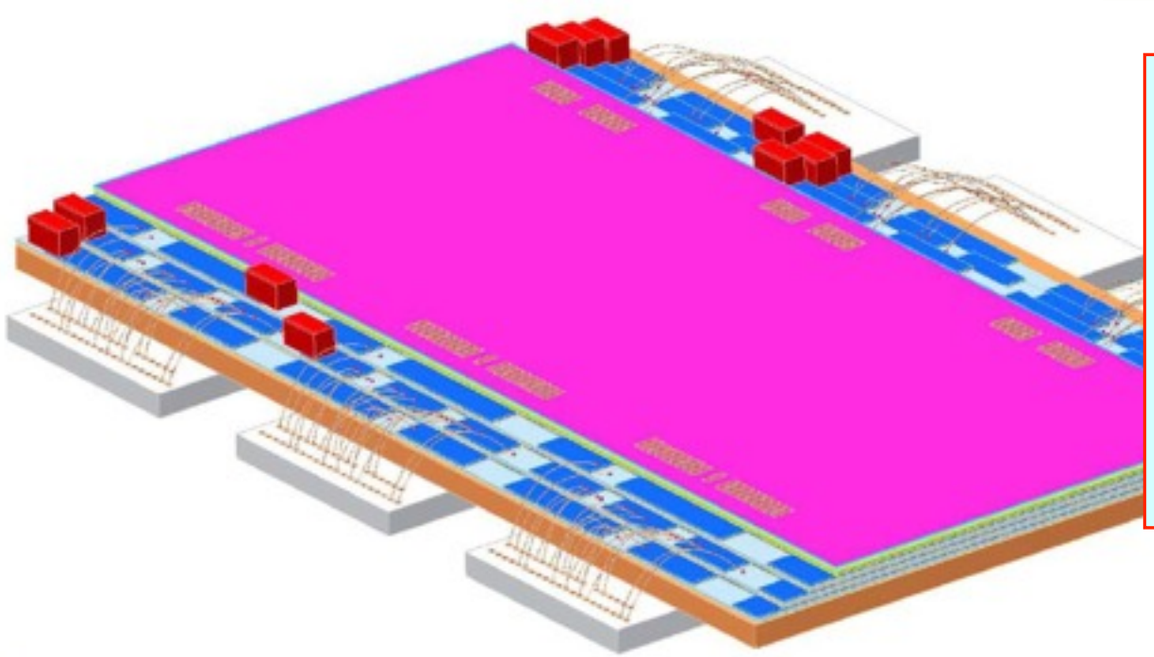
# LO Pixel Module




Layer0 module cross section




Note: drawing not to scale



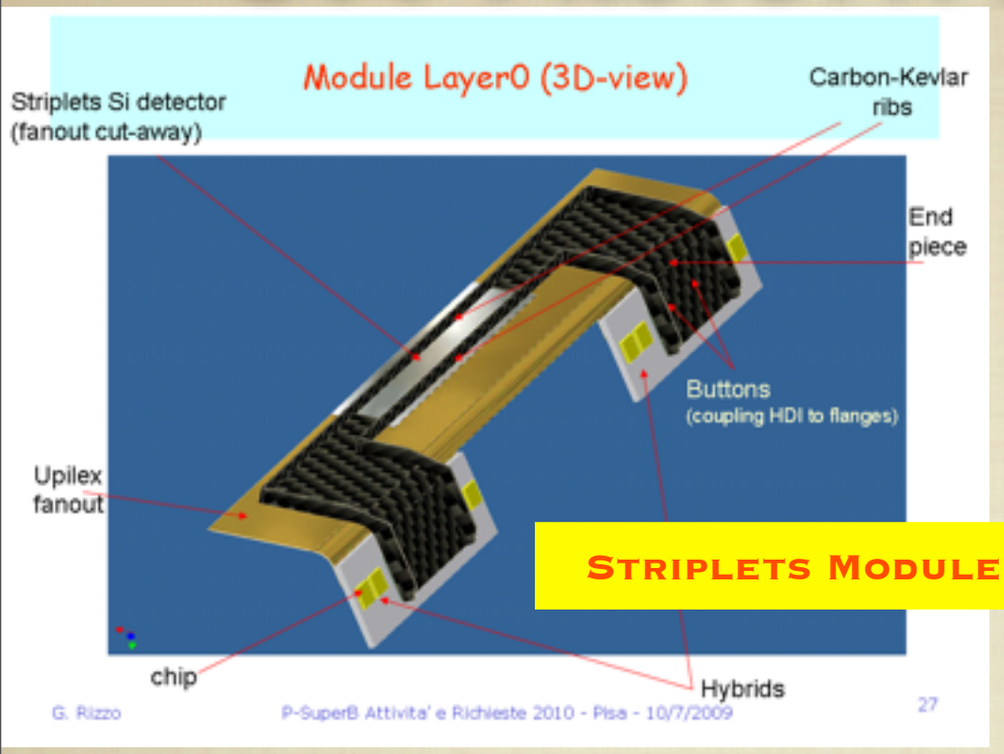
## Pixel Bus Protoype tested

- frequency response (signal up to 200 MHz, on individual lines) promising at full BUS lenght ~ 10 cm

## Prototype Pixel Module in 2010:

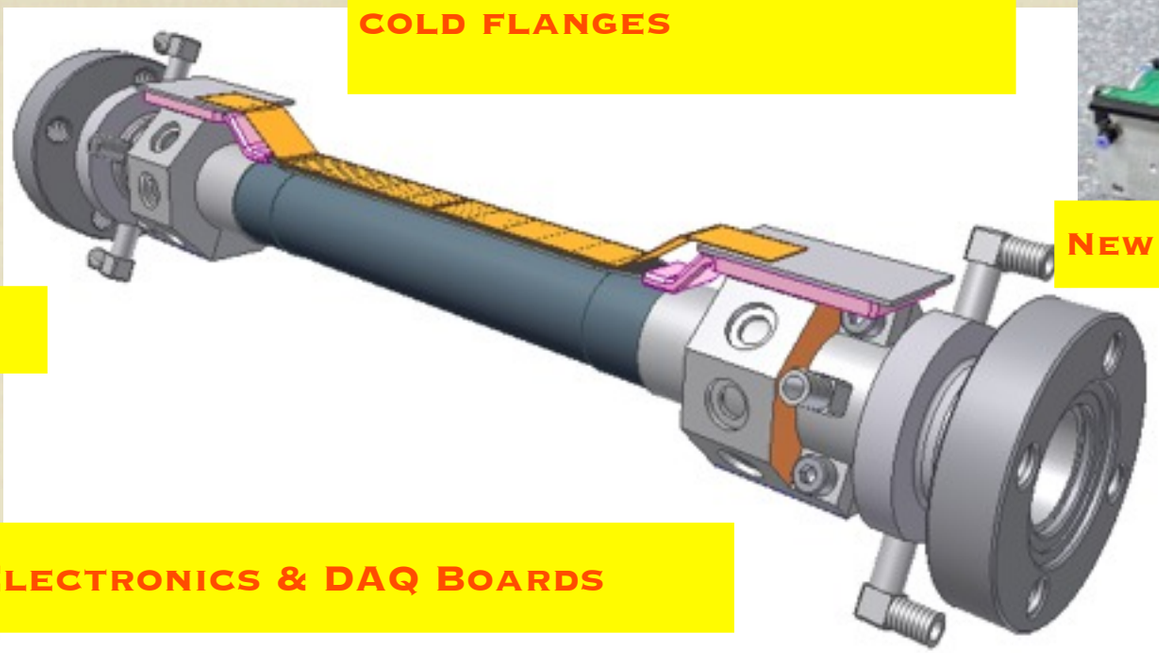
- 3 chips bump bonded on 1 sensor matrix + support with microchannel cooling + Al pixel BUS + testbaord:

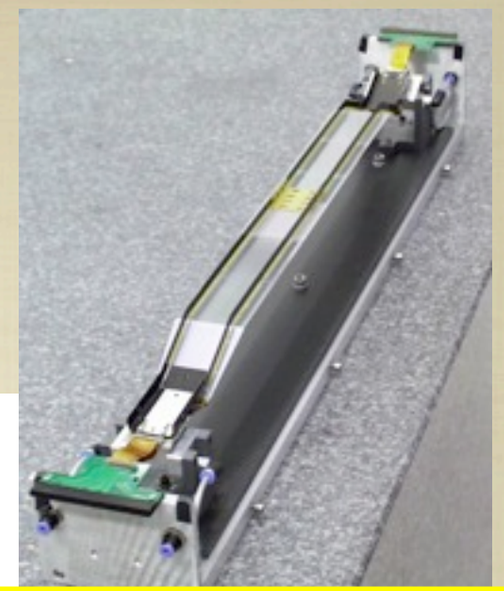
# SVT Prototypes in 2011




**Striplets Module**

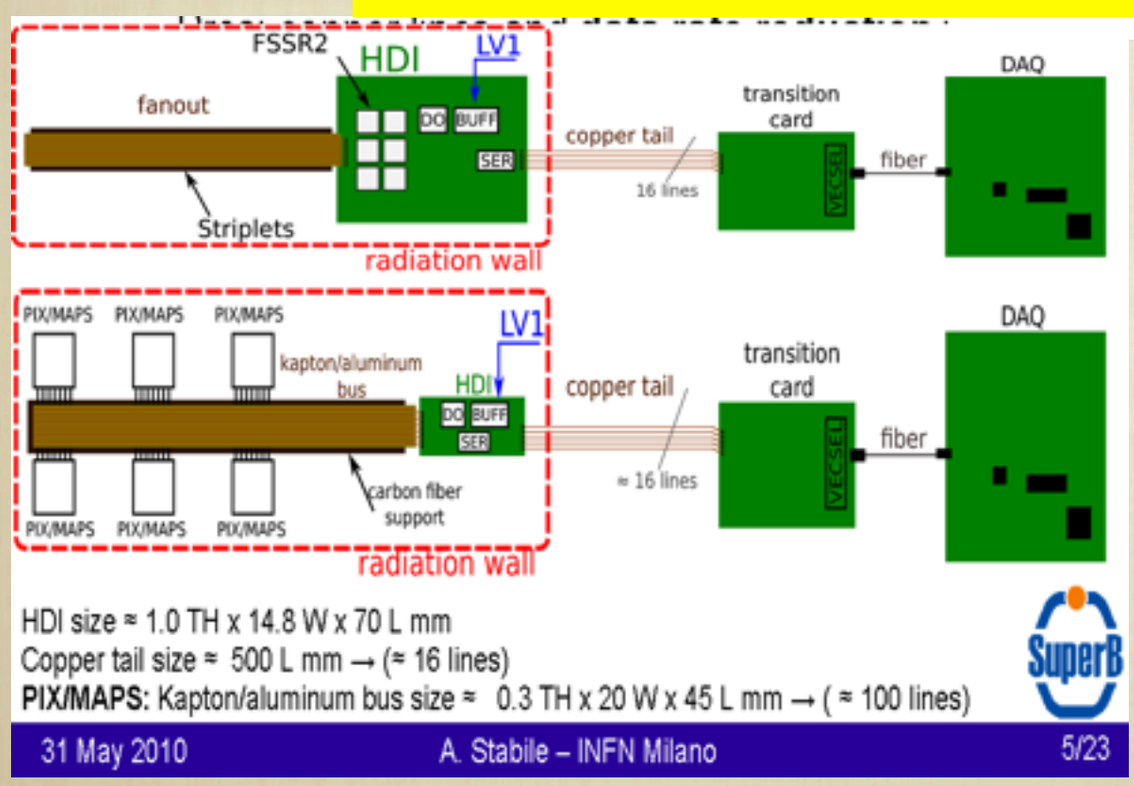
**Layer0 Pixel Module integrated with beam pipe cold flanges**

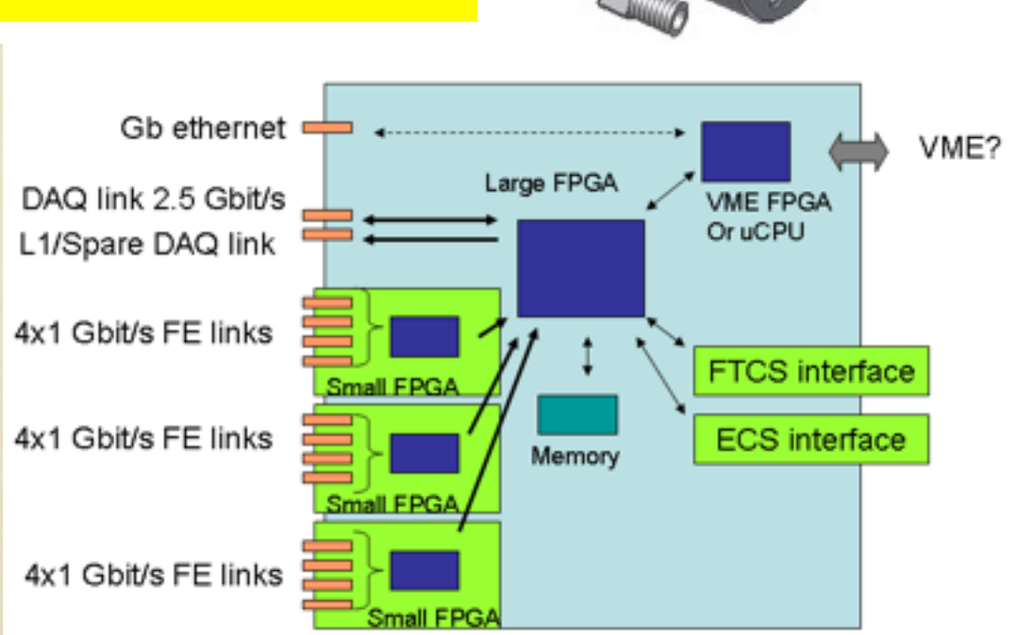




**New Arch Module**

**HDI- Off detector Electronics & DAQ Boards**



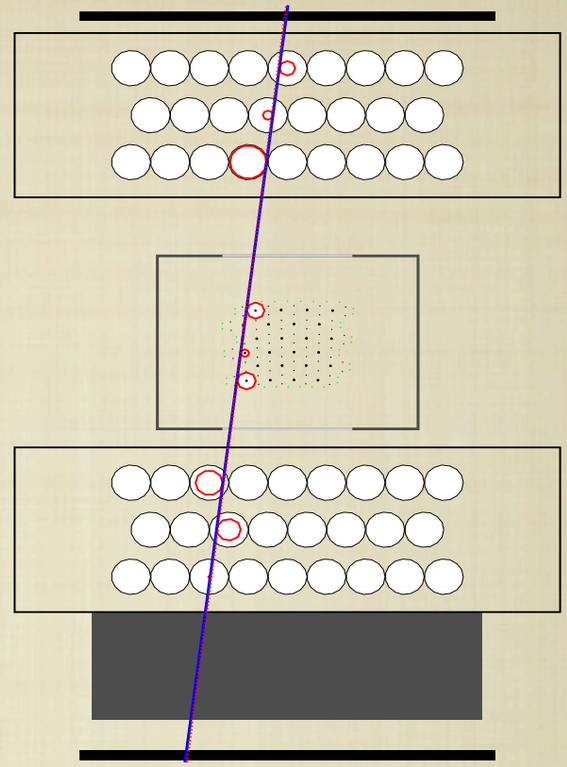



Giuseppe Finocchiaro
Mike Roney

DCH

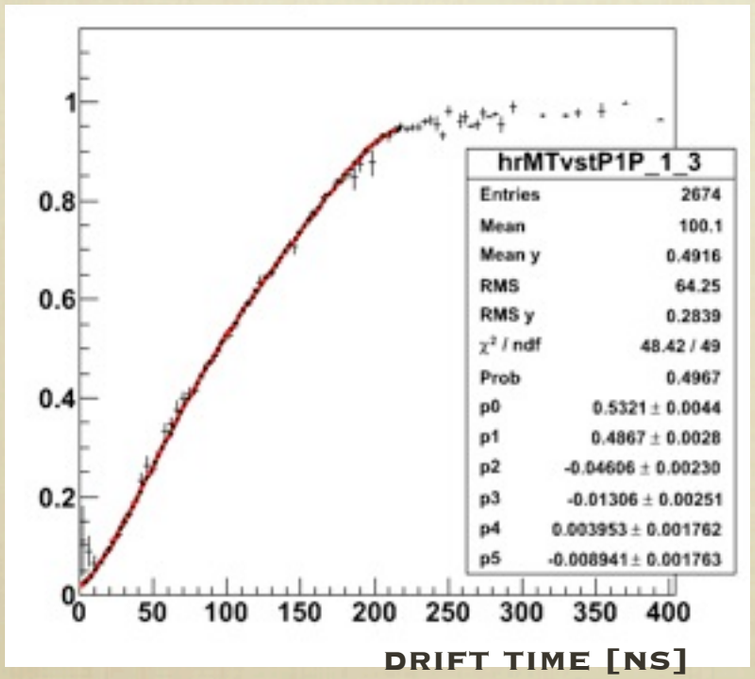
# Activity @ LNF: Prototype 1

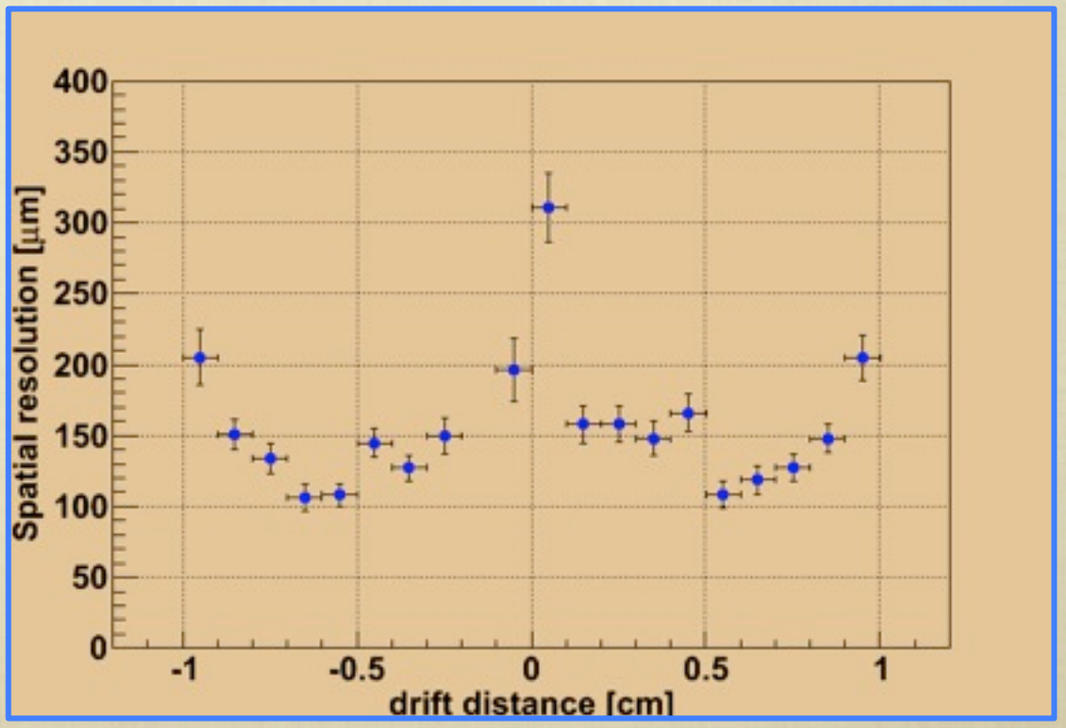
- Continuing cosmic ray data taking with "Proto 1"
  - 6x4 BaBar–like hex cells – external tracker with ~80μm extrapolation accuracy
- Campaign with He + various $iC_4H_{10}$ / $CH_4$ / $C_2H_6$ mixtures and HV / threshold settings



1. Example: 60%He-40%$C_2H_6$ gas mixture
   - blue (red) line: fit from external tracker (proto1) hits

2. Example: space-time relation fitted with 5-th order Chebichev polynomials + spatial resolution

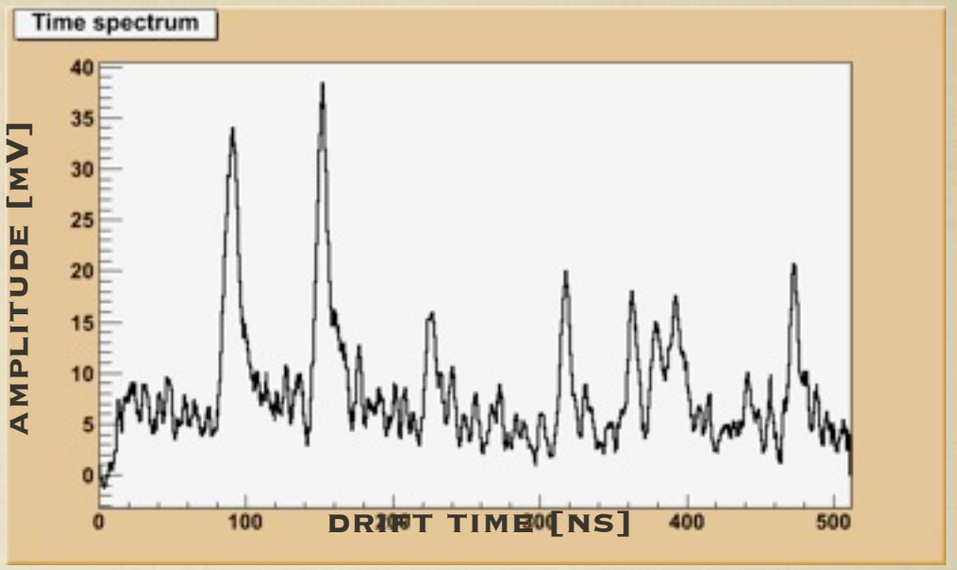


# Activity @ LNF: R&D and FEE

## R&D on cluster counting

- Two square drift tubes have been realized to study feasibility of cluster counting.
  - 24mm inner side, 400 and 1500 mm long
- 400mm tube instrumented with 300 MHz BW preamp, output signal read out with fast digitizer.
  - Studies on peak detection algorithms based on DSP techniques ongoing




## FEE ELECTRONICS

- Design and simulation of digital readout section - pipelines and concentrators - for standard solution (no-CC)
- Evaluating pros and cons of low-cost and well-consolidated 0.35um technology vs. 0.13um, more performing wrt. radiation hardness

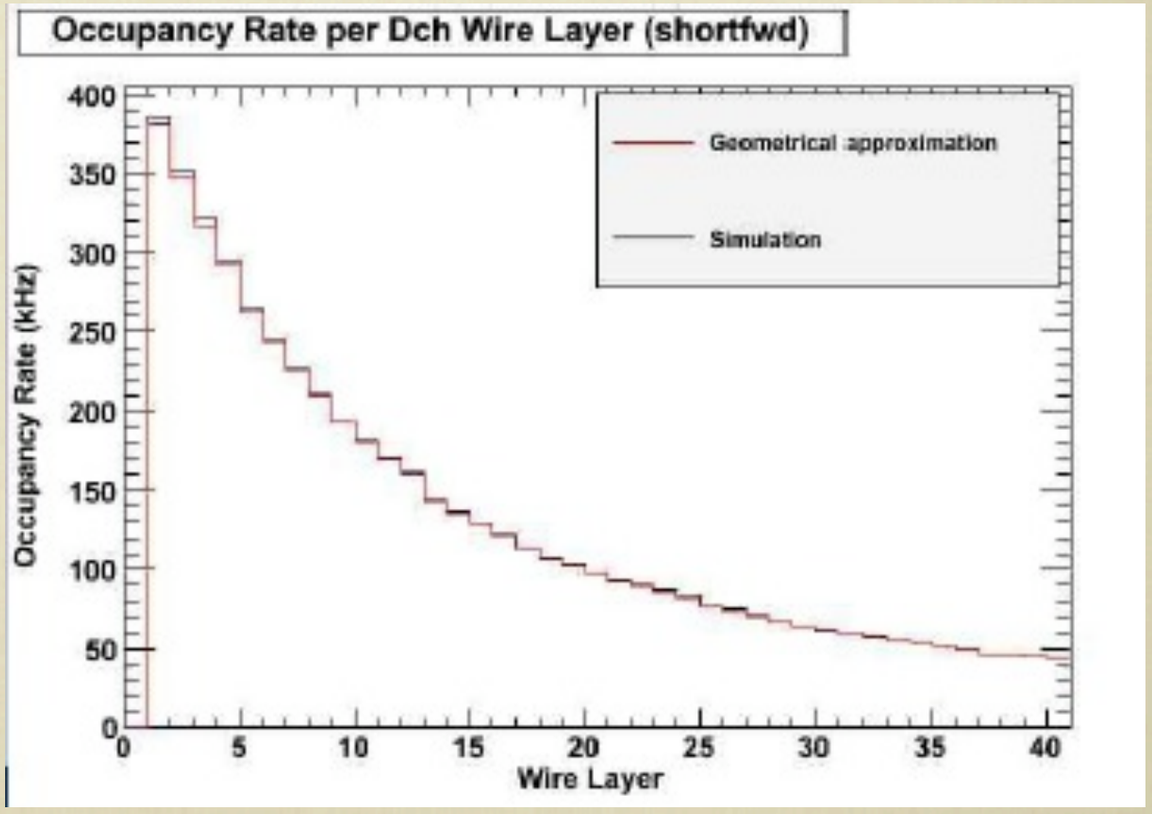
# Background&Geometry Studies at McGill

- Track efficiency and DCH occupancy studies using rare decay modes w/ tag reconstruction in full simulation.
  - Goal: to compare performance in various geometry models (e.g. table to right)

Table 2: Percentage (%) of B mesons with all tracks present

| Sample | flat | WC | spherical | shortShield | flat-unsh |
|---|---|---|---|---|---|
| $B^+B^-$ | 51.8 | 49.6944 | 51.0263 | 51.1053 | 58.2105 |
| $B^0\overline{B}^0$ | 45.125 | 43 | 43.65 | 32.55 | 50.475 |
| Benugam | 50.7797 | 50.2 | 50.1 | 49.7778 | 57.5556 |
| Bmnugam | 51 | 48.95 | 49.95 | 49.95 | 56.2105 |
| BKnunu | 50.8 | 49.2632 | 50.1053 | 50.1579 | 55.8947 |
| Ave | 49.9009 | 48.2215 | 48.9663 | 46.7082 | 55.6693 |

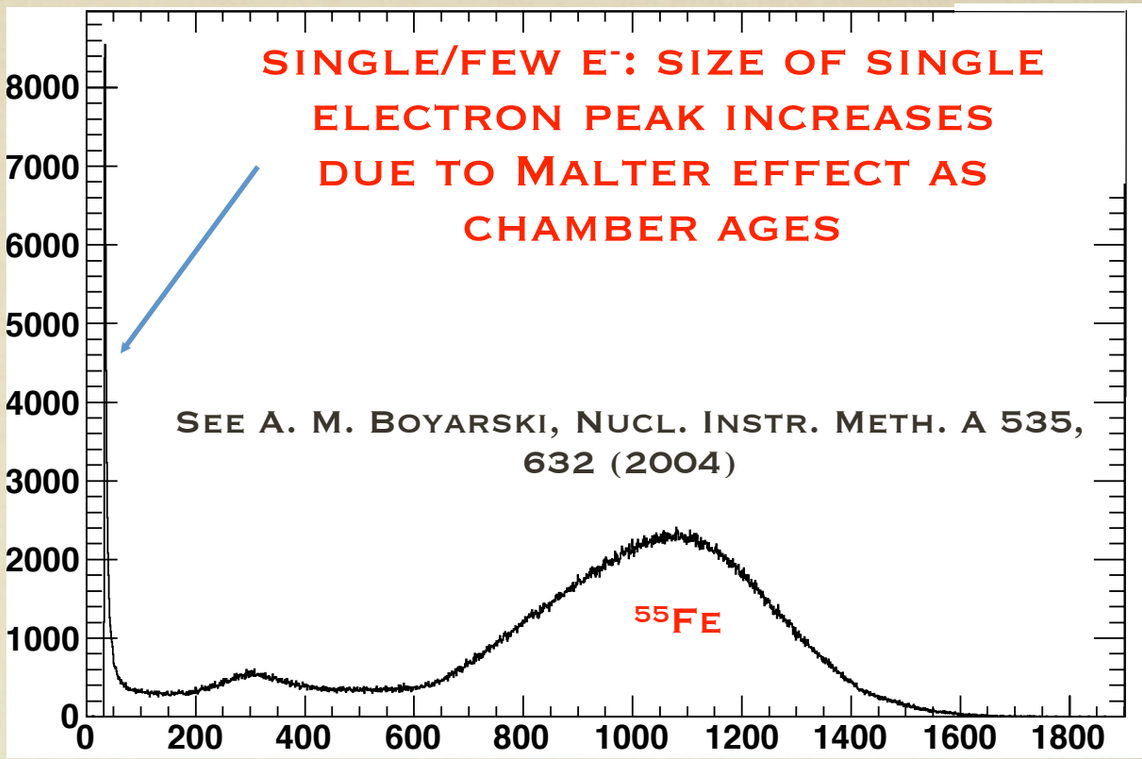
- Bhabha fast simulation studies of DCH occupancy in various geometry models.
  - Goal: validation of FastSim by comparing rate prediction with a "back of the envelope" geometrical approximation - gets good agreement (e.g. plot to right) then compares rate vs layer estimates between different geometries.



# Recent SuperB activities at TRIUMF

- TRIUMF activities are focused on drift chamber R&D.
- **Garfield studies** of cell design: cell shape, superlayer transitions
- **Aging:** many studies already done by A. Boyarski. Use his techniques to check that chamber is viable for a SuperB lifetime.
  - Verify that bare aluminum field wires are OK.
- **Cluster counting:** use a single-channel 2.7m long drift tube to check feasibility and benefits of detecting individual clusters.

Aging chamber $^{55}$Fe spectrum




2700 mm long 19 mm diameter copper tube strung with 20 tungsten sense wire

Nicolas Arnaud
Jerry Va'vra

# PID

# FDIRC progress

## (SLAC, Maryland, Hawaii, Orsay, Padova)

- Raw quartz for FDIRC optics ordered (Delivery in the middle of Nov.)
- Final bids for machining the FBLOCK optics launched (6 companies).
- FDIRC mechanical design for CRT tests in progress.
- H-8500 photon detectors (at the moment we will have at least 14 detectors in FDIRC).
- Concepts how to couple the detectors to electronics discussed.
- Concrete R&D ahead of us: Glue tests, grease tests for detector coupling to quartz, etc.
- Electronics (TDC/ADC development in progress + Hawaii BLAB3 electronics).
- Laser calibration (MC simulation in progress, ideas how to do it exist).
- Start time resolution in CRT (the timing resolution in CRT being analyzed).
- Gas flow & sealing on the FBLOCK (initial discussion has started).
- CRT DAQ system (would like to unify the DAQ system).
- Approximate start of the CRT tests with FDIRC: May - June, 2011

# Forward TOF PID (SLAC, Maryland, Hawaii, Orsay, Padova)

- Will present results from pixilated detector tests in CRT (SLAC):
  - LYSO + MCP-PMT
  - Quartz + G-APD (4x4 array)
  - LYSO + G-APD (4x4 array) Scintillator + G-APD (4x4 array)
  - Scintillator + mesh-PMT

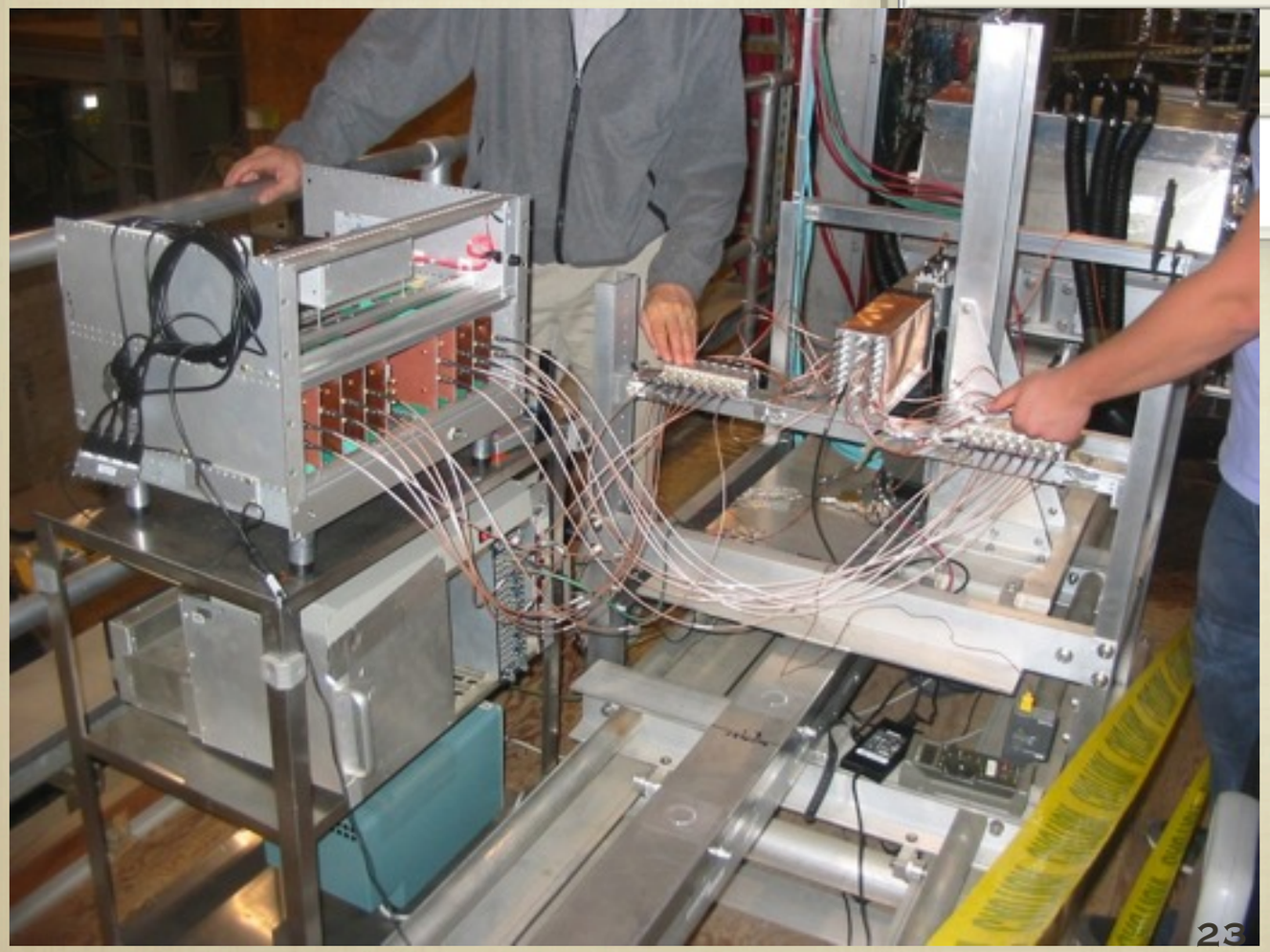
- DIRC-like TOF counter (SLAC & Orsay):
  - Design & construction of the prototype finished (SLAC)
  - Electronics finished (Orsay)
  - CRT tests at SLAC have started a week ago (SLAC + Orsay)
  - Reconstruction tests ongoing.

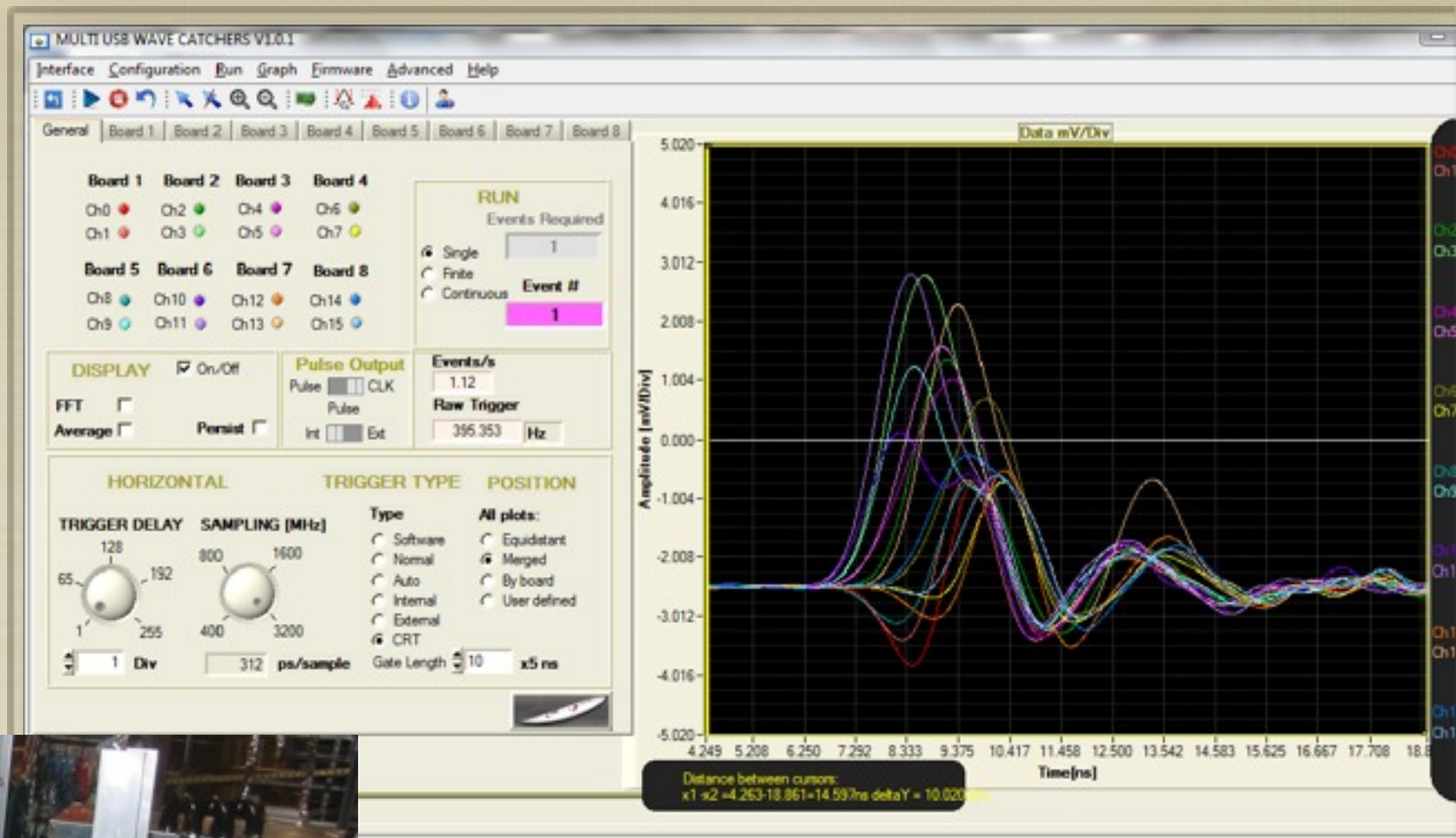
- Tests with SiPMTs at LAL

- See talks in PID parallel sessions for more details.

# PID

## CRT DAQ






## Cosmic in two bars

Claudia Cecchi
Frank Porter

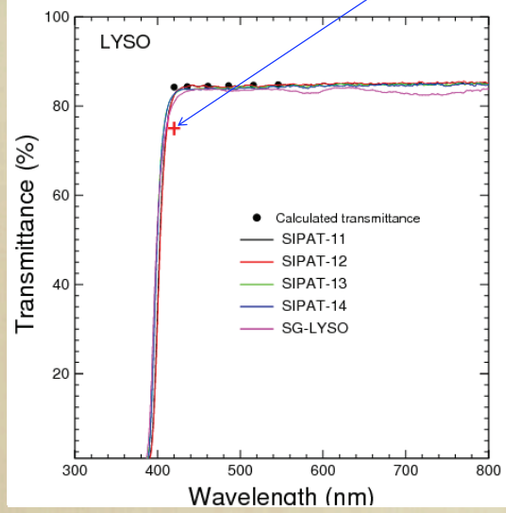
EMC

# EMC - Forward

- LYSO
  - SIPAT now produces crystals performing similarly with Saint-Gobain
  - Developing longitudinal uniformity procedure; tentative target is 5%, MC studies underway to understand requirement

## Longitudinal Transmittance Summary

T% specification: 75% @ 420 nm




All crystals, including SG-05-4, satisfy the transmittance specification.

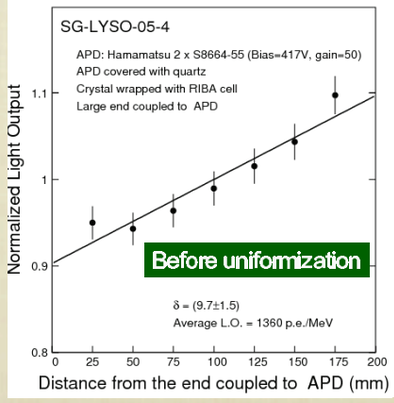
## Summary of Energy Resolution (σ) by APD

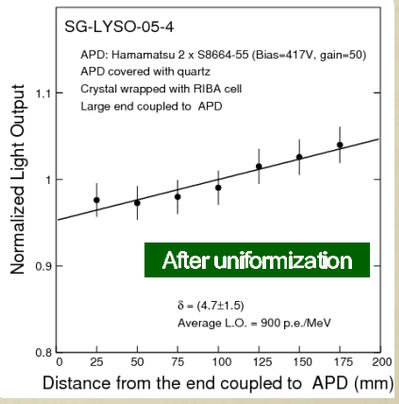
The SG sample is compatible with SIPAT-L13

| Sample ID | | Energy resolution (%) (Mean value of σ at 7 locations) |
|---|---|---|
| SIPAT-11 | Before | 15.5 |
| | After | 27.4 |
| SIPAT-12 | Before | 15.1 |
| | After | 26.7 |
| SIPAT-13 | Before | 14.9 |
| | After | 22.6 |
| SIPAT-14 | Before | 14.9 |
| | After | 24.7 |
| SG-05-04 | Before | 17.3 |
| | After | 23.8 |

## Uniformization: SG-05-4

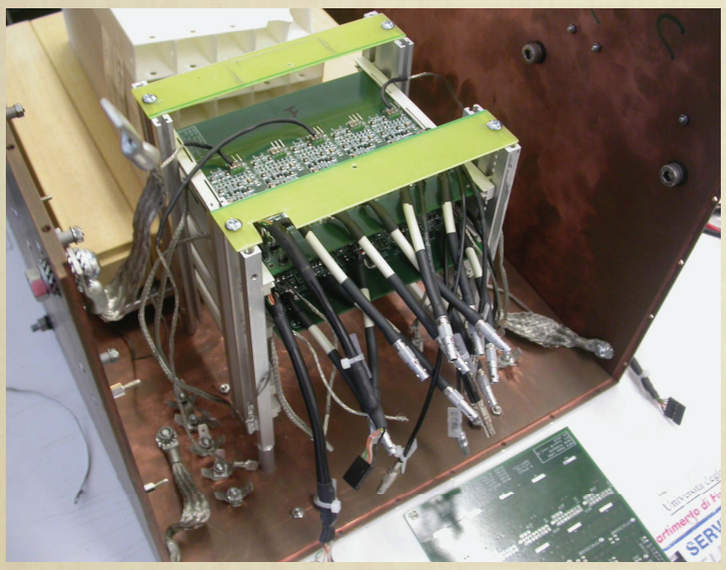
A good light response uniformity of < 5% can be achieved with black strips with a price of losing 34% of the light output.



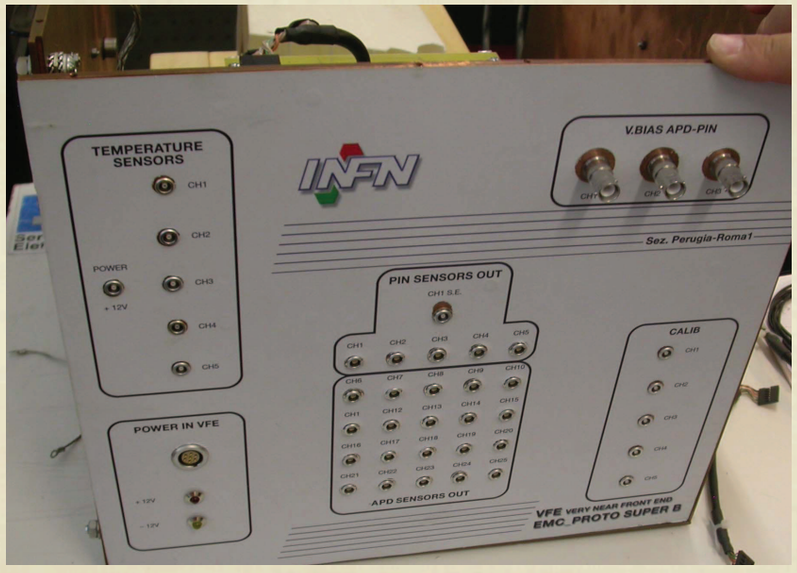



# EMC - Forward

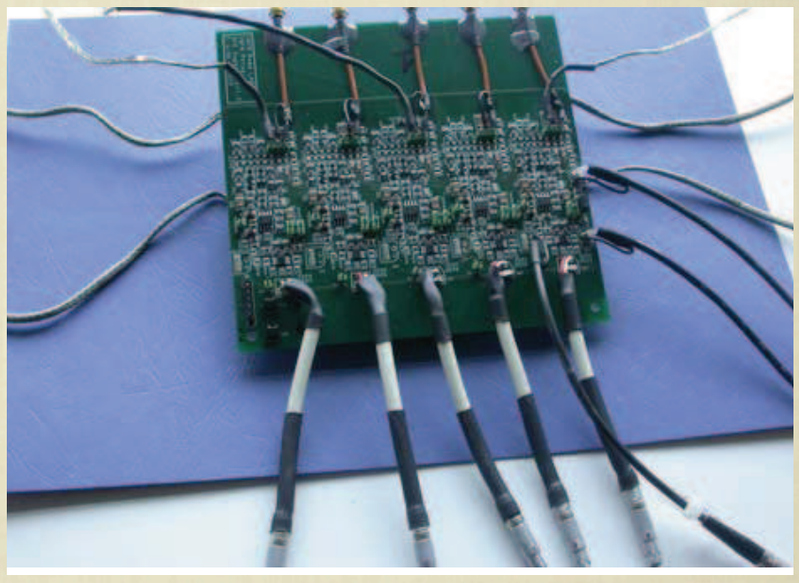
- Focus is on CERN test beam, Oct 11-31, 2010
  - Mechanical structure available
  - Prototype electronics will be used, with single range
  - VME DAQ with vmware for crystals, beam parameters



Mechanical structure



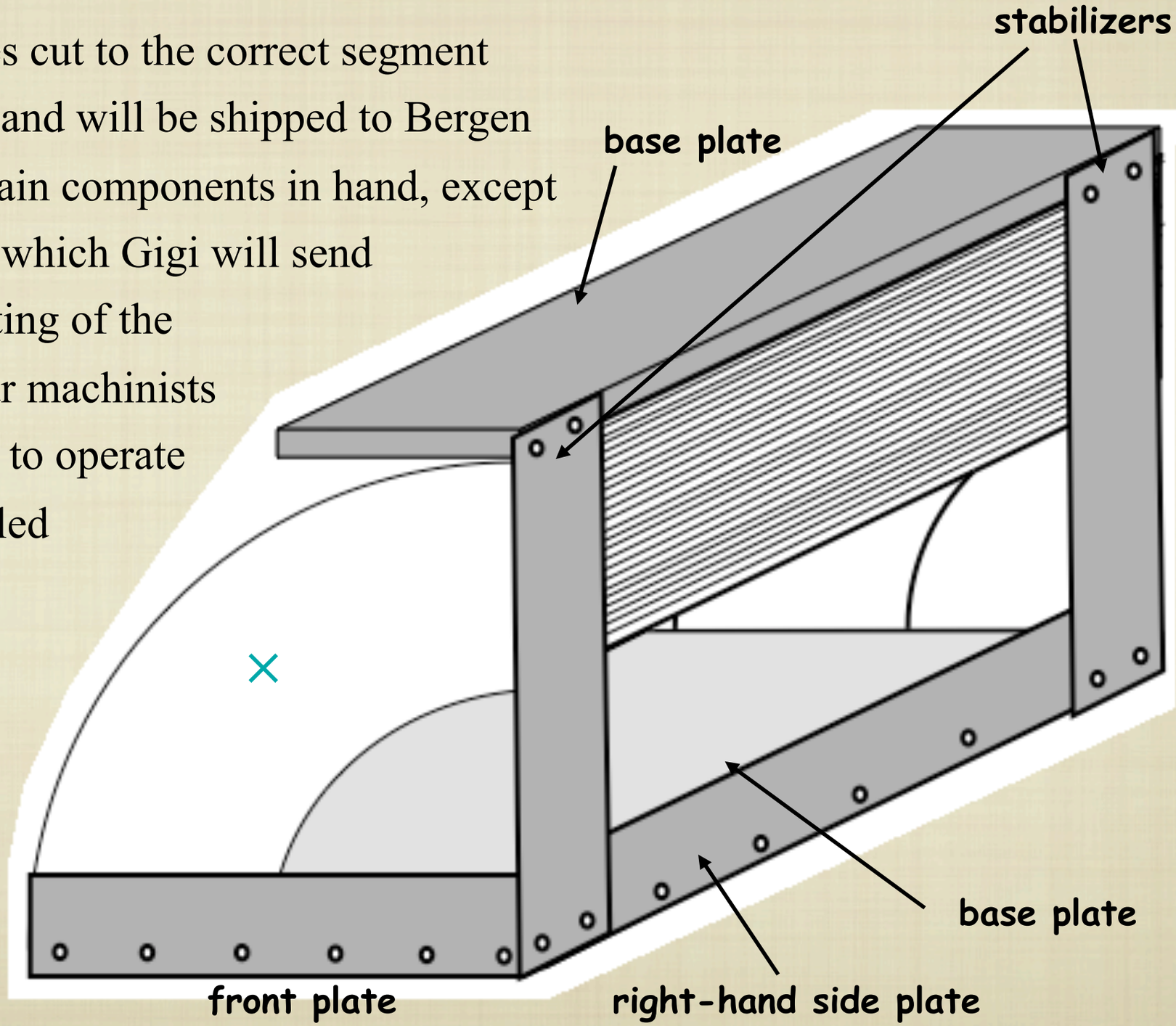

Front panel



VFE card

# Backward Endcap Prototype

- 24 hardened Pb plates cut to the correct segment shapes are at CERN and will be shipped to Bergen
- Thus, we have all main components in hand, except the 80 m Y11 fiber which Gigi will send
- Bottleneck is the cutting of the spiral strips (since our machinists are still learning how to operate the computer-controlled milling machine)
- Aim for testbeam at Frascati next year

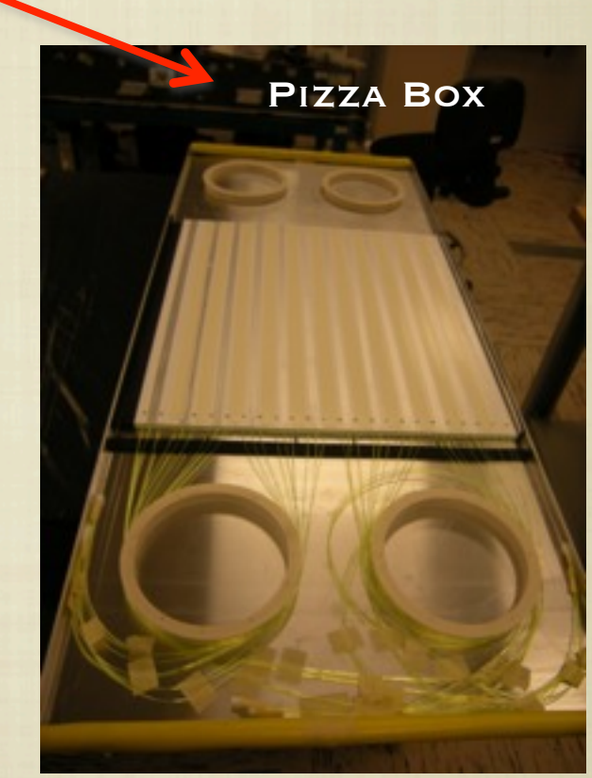


ROBERTO CALABRESE

IFR

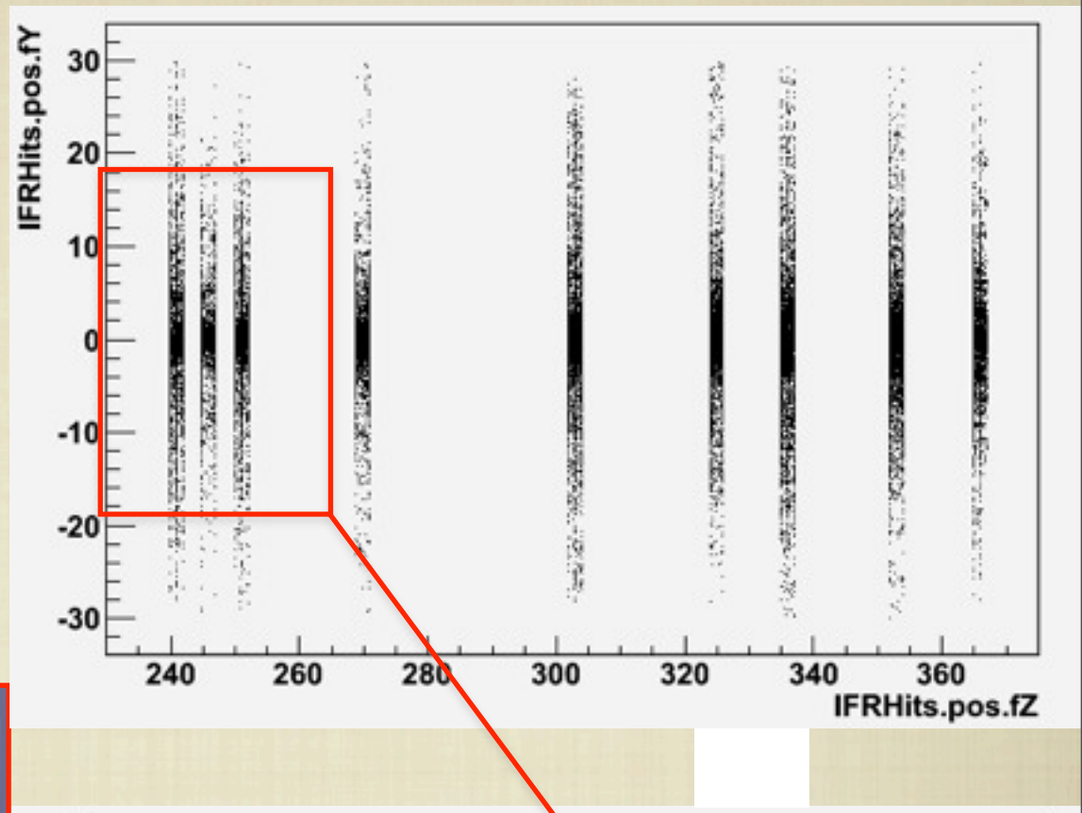
# Advancements since last meeting (I): prototype preparation

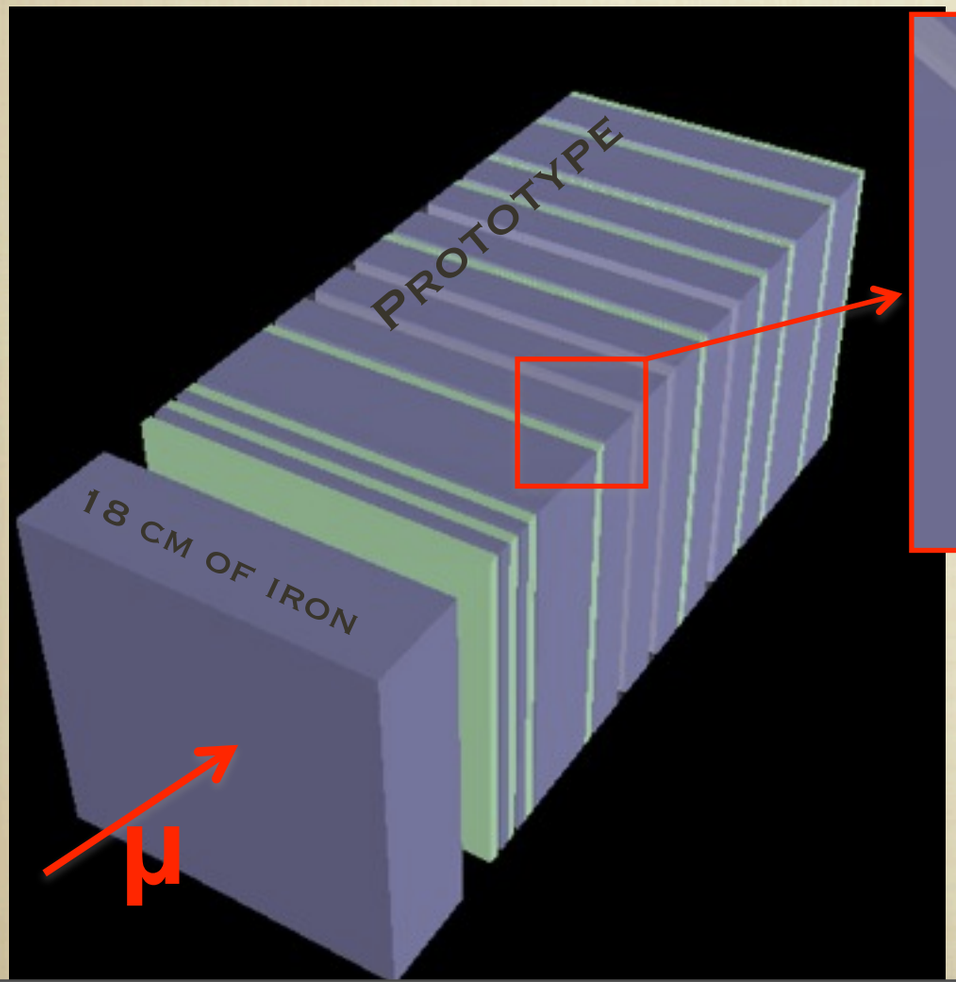
- **The prototype is almost ready:**
  - Iron is on its way  to Fermilab
  - The Active Layers (12 "pizza boxes") assembling is done
  - The coupling fibers-SiPM will be done as soon as we receive all sensors. So far we have about half  of them
  - SiPM characterization ongoing (tested ~ 200/400), about 87% are good
  - We plan to test all active layers with cosmics in October

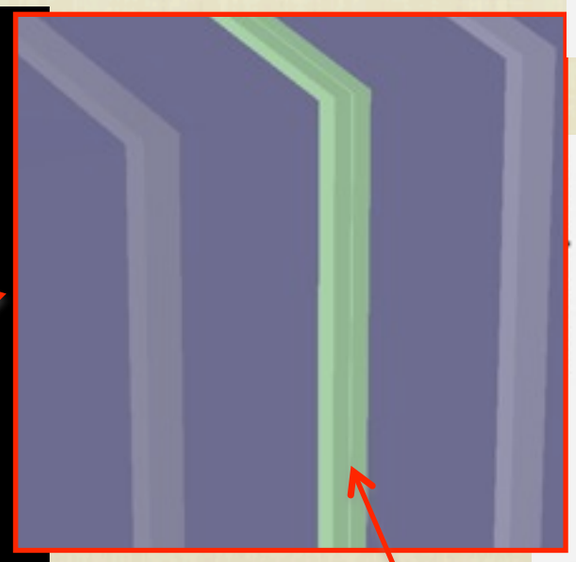


# Advancements since last meeting (II): simulations

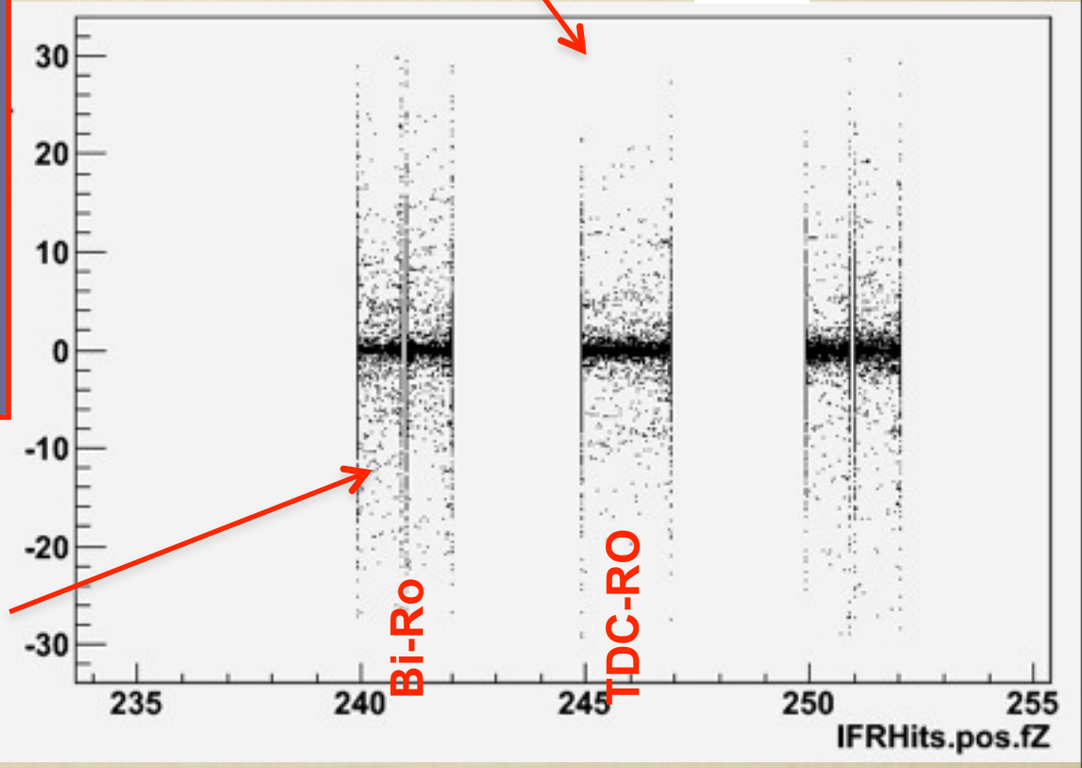
- A full prototype simulation has been developed:
  - It takes into account the realistic condition of the testbeam
  - It simulates both types of Layers (TDC-ReadOut and BI-RO)
  - It allows to move the active layers in different slots, to study the best configuration



X and Y separate Layers for Bi-Ro



# Goal for this meeting

- Review advancements and achievements in all the development areas

- Particular focus on:

  - Prototype finalization and local tests (cosmics, source)

  - Detailed planning and coordination of the the testbeam

  - Analyze the TDR preparation process and prioritize the short and medium term activities

# Towards the TDR

Updated schedule

done
**Fall 09** — finalize prototype design (mechanics and electronics)

done
**December 09** — place orders for prototype construction

done
**January 2010** — prototype preparation

**Oct/Nov 2010** — prototype test with cosmics

**December 2010** — test beam @ FNAL

**Spring 2011** — analyze/review test results and write the TDR

Dominique Breton
Umberto Marconi
Steffen Luitz

ETD

# What was done since Elba workshop

- In Elba, we had a lot of interesting meetings:
  - two of them were dedicated to open discussions about common items and trigger
  - it allowed us to refine the main implementation choices
- During summer, we had interesting discussions between conveners (and with external expert people) about these subjects:
  - Steffen sent a list of points to think about to prepare this meeting (see next slides)
  - They are mainly linked to hardware trigger and system dead time
- Work is going on in Napoli concerning the clock and control links:
  - Progress on understanding the reliability of the clock distribution will be presented on Thursday by Sergio
  - Irradiation of the SERDES chipset is foreseen beginning of next year
- R&D has started on implementing the UDP protocol on a FPGA to be used as ROM's output stage toward the PC farm
  - A working meeting took place in Bologna last week
  - A summary will be presented on Thursday by Domenico or Daniel.

# What we expect from this workshop

- We will have 3 sessions during this workshop:
  - front-end electronics; common items, with time for discussion; hardware trigger.
- During the two last sessions, we would like to start answering the following questions:
  - Will the subdetector be usable in the trigger? (That's mainly an SVT question).
  - What are the achievable time resolution and trigger jitter for a L1 trigger (that has a few microseconds to calculate "a result"), especially in the presence of backgrounds and pile-up? How does this compare to "offline" determination of these parameters e.g. with precise pulse shape fits?
  - What is the achievable time separation between subsequent primitives?

# What do we expect from this workshop (2)

- Is there any intrinsic **per-channel dead time** (like having to wait for the maximum drift time for any given wire before allowing it to trigger again)? To what does this **add up** for a whole sub-detector under realistic conditions?

- Do we need to consider **separate front-end parameters for trigger and event readout** (e.g. in the EMC, do we need different shaping times for trigger and event readout)?

- What **trigger readout granularity** do we need?

- What are the possibilities of **simulating the detector** or using BaBar data for trigger studies?

- We would like the concerned colleagues to think about these questions and to prepare a few draft slides for the sessions.

# Workshop Agenda

## today

**11:15->*12:45* Parallel - Det: Discussion with BELLE**
(Convener: Francesco Forti (*PI*) , Blair Ratcliff (*SLAC*) ) (Aula Touschek )
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2772

| | | |
|---|---|---|
| 11:15 | Belle II - Beam Pipe and Backgrounds (20') | Hiroyuki Nakayama (*KEK*) |
| 11:35 | Belle II - Other Detector Issues (20') | Yutaka Ushiroda (*KEK*) |
| 11:55 | Backgrounds in SuperB (20') | Eugenio Paoloni (*PI*) |
| 12:15 | Discussion (20') | |

**14:00->*15:30* Parallel - Acc + Det: MDI** (Convener: John Seeman (*SL*
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2772

**14:00->*15:30* Parallel - Phys + Comp: FastSim** (Convener: David
) (Aula Seminari )
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2751

15:30 coffee break (30') (Aula Touschek Fo

**16:00->*17:40* Parallel - Accelerator II** (Convener: Pantaleo Raimondi
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: ????

**16:00->*17:30* Parallel - Det + Comp: Backgrounds** (Convener:
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2772

**16:00->*17:40* Parallel - ETD 1 - Front-end electronics** (Conve
Umberto Marconi (*INFN*) ) (Aula Seminari )
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2751

# Workshop Agenda

## Today

**11:15->*12:45* Parallel - Det: Discussion witl**
(Convener: Francesco Forti (*PI*) , Blair Ratcliff (*SLAC*) ) (Aula Tousch
Description:
Phone number: +39 06 6228 8548
or http://server10.infn.it/video/index.php?page=telephone_nun
Meeting ID: 2772

| | | |
|---|---|---|
| 11:15 | Belle II - Beam Pipe and Backgrounds (20') | H |
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or http://server10.infn.it/video/index.php?page=telephone_numbers
Meeting ID: 2751

15:30 coffee break (30') (Aula Touschek Fo

| Parallel - Accelerator III | Parallel - Computing: R&D 1 | Parallel - Det: ETD 2 - Common items | Parallel - Physics |
|---|---|---|---|
| Conveners: John Seeman (SLAC) (Aula DA - Div. Acceleratori: 09:00 - 10:30) | (Aula Seminari: 09:00 - 10:30) | Conveners: Mr. Dominique Breton (LAL ORSAY); Dr. Steffen Luitz (SLAC); Dr. Umberto Marconi (INFN) (Aula Touschek: 09:00 - 10:30) | Conveners: Prof. Achille Stocchi (LAL - Univeriste Paris Sud and IN2p3/CNRS); Dr. Adrian Bevan (Queen Mary); Marco Ciuchini (RM3); Dr. David Brown (Lawrence Berkeley National Lab) (Aula A-1: 09:00 - 10:30) |

**coffee break**
(Aula Touschek Foyer: 10:30 - 11:00)

| Parallel - Accelerator IV | Parallel - Det + Phys + Comp: DGWG |
|---|---|
| Conveners: Michael Sullivan (SLAC National Accelerator Laboratory) (Aula DA - Div. Acceleratori: 11:00 - 12:30) | Conveners: Matteo Rama (LNF); Prof. Achille Stocchi (LAL - Univeriste Paris Sud and IN2p3/CNRS) (Aula Touschek: 11:00 - 12:30) |

## Tomorrow

| PID open discussion | Parallel - Accelerator VI | Parallel - DCH | Parallel - EMC | Parallel - IFR | Parallel - SVT |
|---|---|---|---|---|---|
| Conveners: Dr. NICOLAS ARNAUD (LAL ORSAY CNRS-IN2P3); Dr. Jerry Vavra (SLAC) (Aula B-1: 16:00 - 17:30) | Conveners: Maria Enrica Biagini (LNF) (Aula DA - Div. Acceleratori: 16:00 - 17:50) | Conveners: Giuseppe Finocchiaro (INFN - LNF); Prof. Michael Roney (University of Victoria) (Aula Calcolo: 16:00 - 17:30) | Conveners: Claudia Cecchi (PG); Prof. Frank Porter (Caltech) (Aula A-1: 16:00 - 17:30) | Conveners: Roberto Calabrese (FE) (Aula Seminari: 16:00 - 17:30) | Conveners: Giuliana Rizzo (PI) (Aula Touschek: 16:00 - 17:30) |

# Workshop Agenda

## Thursday

| | | | | |
|---|---|---|---|---|
| **Parallel - Accelerator VII**<br>(Aula DA - Div. Acceleratori: 09:00 - 10:30) | **Parallel - Computing: R&D 2**<br>(Aula Seminari: 09:00 - 10:30) | **Parallel - Det: BEMC Panel Mtg (closed)**<br>(Aula B-1: 09:00 - 10:30) | **Parallel - Det: ETD 3**<br>(Aula Touschek: 09:00 - 10:30) | **Parallel - Det: FPID Panel Mtg (closed)**<br>Conveners: Francesco Forti (PI)<br>(Aula A-1: 09:00 - 10:30) |
| **coffee break**<br>(Aula Touschek Foyer: 10:30 - 11:00) | | | | |
| **Theory Seminar**<br>Conveners: Gino Isidori (LNF)<br>(Aula Touschek: 11:00 - 12:30) | | | | |
| **lunch break**<br>(Aula Fermi (bldg. 33): 12:30 - 14:00) | | | | |
| **Parallel - Accelerator VIII**<br>(Aula DA - Div. Acceleratori: 14:00 - 15:30) | **Parallel - Computing: Organization**<br>(Aula Seminari: 14:00 - 15:30) | **Parallel - Physics**<br>Conveners: Prof. Achille Stocchi (LAL - Univeriste Paris Sud and IN2p3/CNRS); Dr. David Brown (Lawrence Berkeley National Lab); Dr. Adrian Bevan (Queen Mary); Marco Ciuchini (RM3)<br>(Aula A-1: 14:00 - 15:30) | **Parallel - TDR Writing**<br>(Aula Touschek: 14:00 - 15:30) | |
| **coffee break**<br>(Aula Touschek Foyer: 15:30 - 16:00) | | | | |
| **Accelerator Board**<br>(Aula DA - Div. Acceleratori: 16:00 - 17:30) | **Detector Technical Board**<br>(Aula Direzione: 16:00 - 17:30) | | | |

# Workshop Goals

## Make sure we're alive

- Advance towards the Technical Design Report

- Technical issues
  - Geometry
  - Technical choices
  - Prototype preparation and testing
- Collaboration and manpower
  - Add institutions
  - Build manpower
  - Prepare hires
- Planning
  - Prepare TDR production plans
  - Prepare construction schedule