Requirement

- Synchronization of the detector

  Clock, reset, buffering
- L1 trigger decision

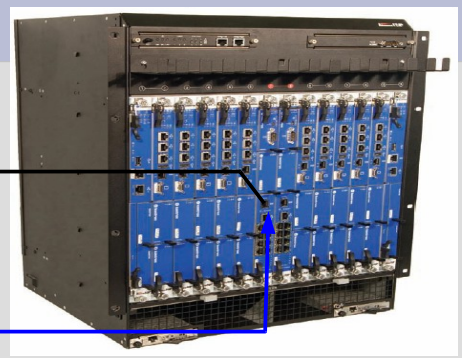
  Handling: Throttle, buffering
- Local trigger

  Calibration, commissioning
- Frame computation

  event identifier

  IP rooting
- Spy event
- Independent by sub-detector

FCTS architecture



Clk machine

FCTS Crate

Global Level 1 Trigger

ECS

EMC FE

IFR FE

SVT FE

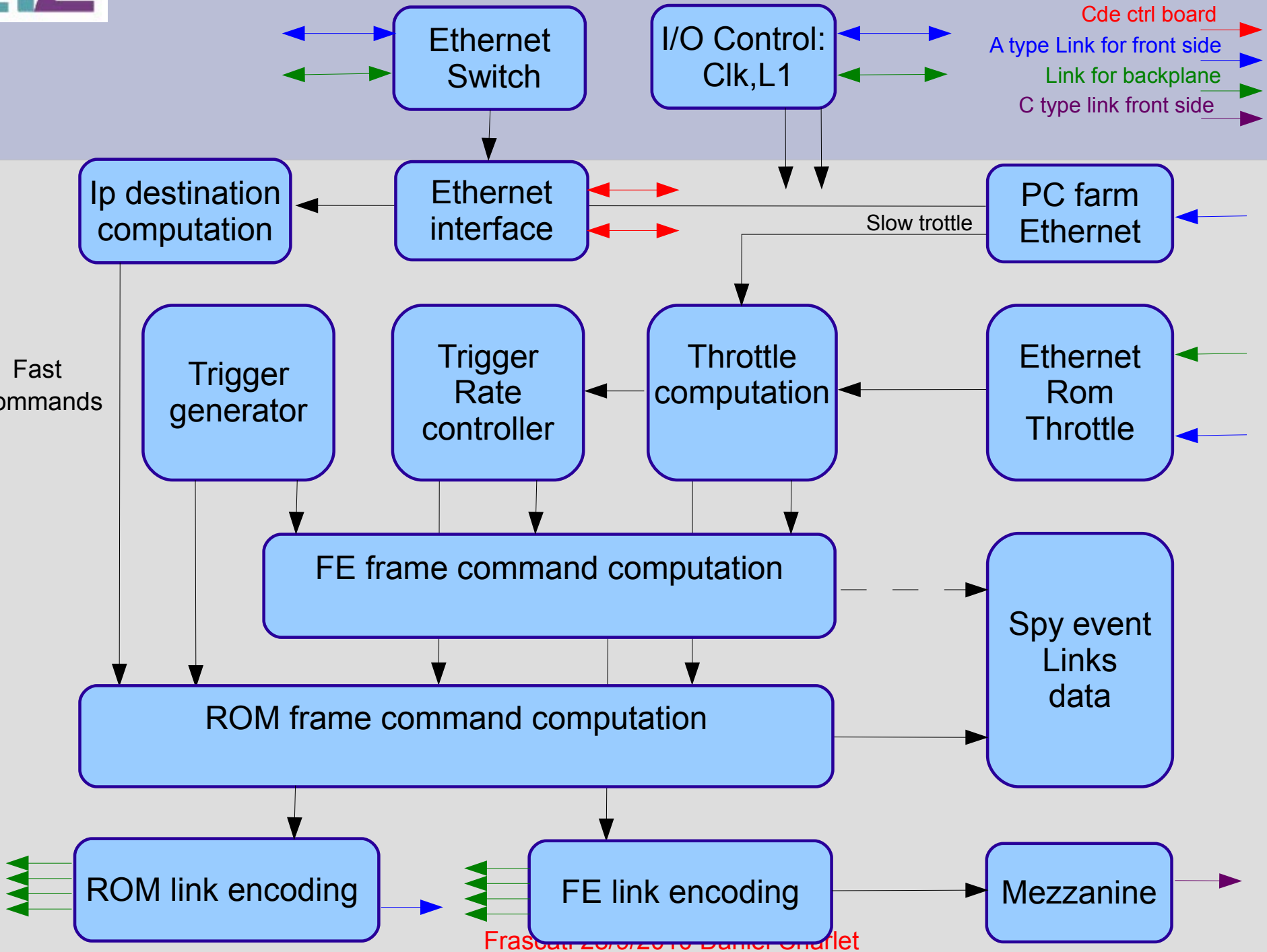
DHC FE

PID FE

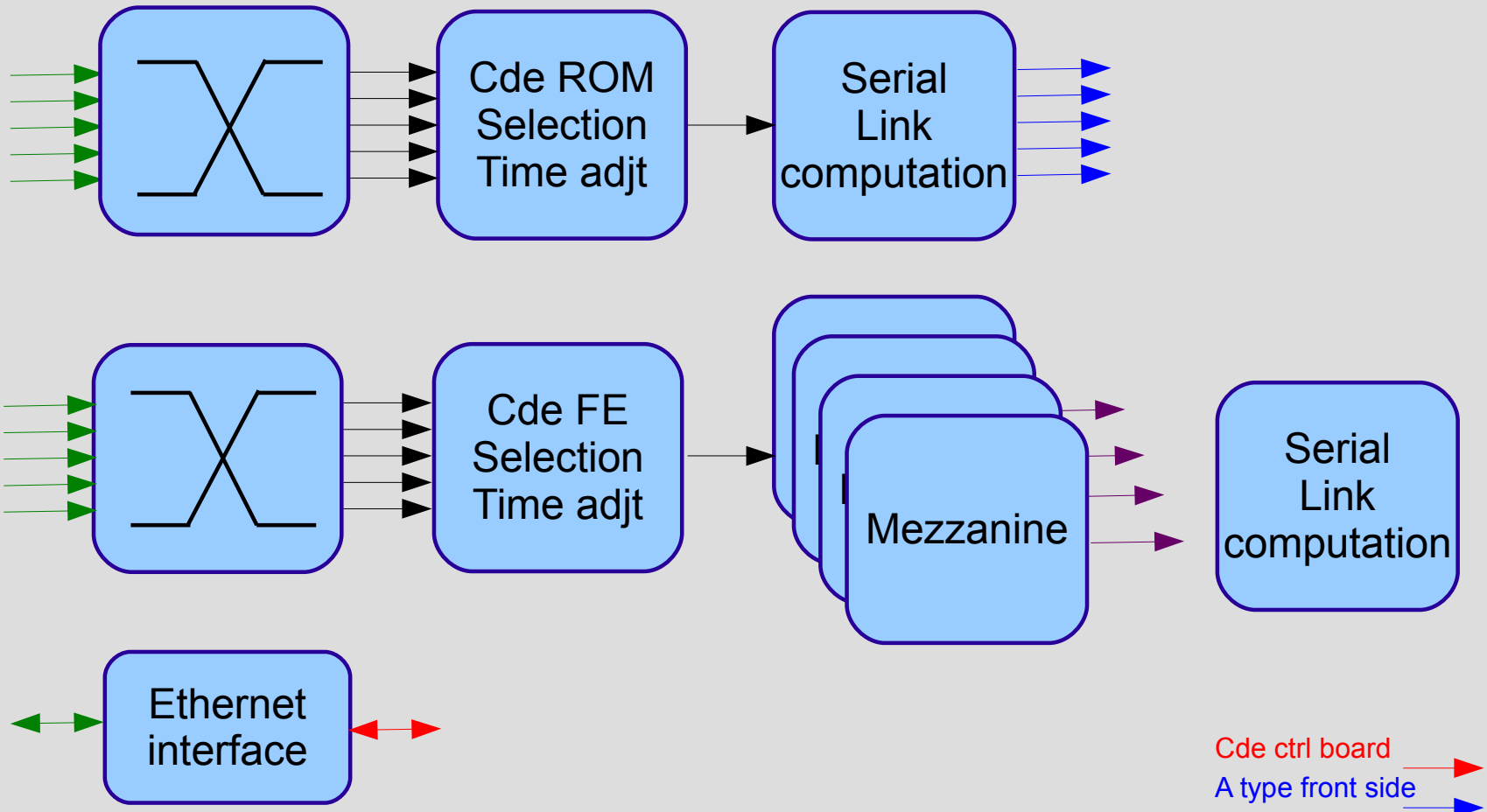
Front-End electronics

ReadOut Module

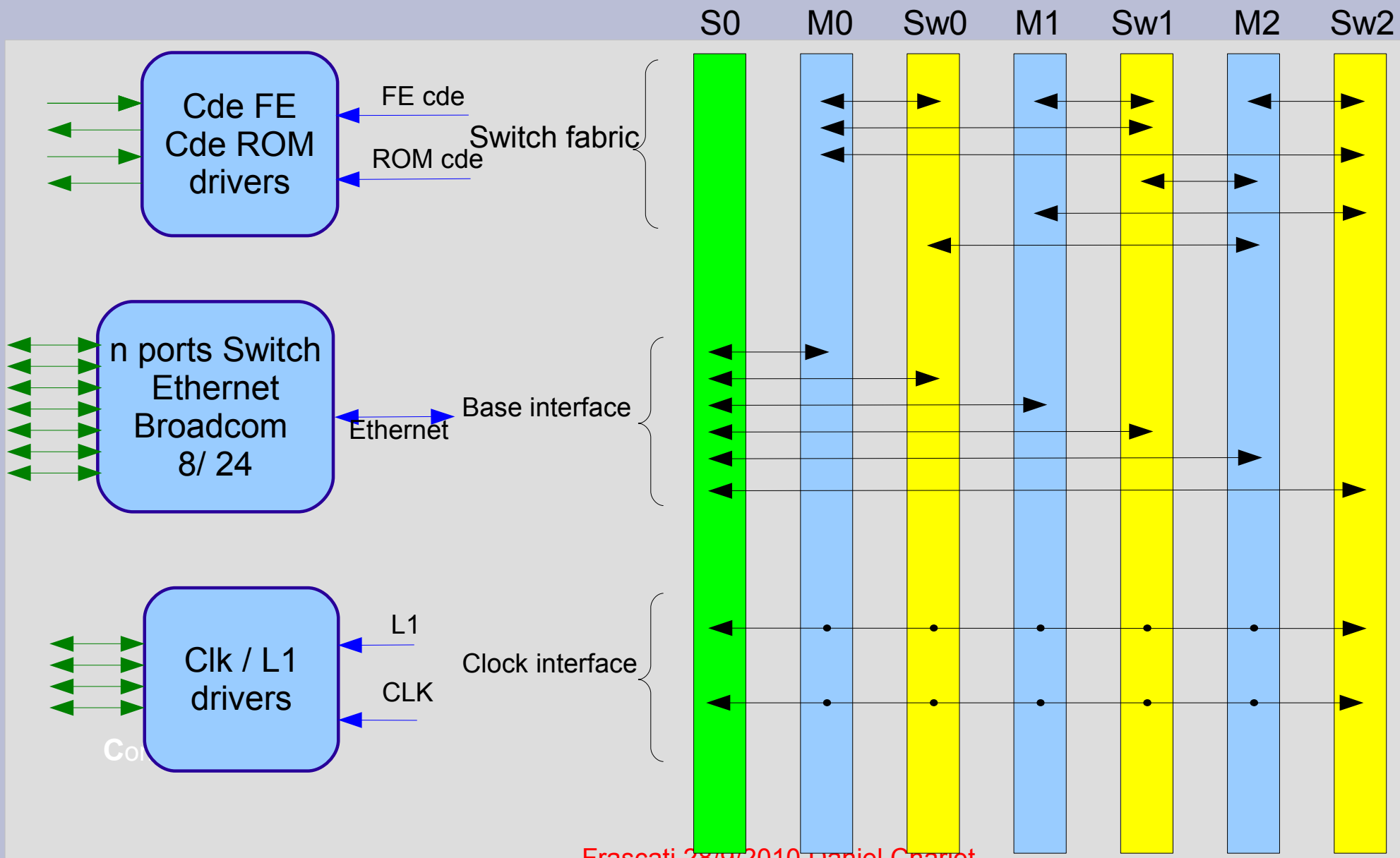
FCTM architecture



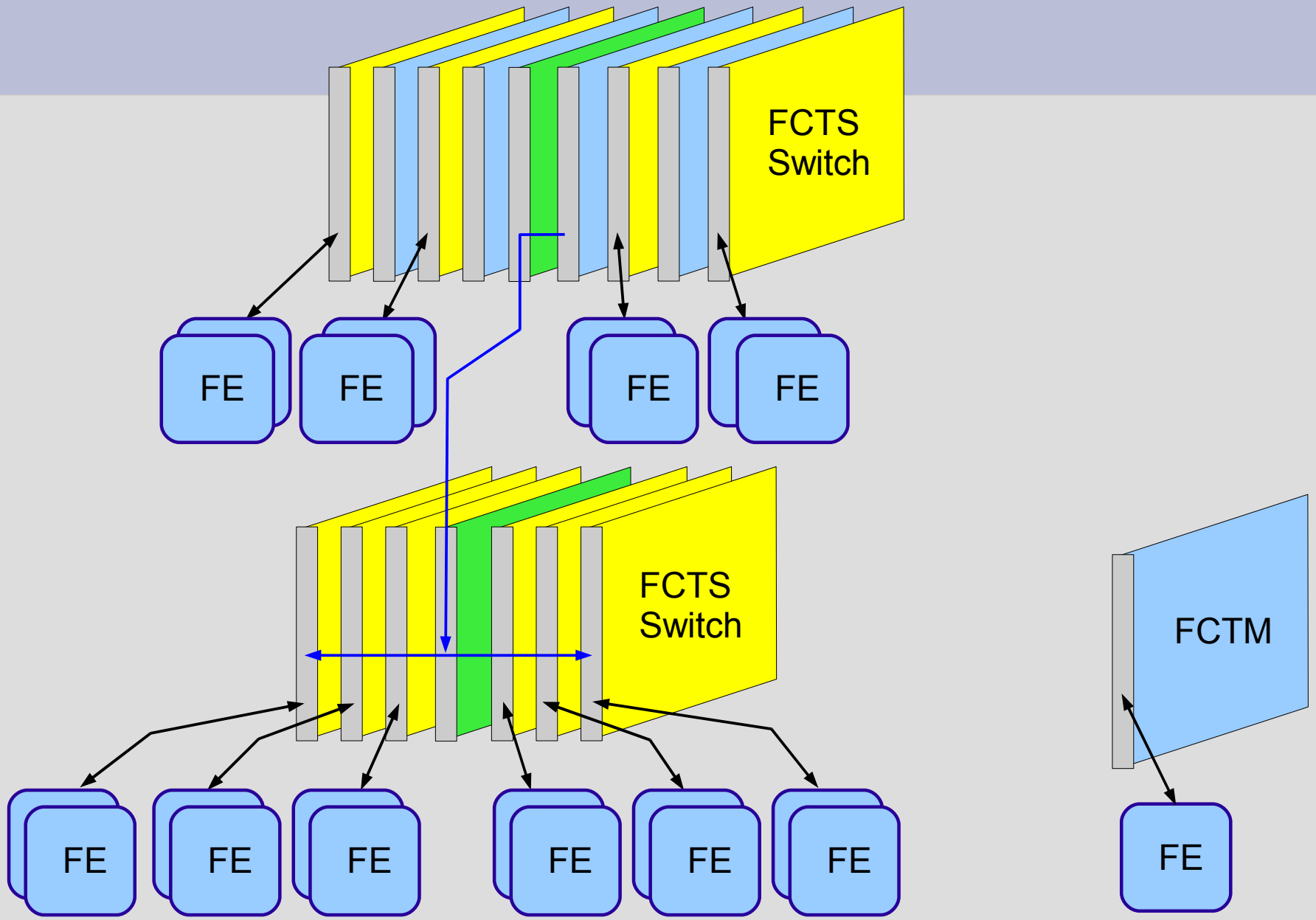
Switch module



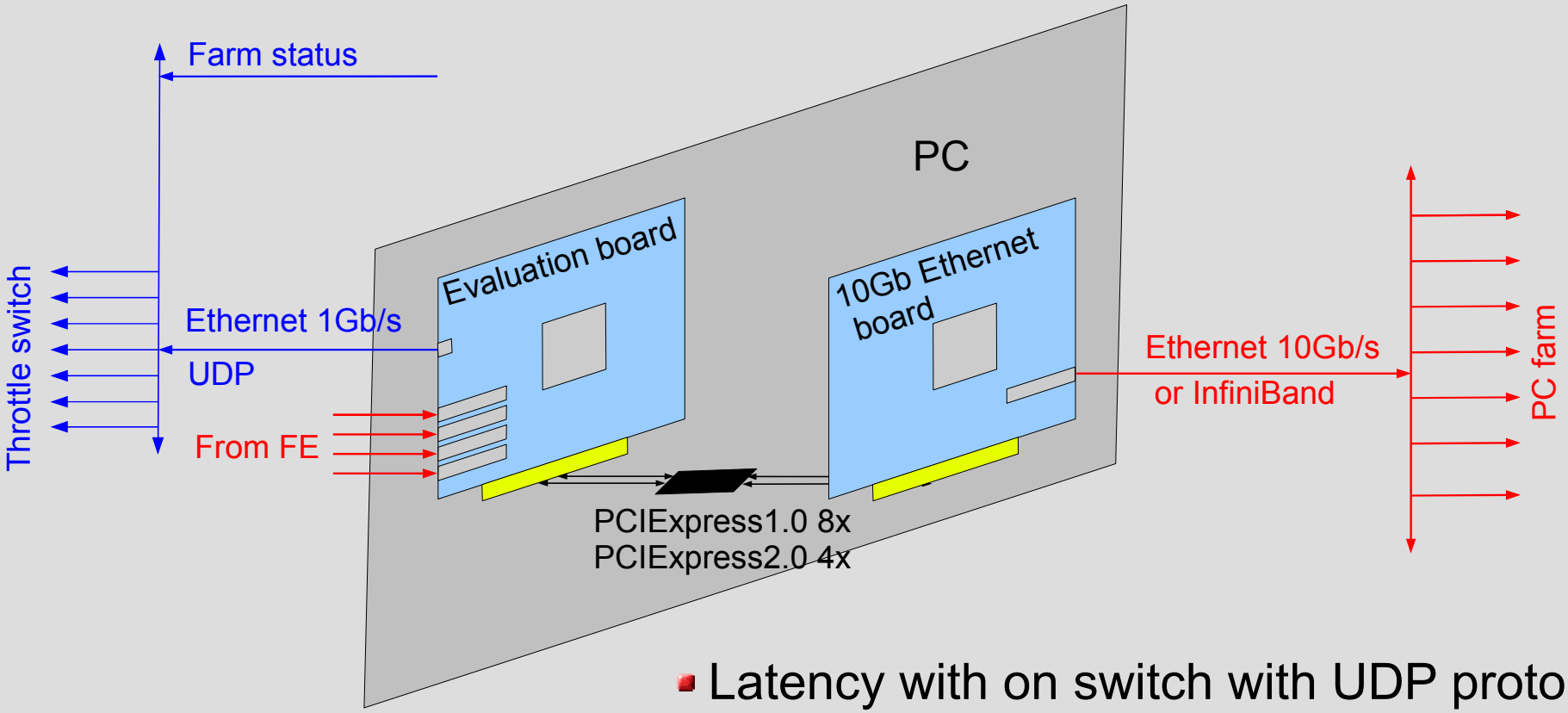
Slot 0 & Backplane ATCA



FCTS implementation



ROM module



- Latency with on switch with UDP protocol?.
- All compression algorithm must be implemented in FPGA.
- IP number will be used as throttle command.
- No board development (Firmware/sofware).

Conclusions

- ATCA crate will be used but in custom way.
- Throttle origin only from ROM.
- Farm status require at the FCTM.
- No board rom development
- No back-plane development.
- ?