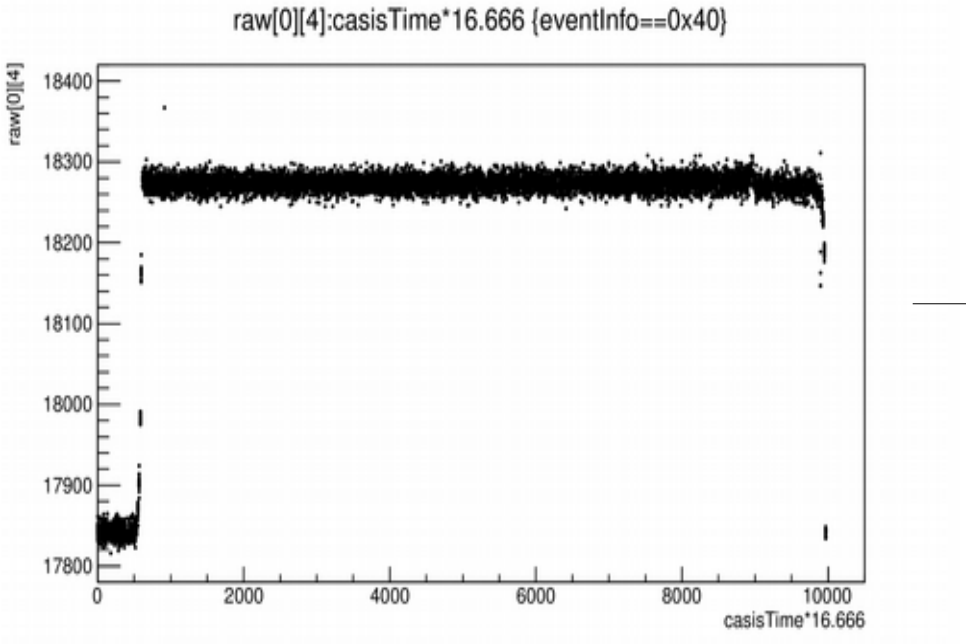
# Test with HiDRA2

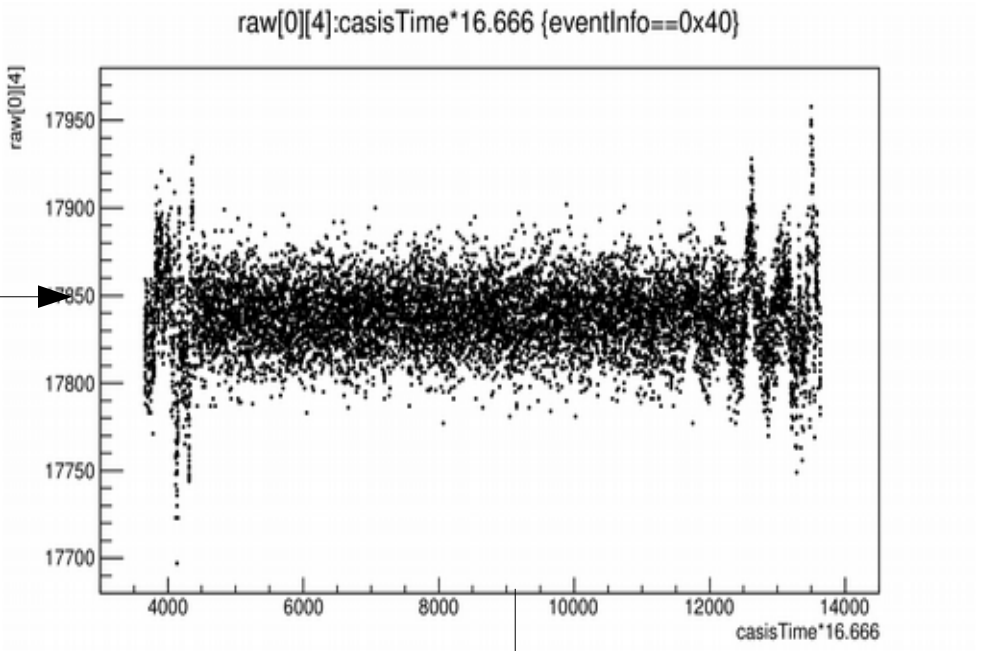
Eugenio and Lorenzo, 27 May 2020

# Pedestal trend

Two different trends were due to CAL_EN signal always sent when a trigger arrives (even outside calibration mode)



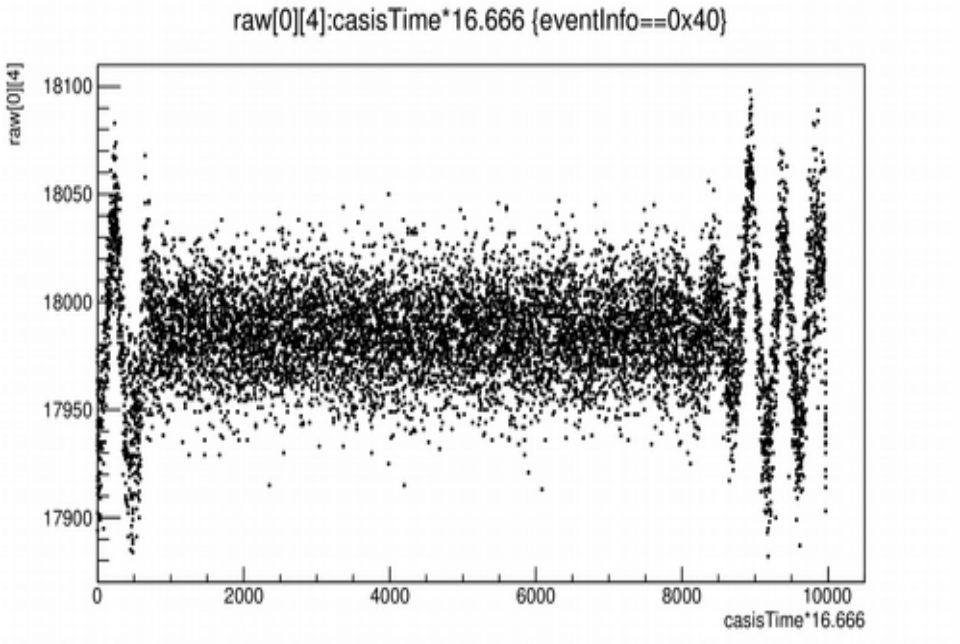

The problem was solved updating TROC2 firmware to version V230B



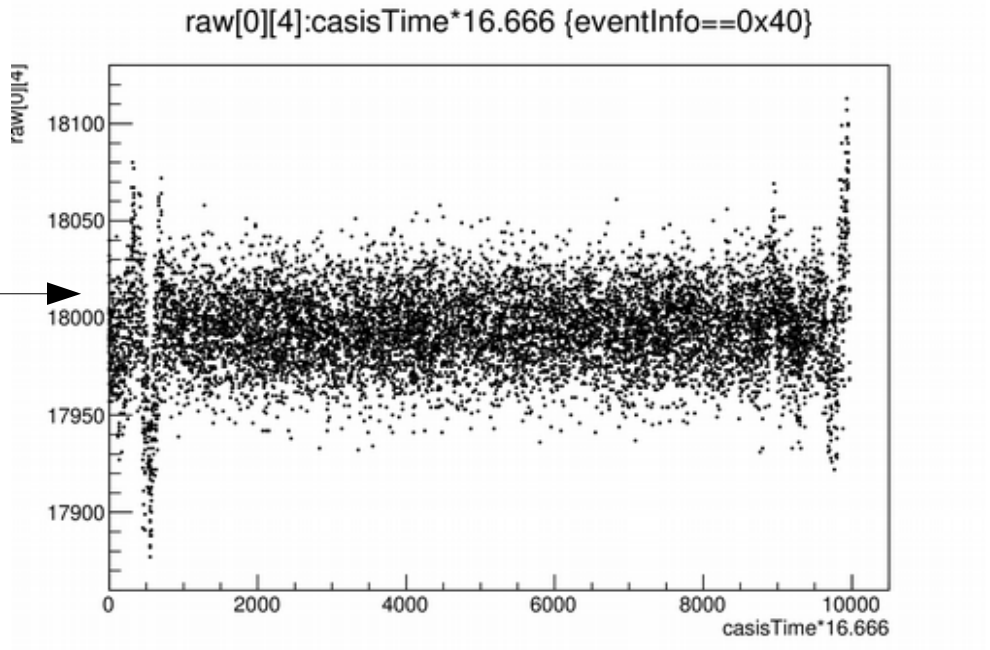

The casisTime has now an offset of 220 clock counts, problem that was solved in version V2514 (but all data shown here was obtained using previous firmware)

# Effect of Power Supply

Keithley



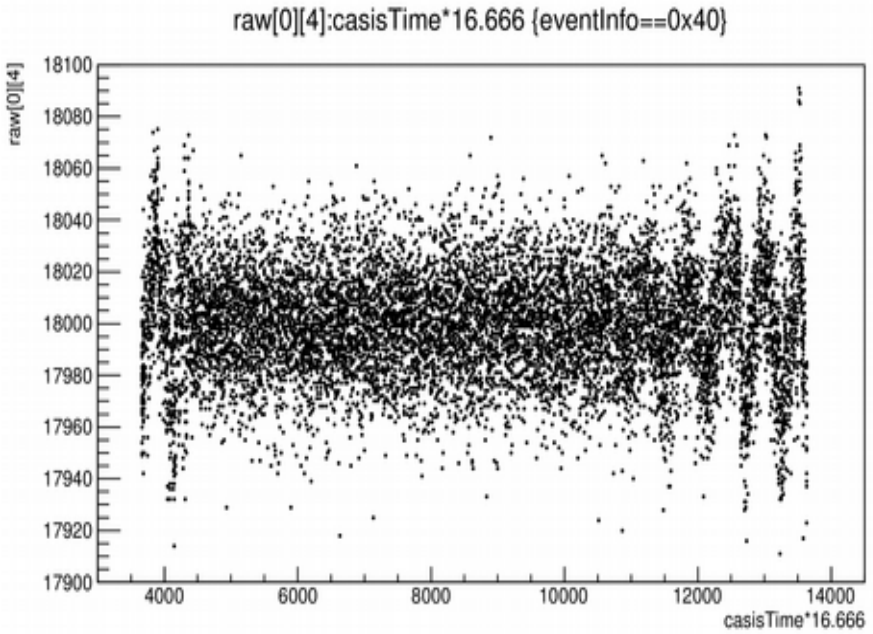

Batteries



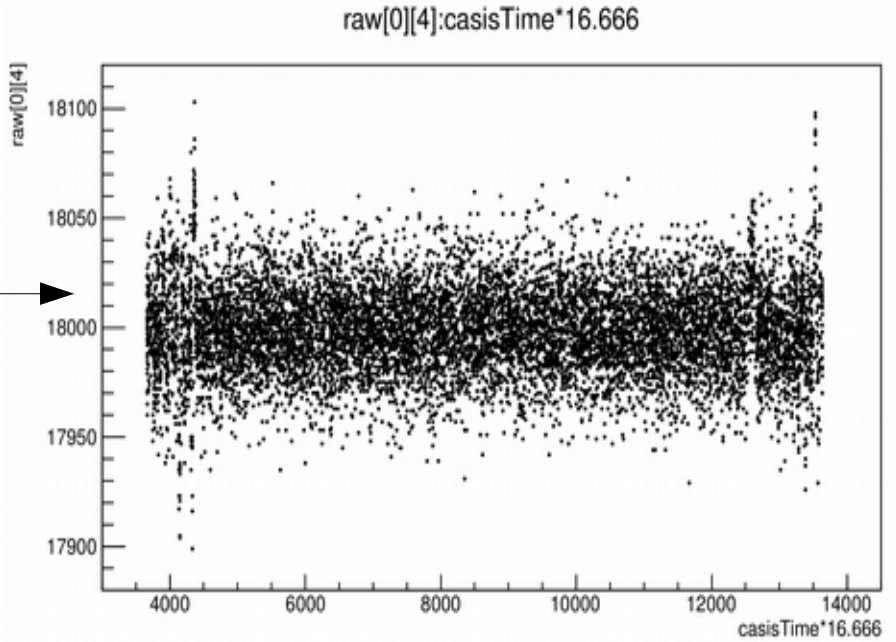

Batteries work much better than Keithley in reducing the external interferences, but they are not very comfortable...

# Effect of Better Configuration

Keithley (Old setup)



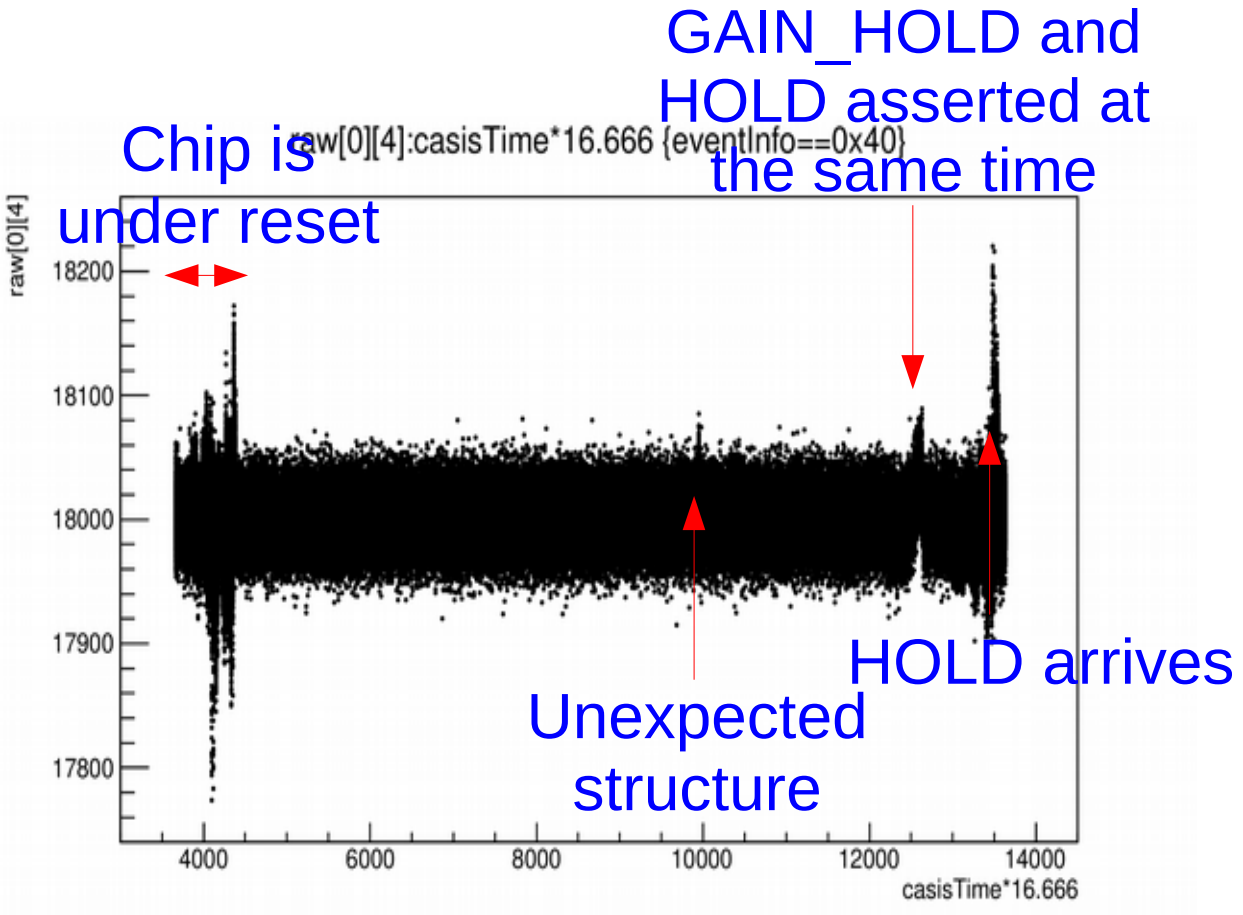

Keithley (New setup)




Following suggestions from Trieste colleagues, we clearly separated digital signals from analog signals on the experimental table. Additionally, we used a power supply filter made by Sebastiano that gave us a result only slightly worse to the batteries one.

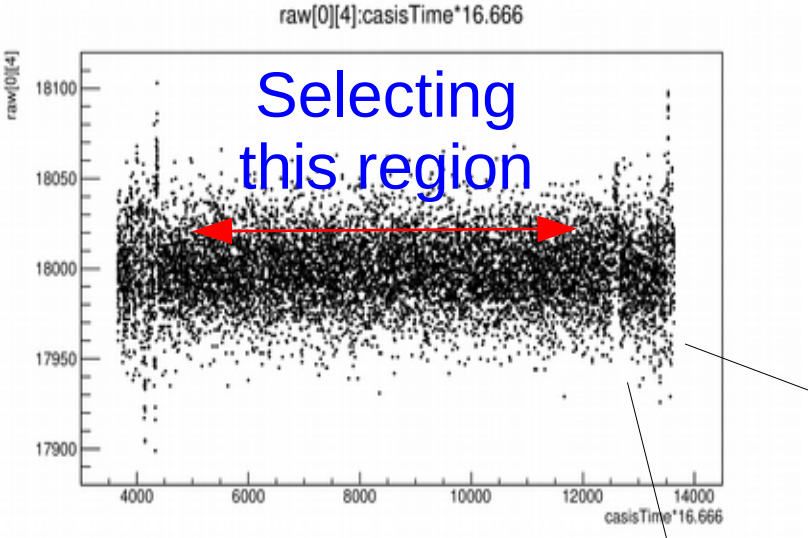
For this reason, in the following we run all tests using this configuration.

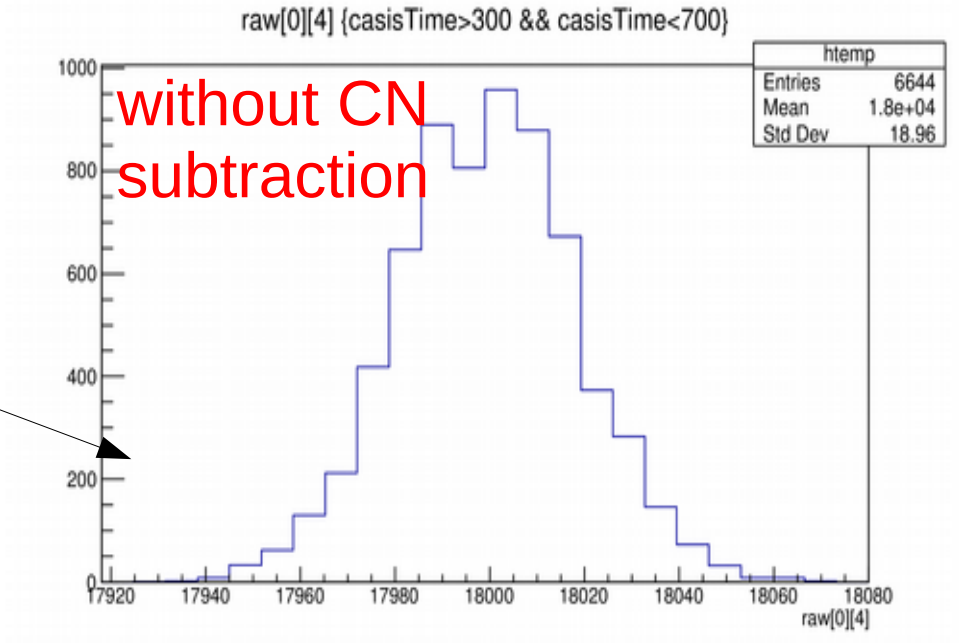
# Residual Pedestal Structures

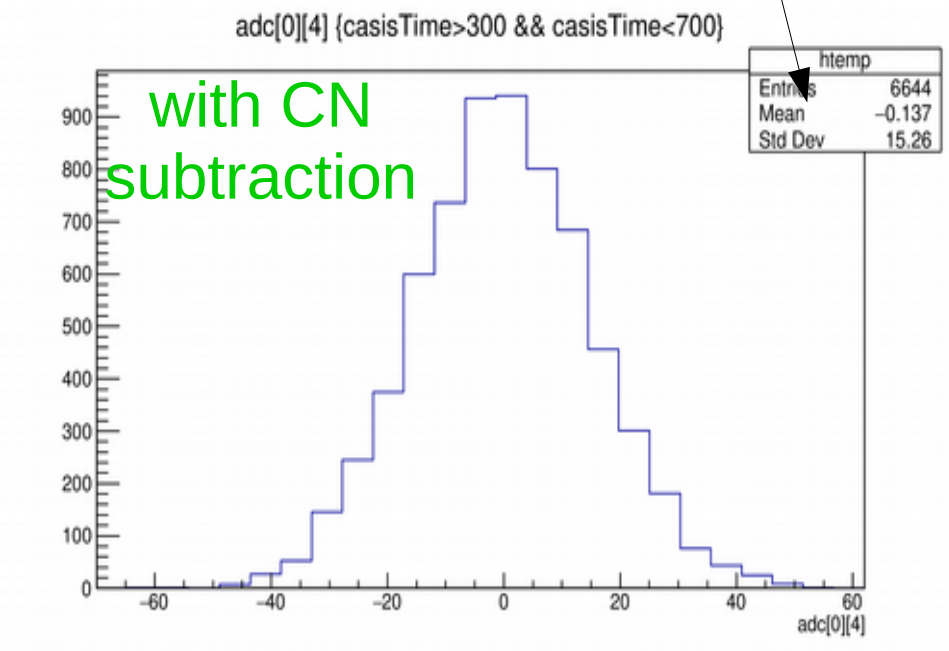



According to suggestions from Trieste colleagues, the simultaneous signals GAIN_HOLD and HOLD could interfere with the analog signal at the board or chip level: what we can do for the moment is to not assert GAIN_HOLD signal when it would arrive synchronous or delayed respect to the HOLD signal.

# Pedestal Noise

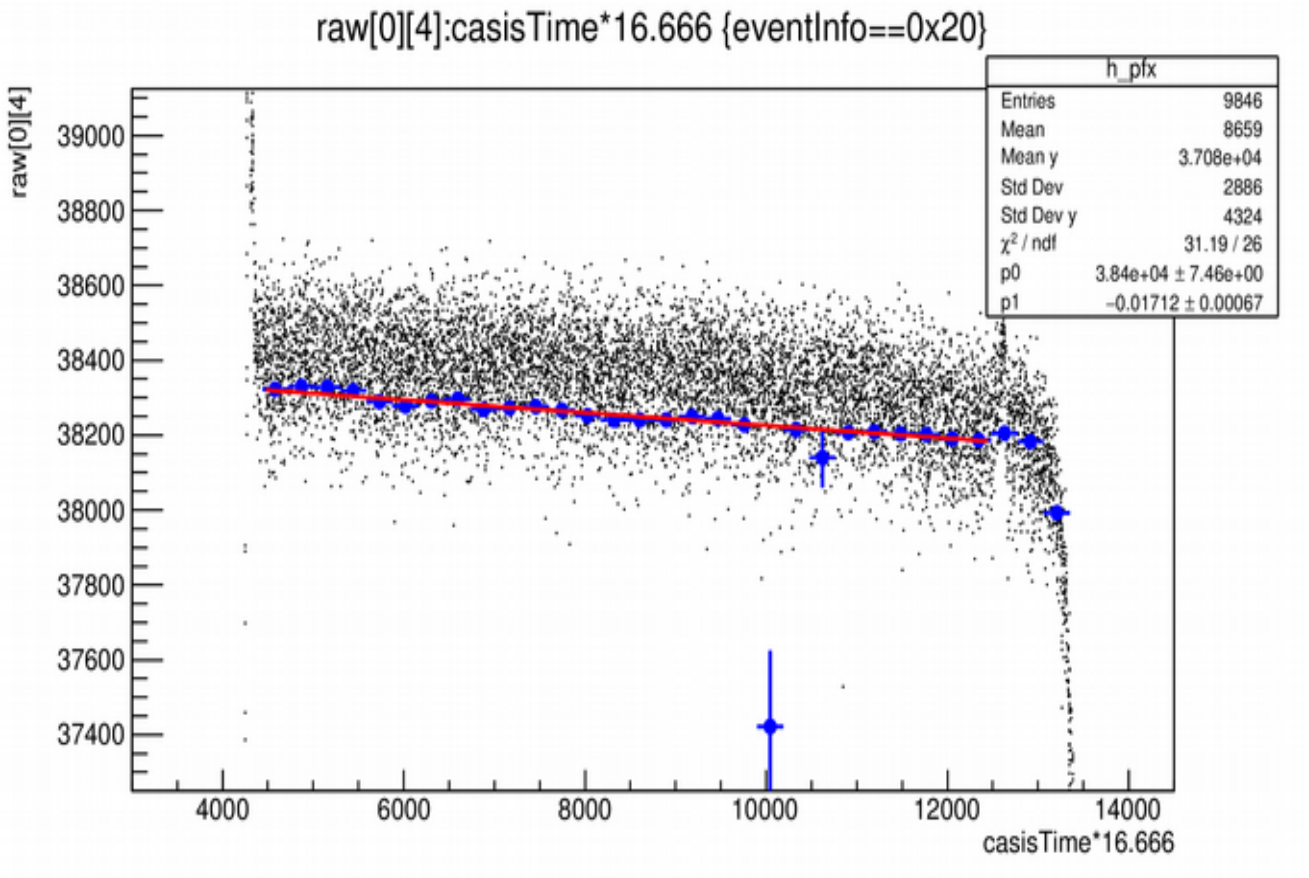


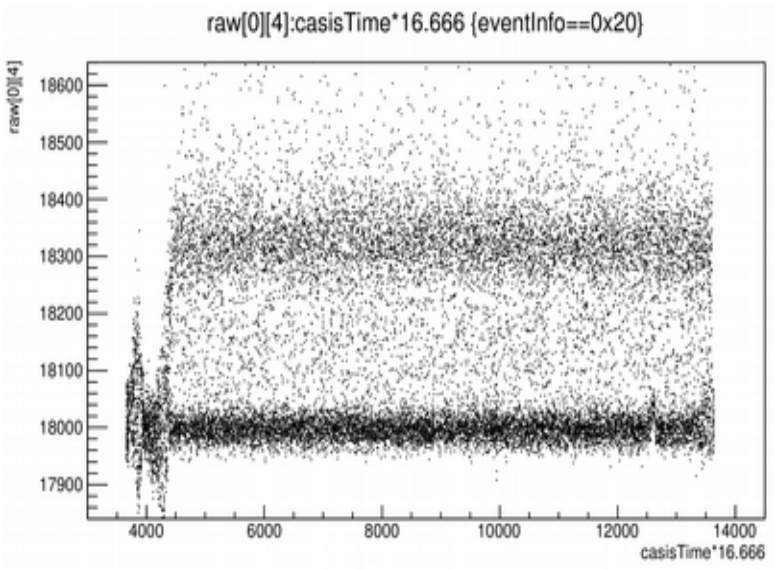

The **RMS** of the *electrical noise* of a channel where we connected a biased PD is now <u>19 ADC (w/o CN subtraction) or 15 ADC (w CN subtraction)</u>, in good agreement with our theoretical expectations.

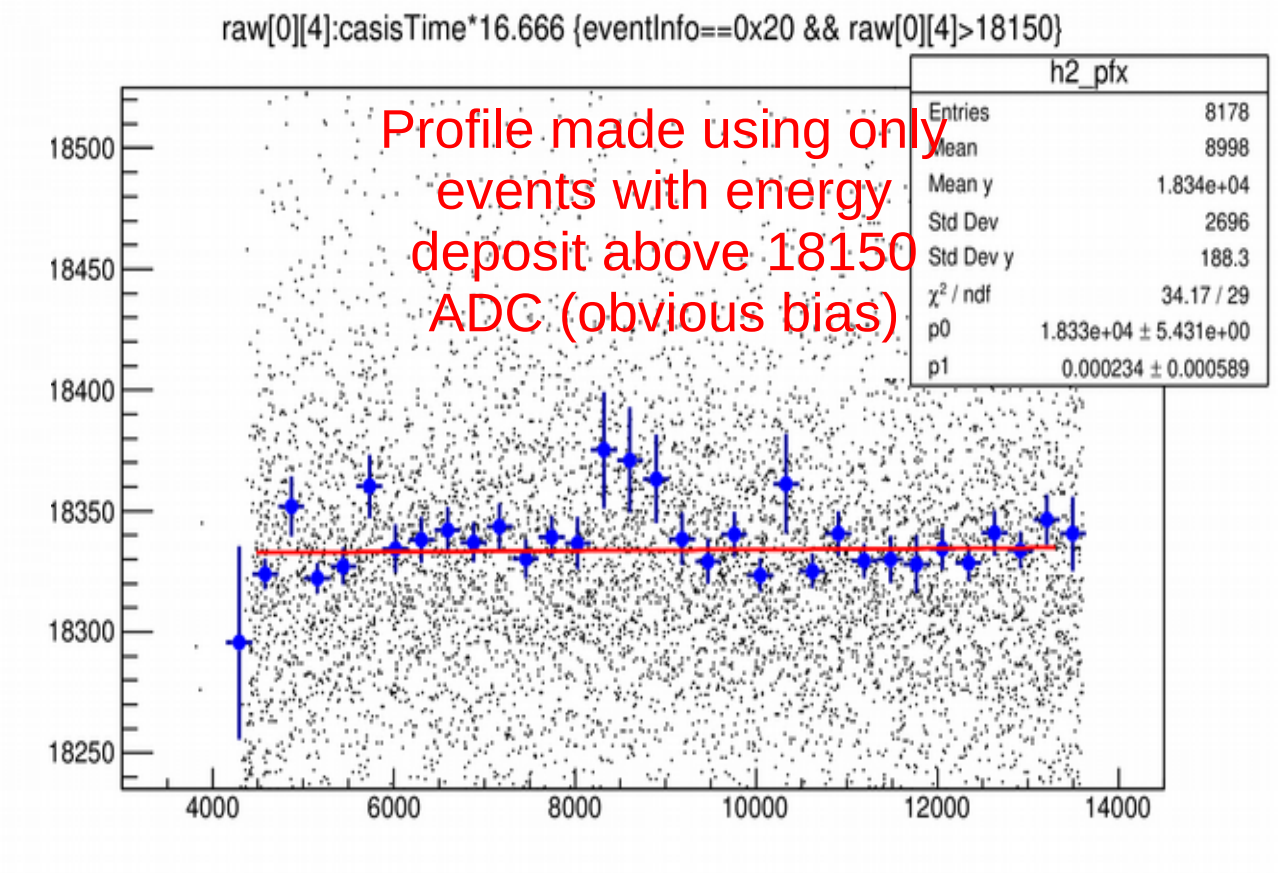
# Injecting signal using LED




The signal decrease as a function of CASIS Time means that, enlarging the integration window, the integrated signal increases by 0.0171 ADC/ns.

# Looking at the MIP signal itself



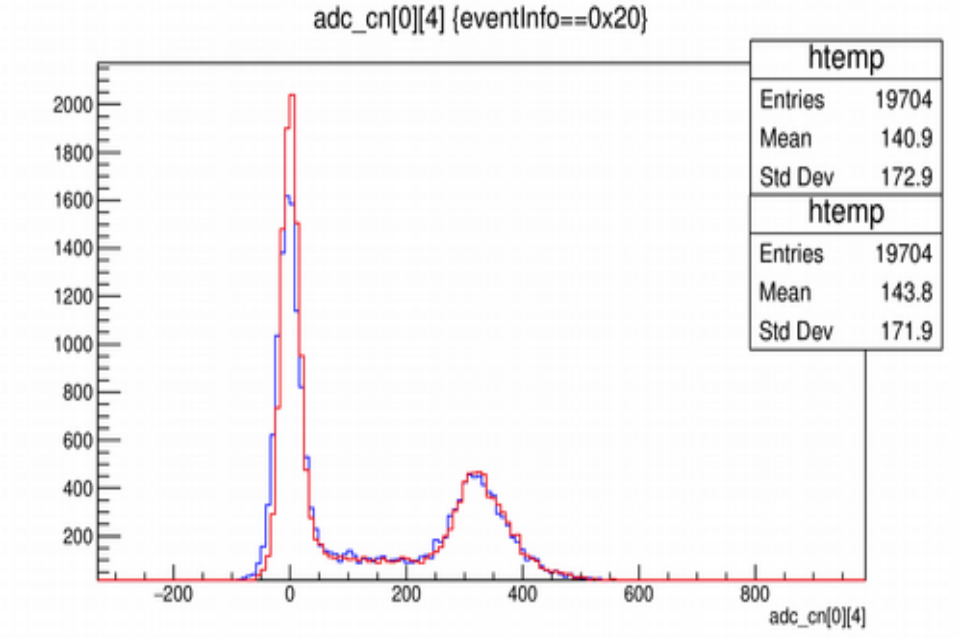



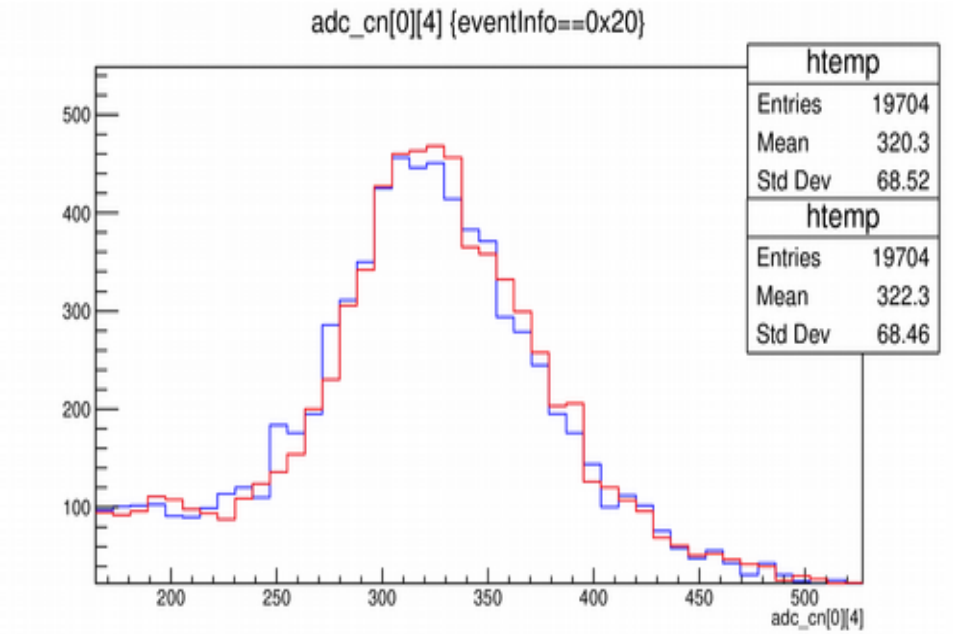

Even if we such a low signal and such a limited statistics, we could not see any evident signal decrease as a function of CASIS Time.

# MIP signal

without CN subtraction

with CN subtraction




The *MIP signal* is located around 320 ADC, so the expected **S/N ratio is about 21**

# Summary

After a HARD LABORATORY WORK we were able to obtain:

- almost stable pedestal VS casisTime
- RMS of pedestals around 15 ADC
- MIP signal around 320 ADC

**but...** it is not clear if we will be able to repeat such a good configuration scheme for all channels on the assembled prototype

**TODO**:

- understand why chip 2 (from 0) appears to be always in low gain even if the digital output signal GAIN is always low (high gain)
- test the calibration mode
- test the self trigger