# HiDRA2 Calibration mode

Eugenio and Lorenzo, XX YYY 2020

# Outline

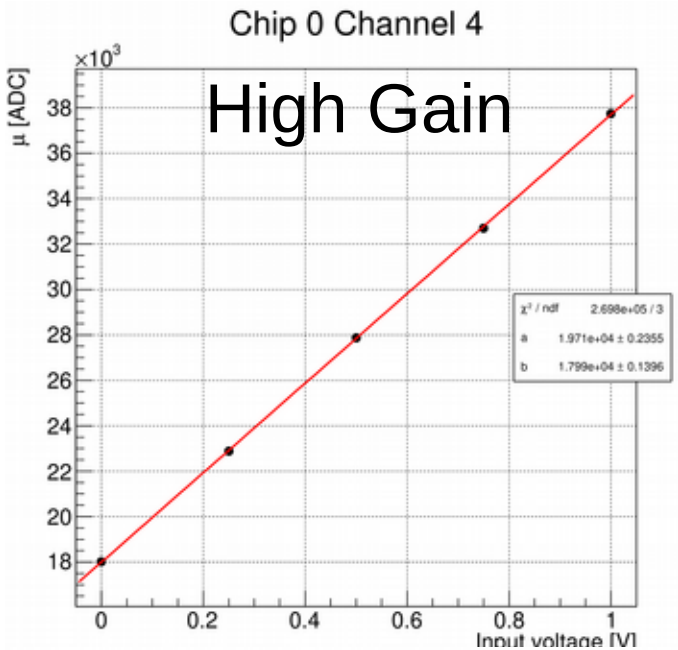
**PURPOSE** Test calibration mode on the HiDRA board 6

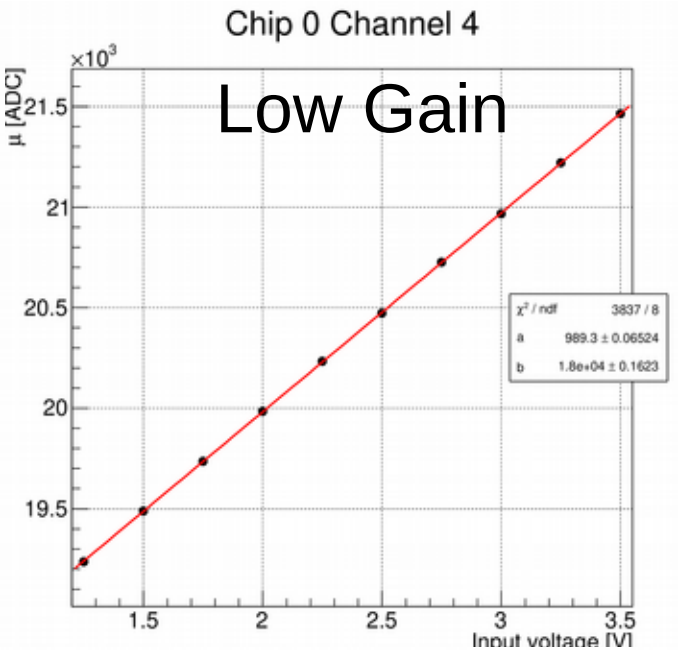
**METHOD** Data acquired in three different configurations:

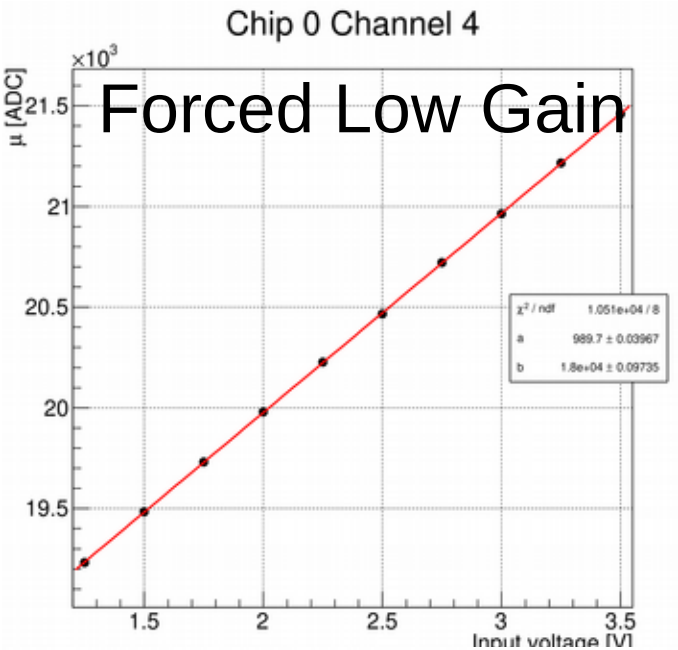
- For High Gain - $V_{cal}$ in [0, 1] V
- For Low Gain - $V_{cal}$ in [1.25, 3.5] V
- For Forced Low Gain (G2SEL on) - $V_{cal}$ in [1.25, 3.5] V

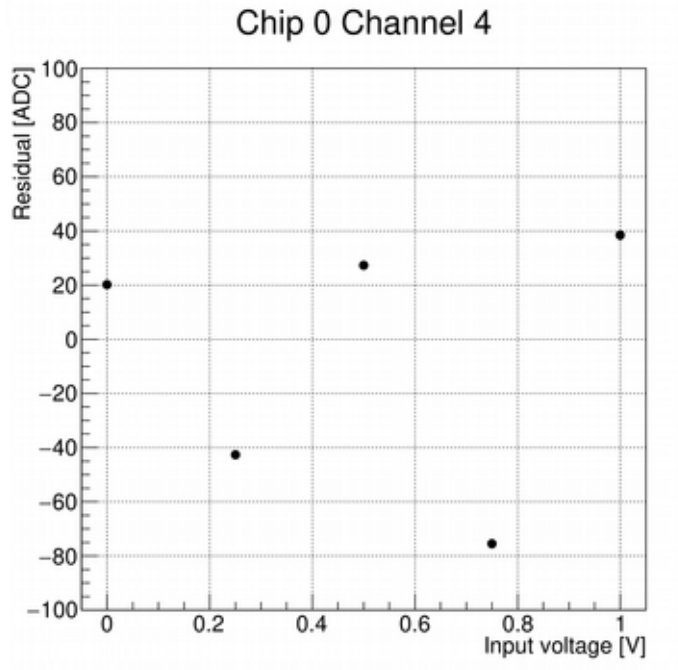
**CAVEAT** Among the four chips mounted on the board, the first two work correctly, whereas strange a behavior was found on the last two (both in acquisition and calibration mode): for this reason we present here the results relative to the channels of the **first chip** only.

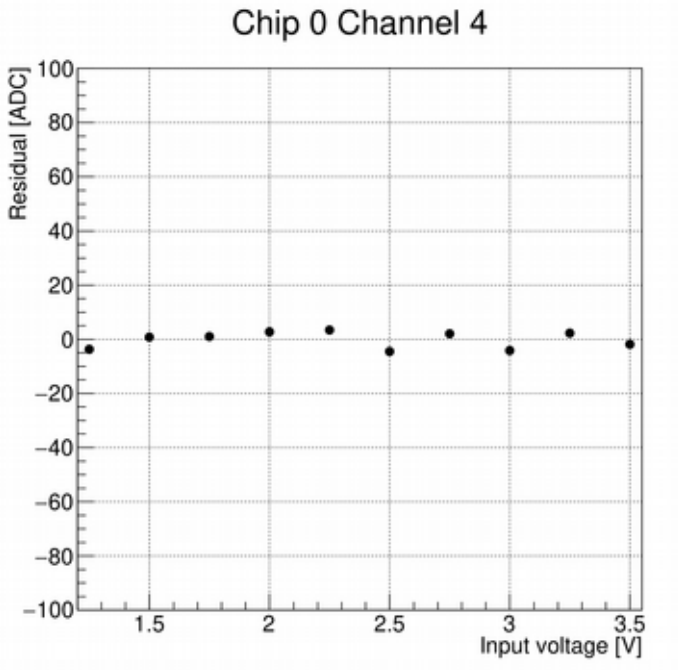
# HiDRA Gain - Chip 0 Channel 4

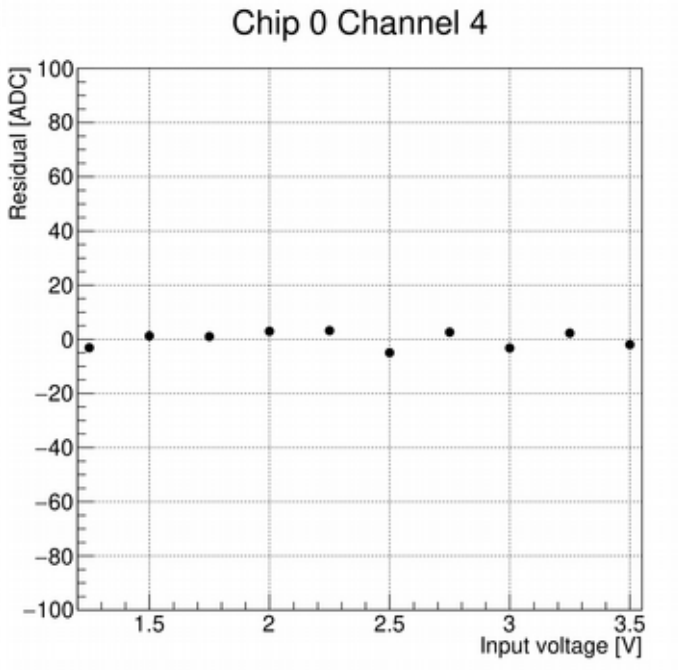


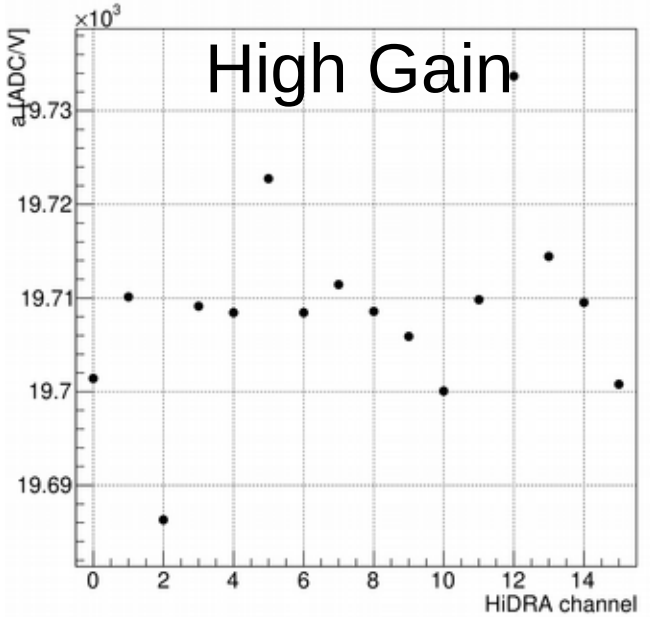



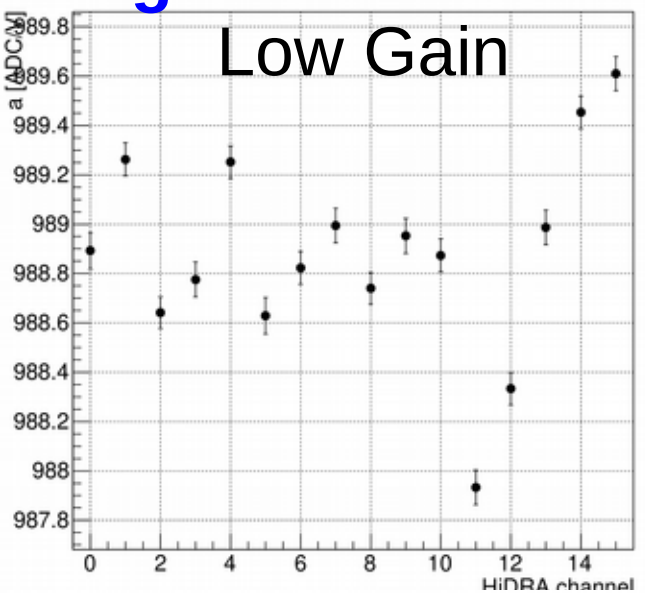



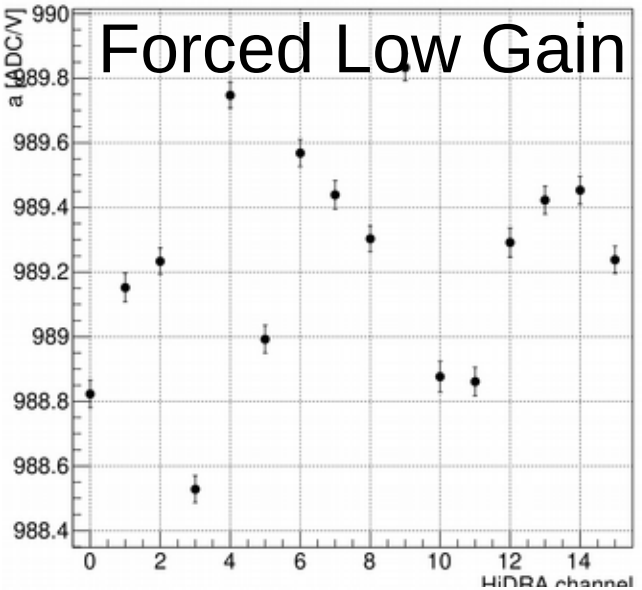



# Linear Coefficient - Chip 0

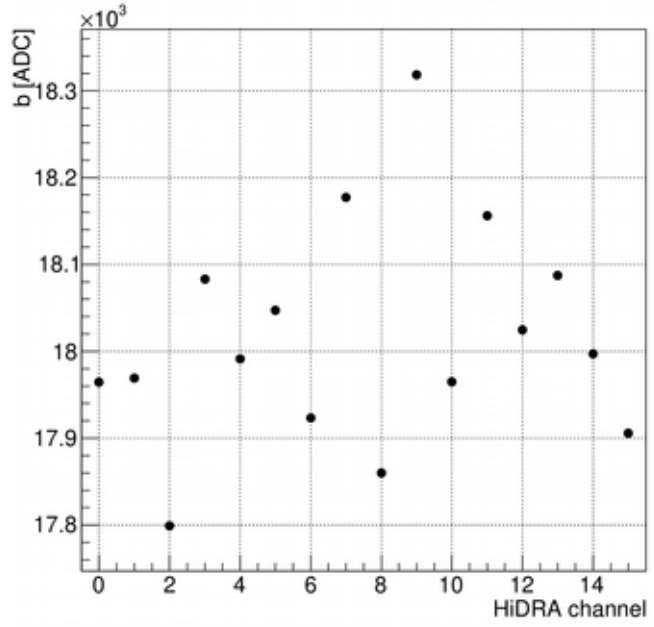
**AngularCoefficient**

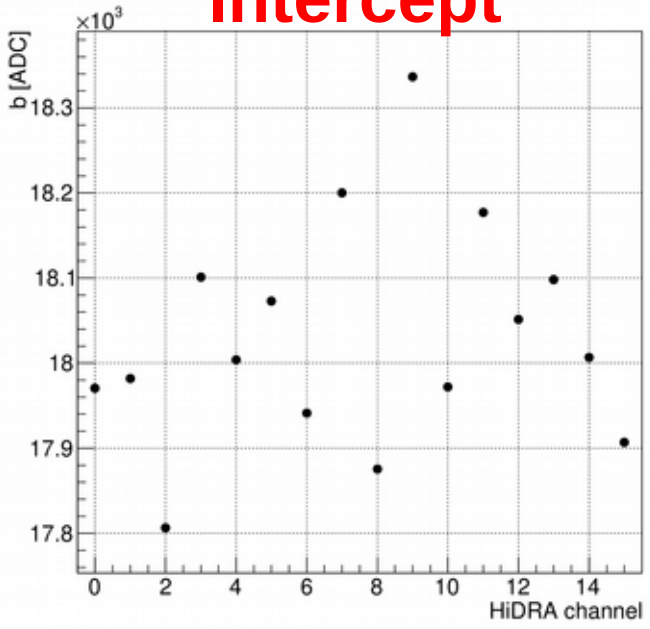


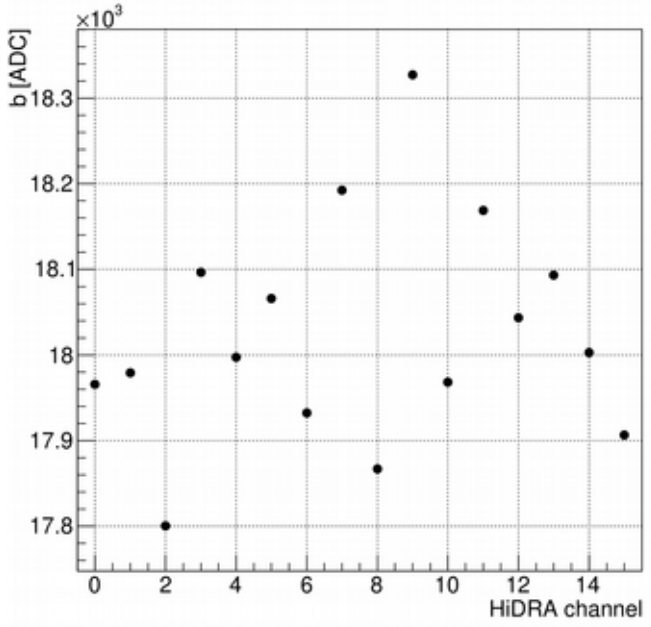




**Intercept**

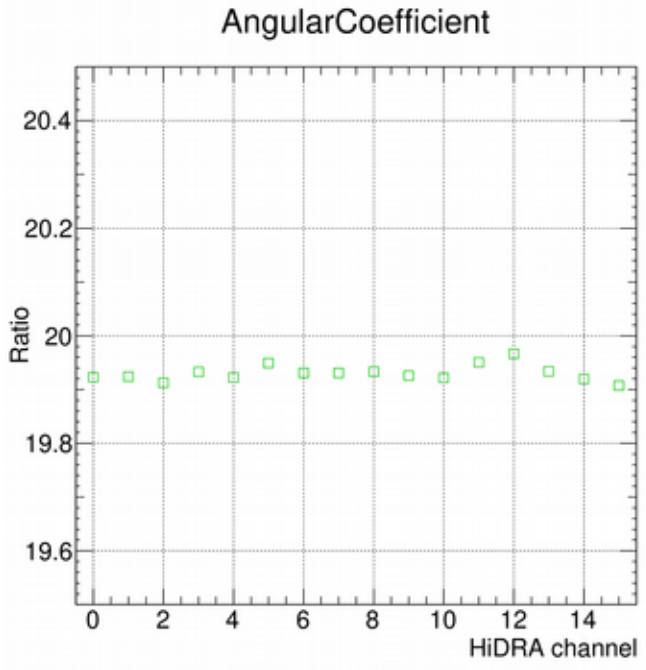


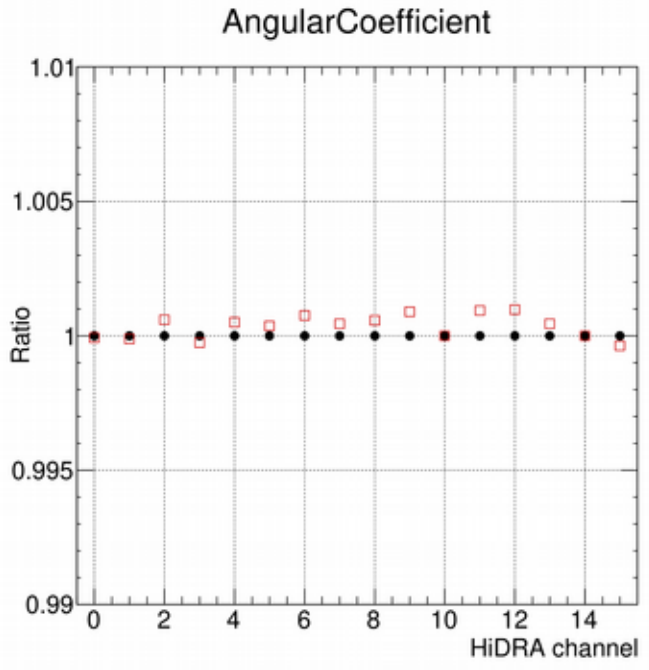



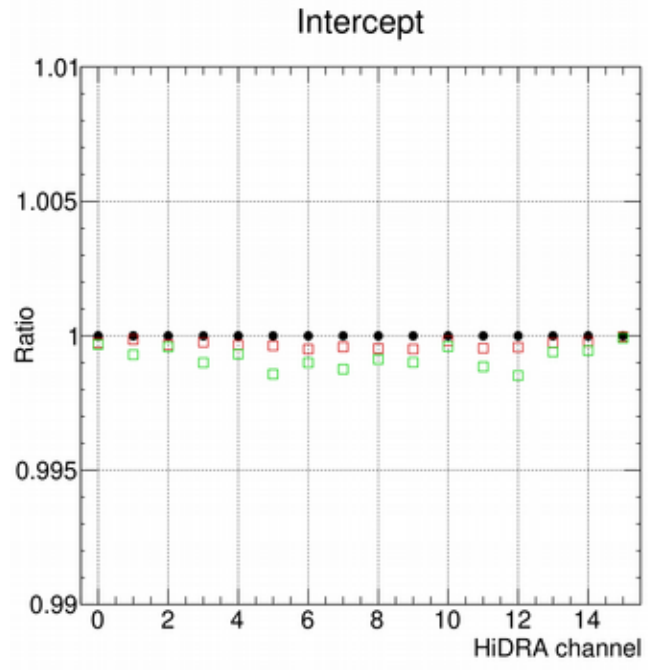



# Linear Coefficient Ratio - Chip 0

High Gain
Low Gain
Forced Low Gain

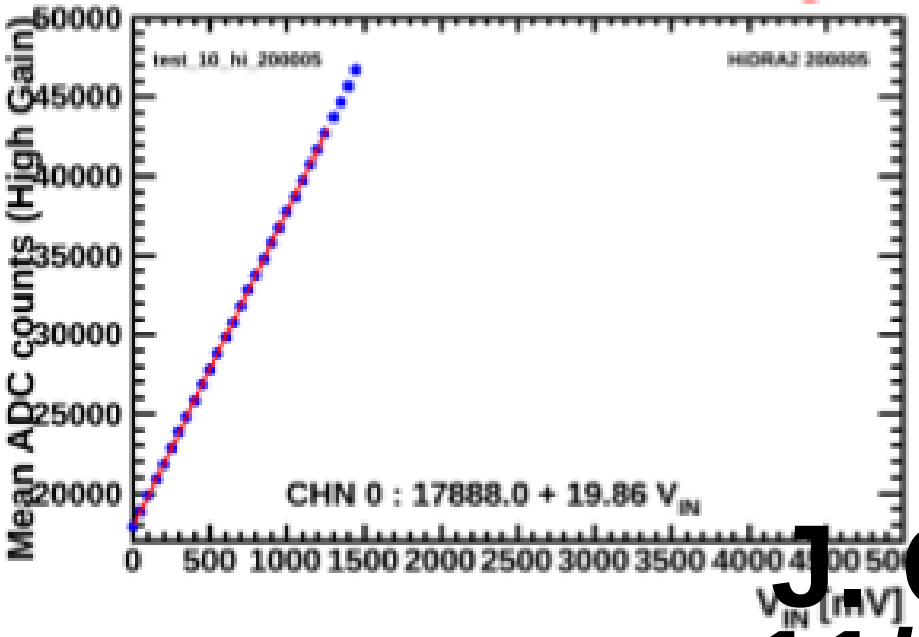


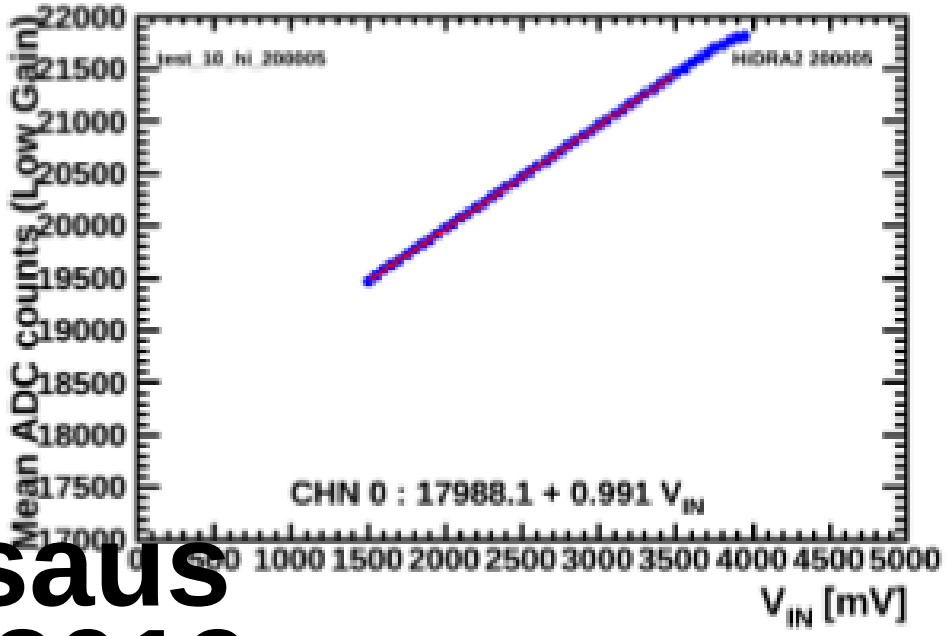



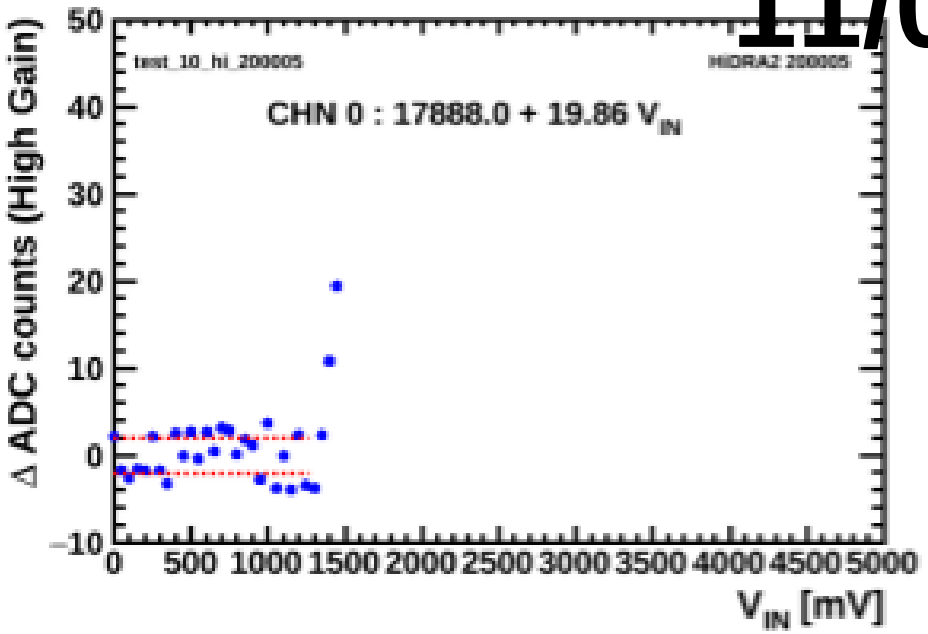
# Back Up

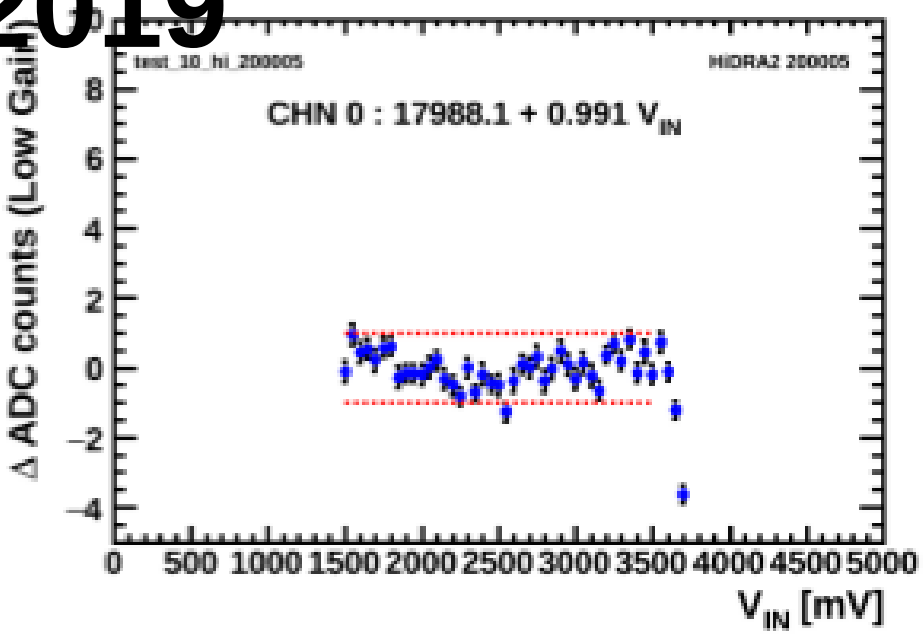
# Gain Calibration: Linearity Range in High & Low Gain



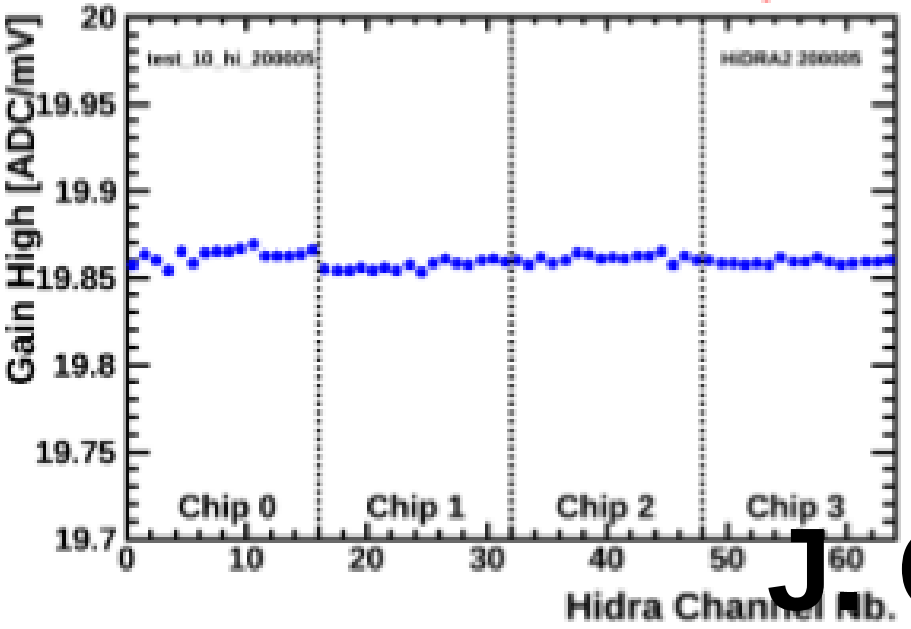



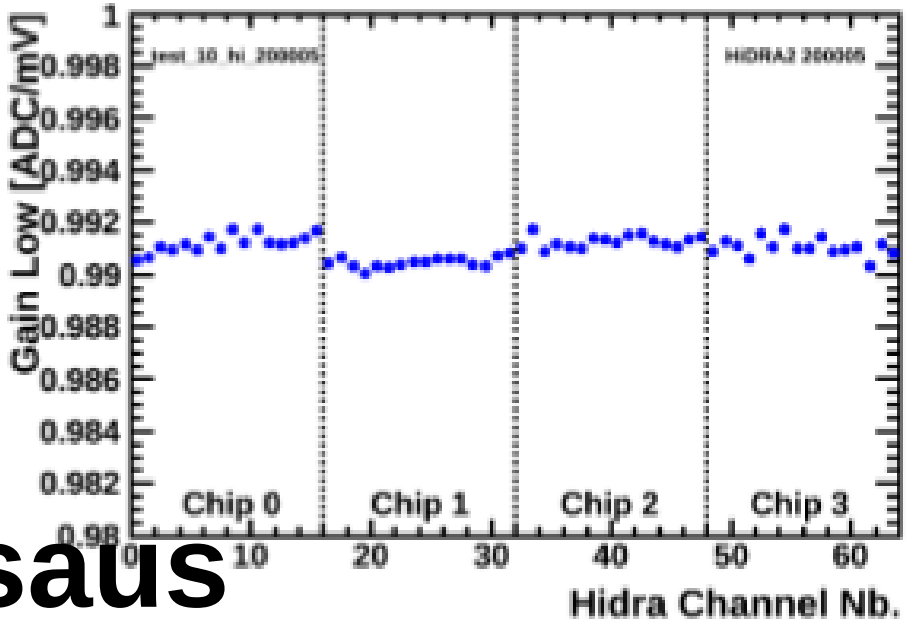

**J.Casaus**
**11/04/2019**



# Gain Calibration: Channel Uniformity in High & Low Gain

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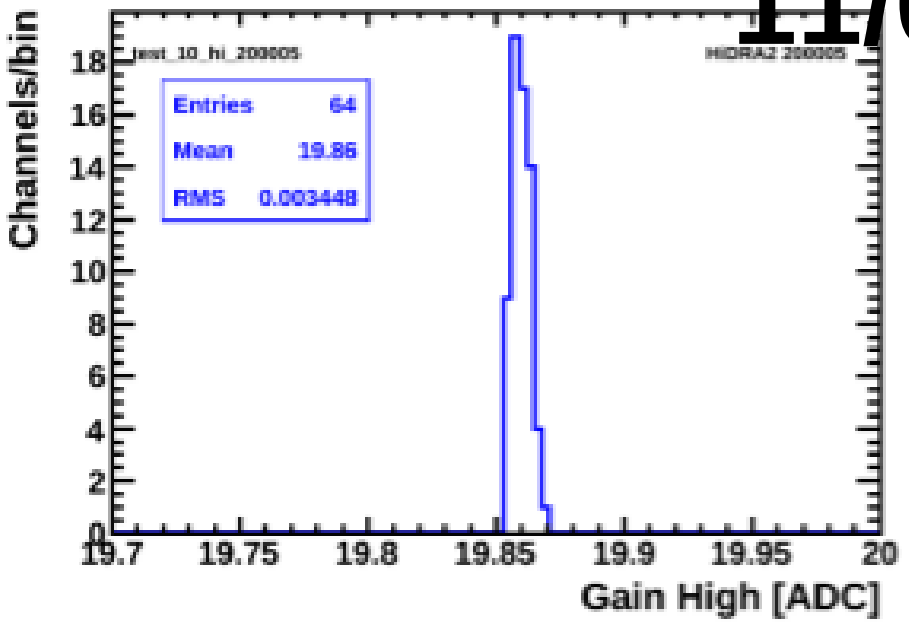


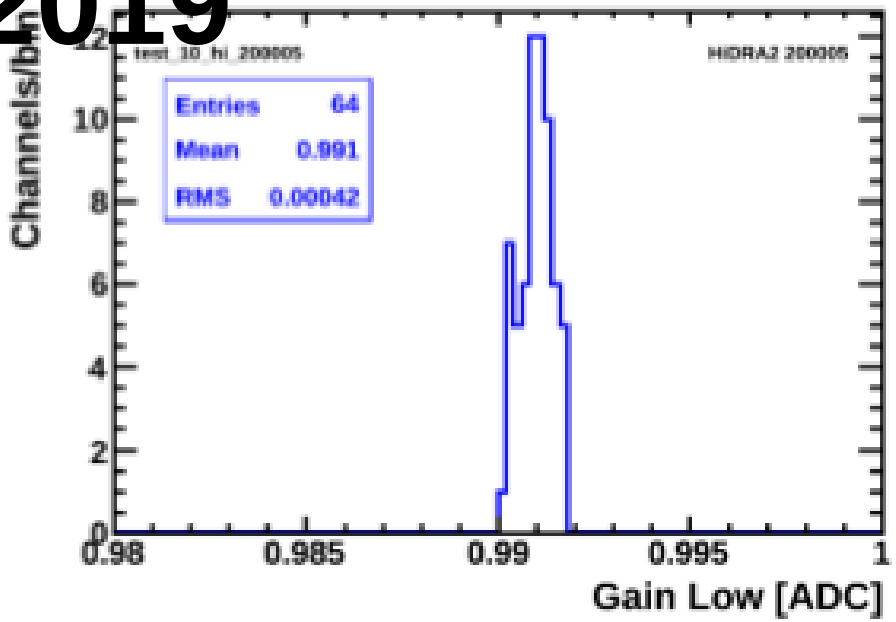

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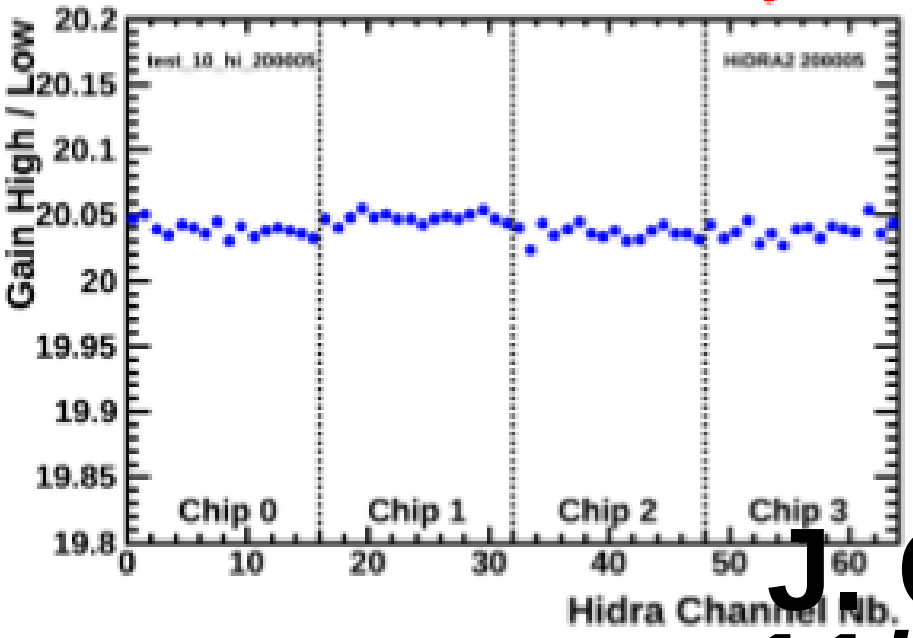


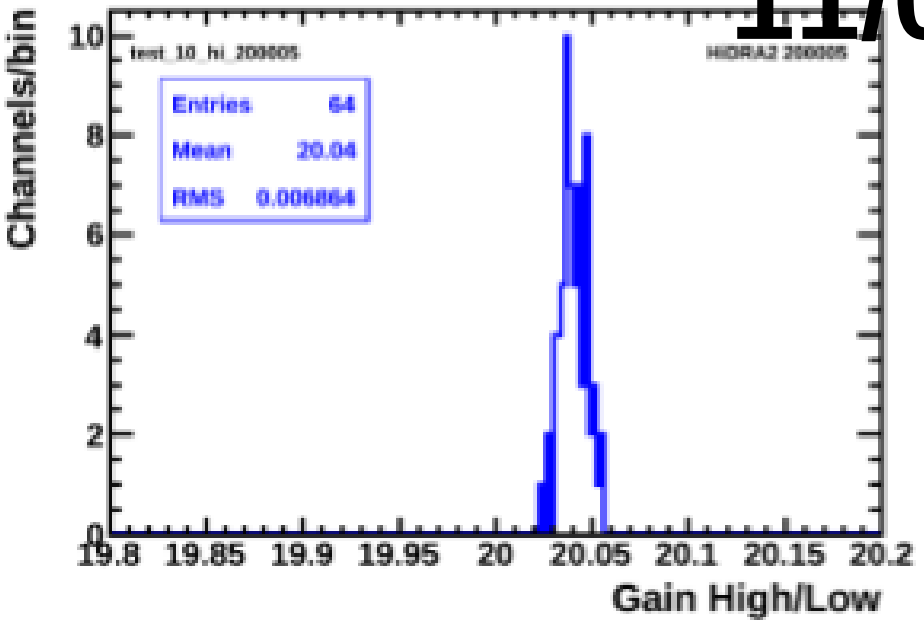


Results on HiDRA2 Board 200005

Pedestals & Noise :

- Pedestal values in the 17500 – 18200 range
- Noise in the range 10 – 14 ADC with a clear odd-even channel structure

Gain

- Average High Gain 19.86 ADC/mV
- Average Low Gain 0.991 ADC/mV
- Average High/Low 20.04
- All channels within 0.1% of the average

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**11/04/2019**