RD53:
Readout architecture and trigger

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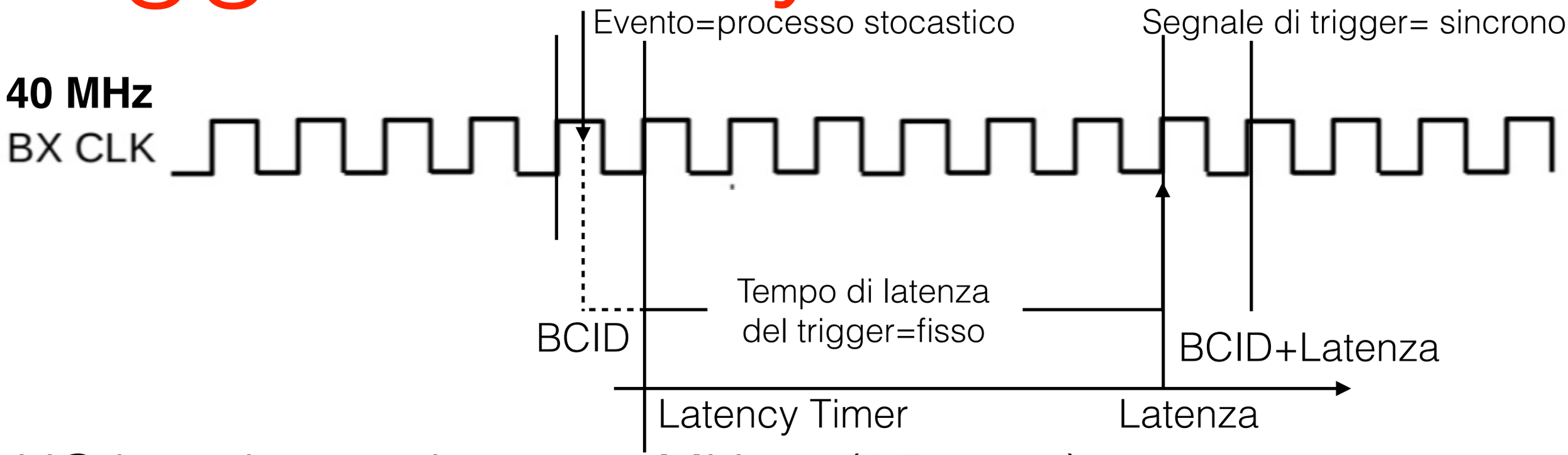
Trigger latency and readout



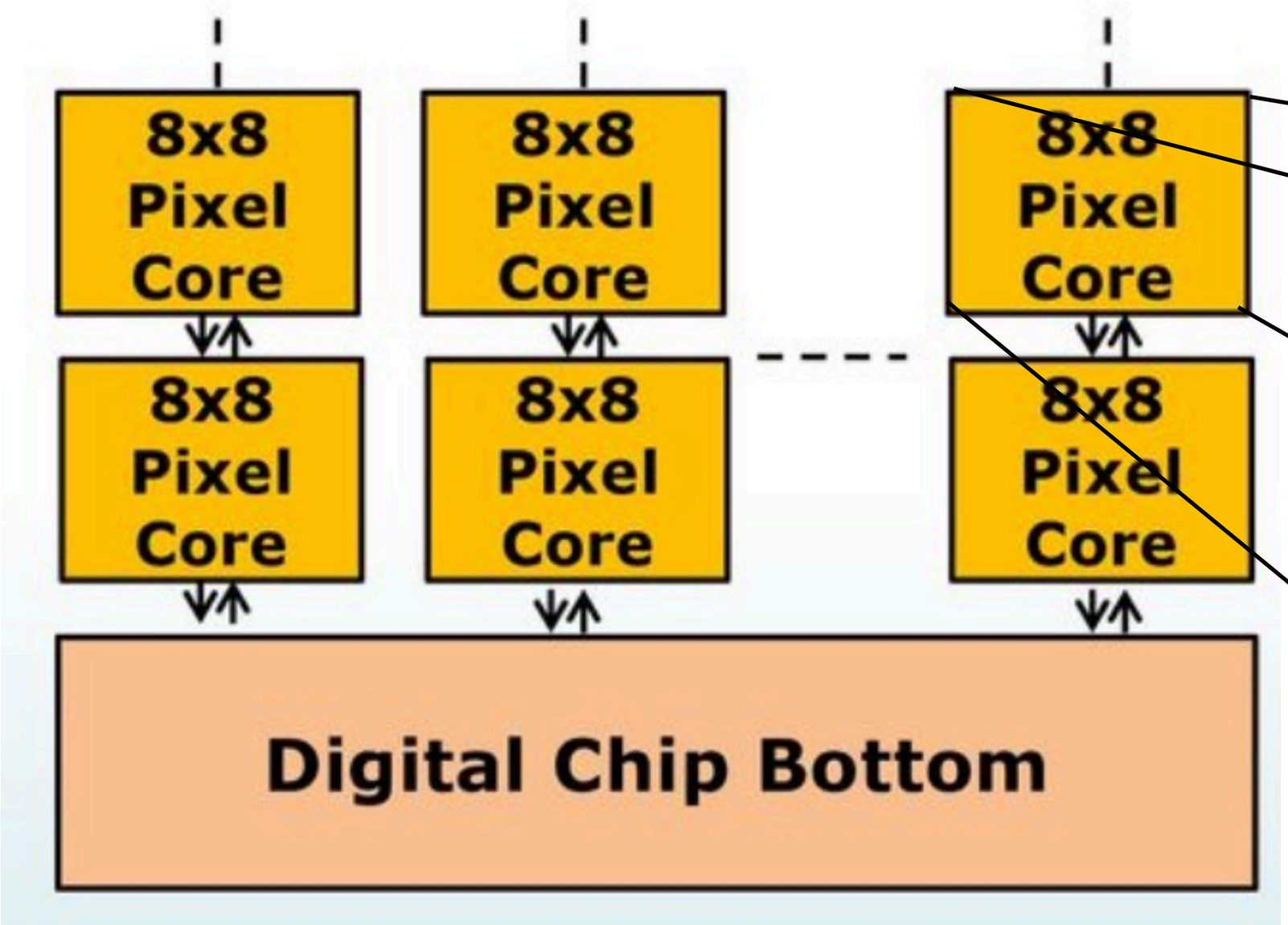
LHC bunch crossing = 40 MHz = $(25\ \text{nsec})^{-1}$

RD53a BCID =15 bit = 0-32767 = 0-0.8192 ms
E’ un free counter che si azzera dopo 0.8192 ms e riparte da zero.

Pixel region Latency Timers = 9 bit = 0 - 511 =12.8us
Sono counter sincroni con il BCID che iniziano a contare quando arriva un hit o più hit nella regione all’interno di uno stesso bunch crossing e che vengano azzerati (se non arriva il trigger) o taggati con il trigger ID in attesa di essere letti (se arriva il trigger) quando raggiungono il Latency Time programmato nel chip.

Digital Matrix

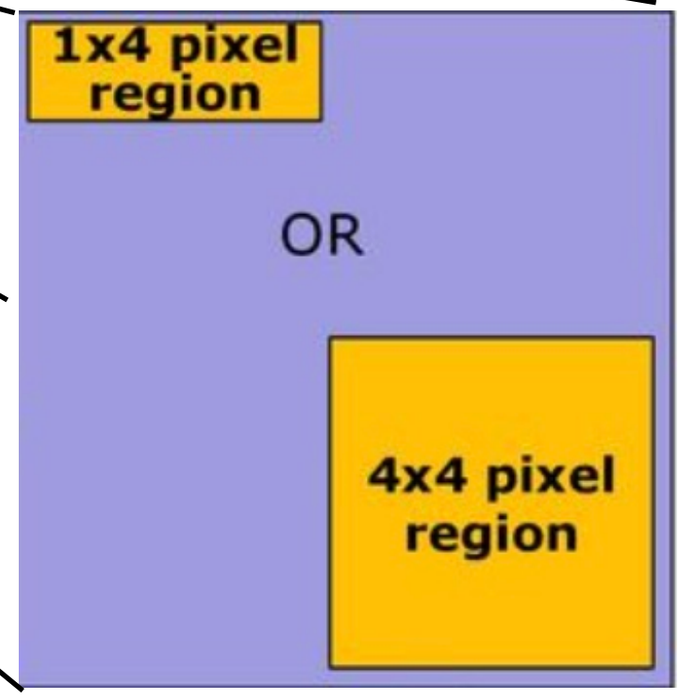
192 x 400 pixel = 24 x 50 Pixel Core



Macro Pixel = Region

It contains the Trigger Latency Buffering of all pixel hits (High Rate).

DBA: 8 x 2 = 16 region

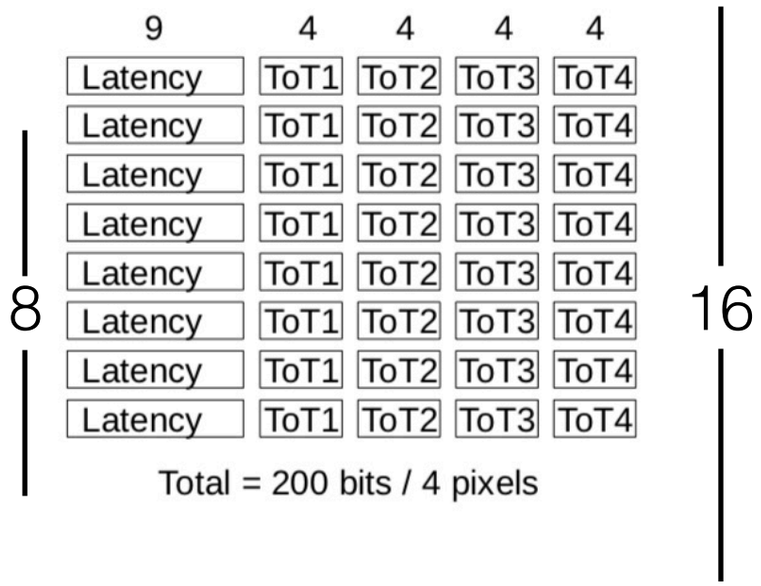


CBA 2 x 2 = 4 region

Un Pixel Core riceve i segnali digitali di uscita dal Pixel Core precedente e li rigenera per il Pixel Core successivo fino a trasmetterli alla parte digitale globale del chip (Digital Chip Bottom) che comunica con il mondo esterno.

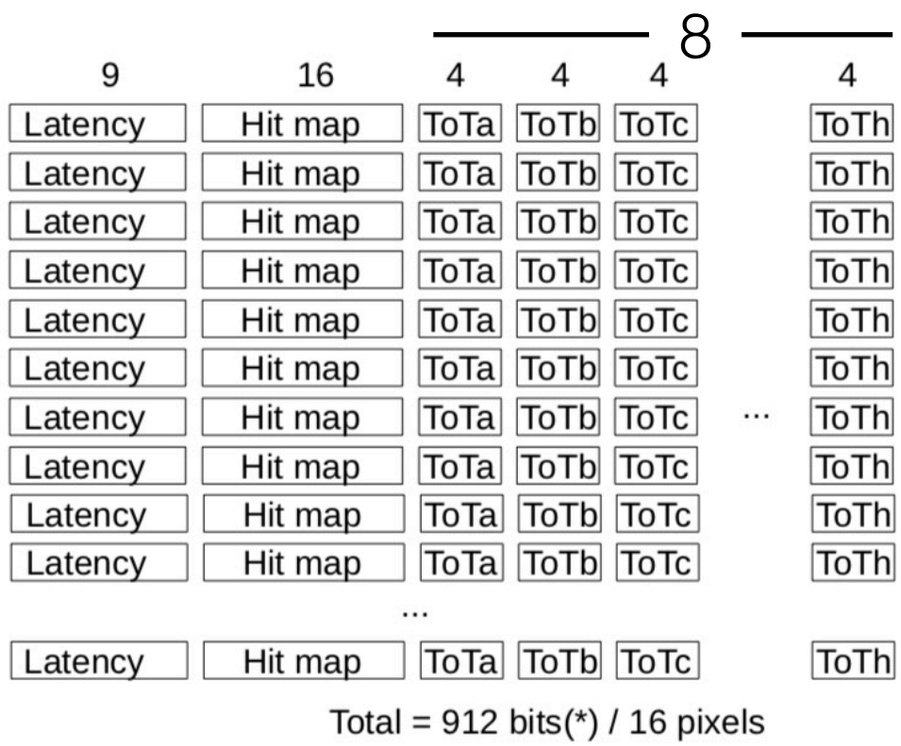
Buffer Architecture of Region

Distributed
LIN FE e DIFF FE



DBA

Centralized (più area e più power)
SYNC FE



CBA

TOT's stored by pixels.
"Waste" memory storing zero ToT, but needs no hit map.
Efficient for small number of pixel/region (few TOT=0).
8 TOT buffer/pixel and 8 Latency Timers/region

TOT are stored in a common memory block.
It have to store a hit map.
Efficient for a high number of pixel/region (many TOT's=0).
A region hit starts a Latency Timer and write in the hit map register. The hit map writing is closed after a delay to wait for all TOT which are saved up to 8 following a fixed priority queue. Above 8 hits/Latency Timer loose TOT but not map hit. Up to 4 hit map registers can be open in writing mode, the other hit are lost.

Trigger

Generazione segnale di trigger:

1. Attraverso il Command Decoder Block (CMD)
2. External Trigger Signal
3. Self trigger not implemented (next version) but can be externally generated using the chip-or output signal

Azione del segnale di trigger:

- Distribuito a tutte le Pixel Region per salvare tutti gli hits il cui la Latency Timer ha raggiunto in quell'istante la Trigger Latency programmata nel chip.
- Aggiunge nella Trigger Table le informazioni relative a quel trigger:
  ID (5bit:0-31), TAG (7 bit) = CODE(5 bit:0-31)+BUNCH POSITION (2bit:0-3), BCID (15 bit:0-32767)
- BCID is equal to the current value of the BC counter minus LATENCY
- The BCR command reset the BC counter to synchronise the CHIP with the DAQ.
- A Trigger Table entry is cleared once the Data Readout starts: First In - First Out

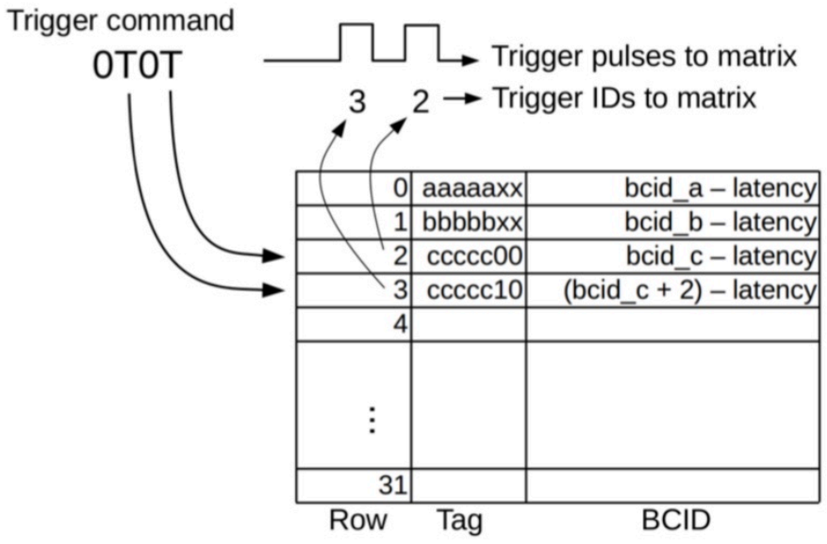


Figure 40: Trigger Table (TT) with example of filling with one trigger command encoding two triggers (first and third bunch crossings).

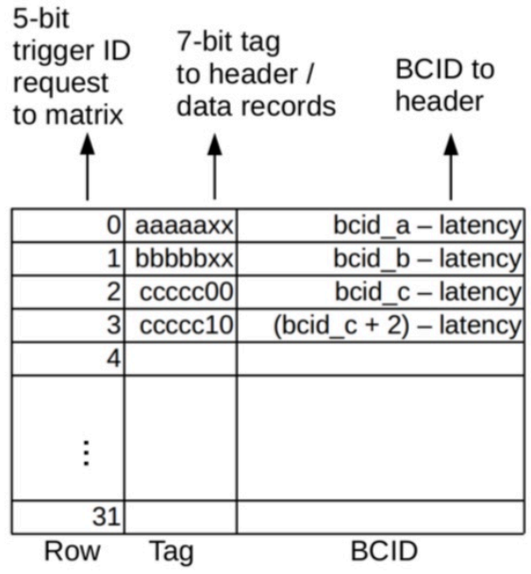


Figure 41: Illustration of how Trigger Table (TT) is emptied by data readout.

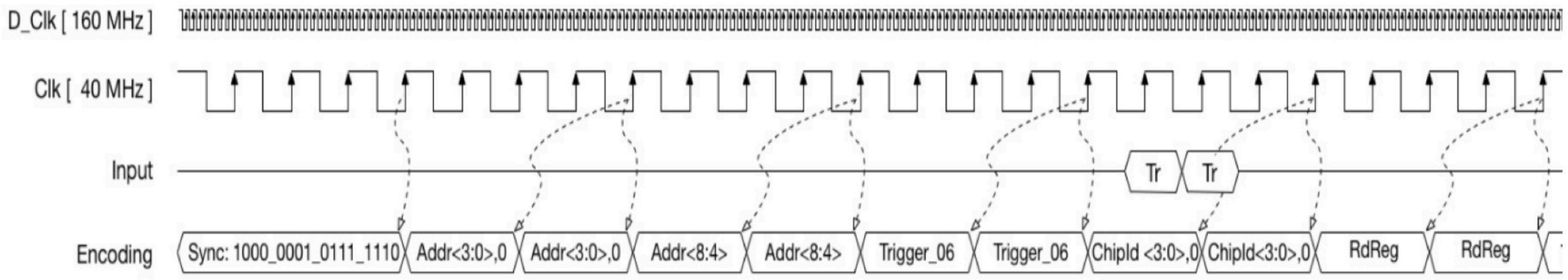
Comandi di Trigger

Generazione comandi di trigger:

1. Un comando di trigger è lungo 16 bit ed è scritto a 160 MHz e quindi impiega 4 BC per essere scritto (BXa,BXb,BXc,BXd).
2. Nel comando di trigger bisogna specificare quale dei 4 BC sono triggerati, cioe' il Trigger Pattern (15 possibilità codificate in 8 bit) e quale è il Tag (32 possibilità codificate in 8 bit)

Symbol Name	Encoding	Trigger Pattern	Symbol Name	Encoding	Trigger Pattern
			Trigger_08	0011_1010	T000
Trigger_01	0010_1011	000T	Trigger_09	0011_1100	T00T
Trigger_02	0010_1101	00T0	Trigger_10	0100_1011	T0T0
Trigger_03	0010_1110	00TT	Trigger_11	0100_1101	T0TT
Trigger_04	0011_0011	0T00	Trigger_12	0100_1110	TT00
Trigger_05	0011_0101	0T0T	Trigger_13	0101_0011	TT0T
Trigger_06	0011_0110	0TT0	Trigger_14	0101_0101	TTT0
Trigger_07	0011_1001	0TTT	Trigger_15	0101_0110	TTTT

Table 3: List of trigger command and symbols used to encode the 15 possible trigger patterns spanning four bunch crossings. Note there is no 0000 pattern as that is the absence of an trigger.



Serie di comandi SYNC + READBACK di un registro + TRIGGER. Nota come il comando di trigger arriva tra la scelta dell'indirizzo del registro e del ID del chip e il comando di READBACK.

Readout

Readout proceeds with column-parallel token chain, one trigger tag at-a-time.

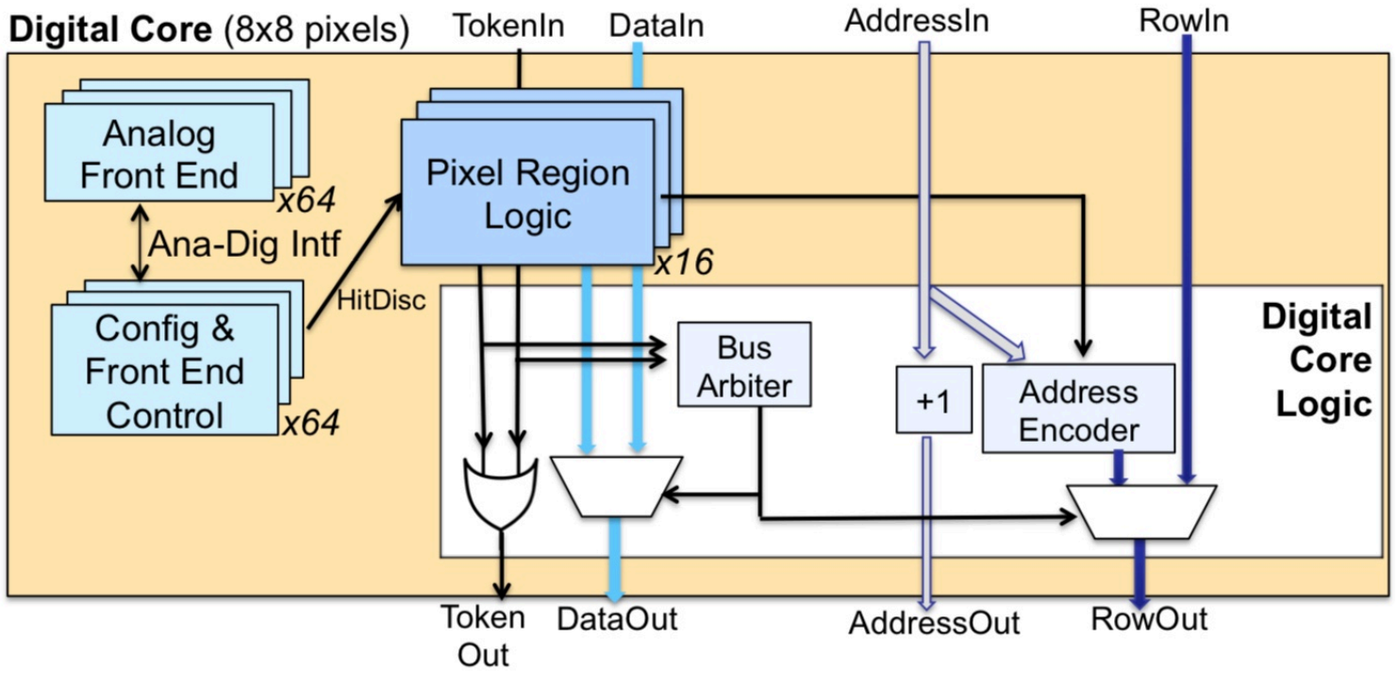


Figure 31: Block diagram of digital core with multiple regions.

TokenIn: LOW/HIGH: DataOut, Address Out, RowOut from (Previous) Pixel Core

DataOut: Hit Position in Region, TOT, Trigger Tag

AddressOut, RowOut: Core (+Region?) Position

On the bottom of any column the pixel data corresponds to the ouput data of the Pixel core with TokenIn HIGH which are flushed one hit at the time at 160 MHz clock.

When a Pixel Core doesn't have any hit to readout corresponding to the current trigger ID the TokenOut goes HIGH which is connected to the TokenIn of the next Pixel Core. If the next Pixel Core doesn't have data corresponding to the current trigger ID the TokenIn is passed to the next-to-next Pixel core.

Digital Bottom of the Chip

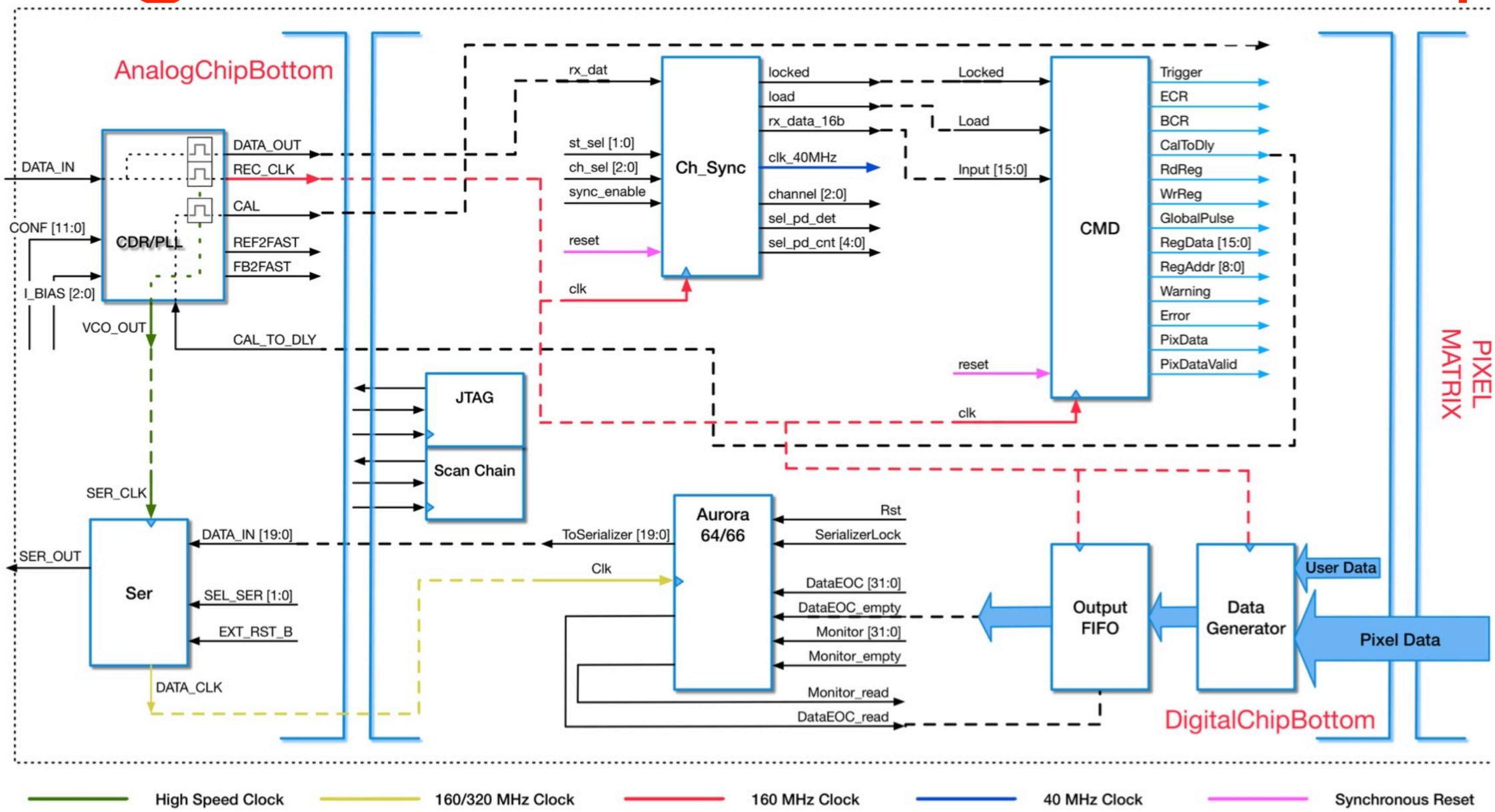


Figure 34: Block diagram of digital bottom of chip showing the command input and data output paths

Data (from Pixel Matrix and Configuration Register) are serialized out of the chip