Understanding the RD53 chip frontends

Including: “Never underestimate the joy people derive from hearing something they already know.” (E. Fermi)

E.J. Schioppa
Lecce, April 2020

RD53 specifications (2015)

Specification	Value	Comment or Test Conditions
Input polarity	Negative	
Interior pixel capacitance	<100 fF	this applies to most pixels
Edge pixel capacitance	<200 fF	see subsection on edge pixels
Interior pixel leakage current	<10 nA	
Edge* pixel leakage current	<20 nA	*see Sec. 5.2 for details
Min. stable threshold setting	600 e^-	With 50 fF load, 4 μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. charge above threshold resulting in <25 ns time walk	600 e^-	With 50 fF load, 4 μA/pixel analog. For free running discriminated pixel. See Sec. 3.1
Min. in-time threshold with free-running front end	1200 e^-	With 50 fF load, 4 μA/pixel analog. Simply the sum of the two above lines
Min. in-time threshold if using synchronous reset	750 e^-	With 50 fF load, 4 μA/pixel analog. See Sec. 3.1
Hit loss from in-pixel pileup	$\leq$1%	at 75 kHz avg. hit rate. See Sec. 3.2
Recovery from saturation	<1 μs	See Sec. 3.2 for discussion
Trigger rate	1 MHz	

Trigger latency	12.5 μs	
Noise occupancy per pixel	$< 10^{-6}$	50 fF load; in a 25 ns interval
Single pixel noise (ENC)	design-dependent	See Sec. 3.1
Radiation dose	500 Mrad	delivered at -15 C. Room T annealing only
Temperature range	-40C to +40C	
Current consumption, analog	4 μA/pixel	periphery consumption not included
Current consumption, digital	<4 μA/pixel	periphery consumption not included
Current consumption, Total	<500 mA/cm^2	Note this is 1 W/cm^2 at 2 V input
SEU's affecting full chip	<0.05/hr/chip	in 1.5 GHz/cm^2 particle flux
SEU's affecting single pixel	<100/hr/chip	in 1.5 GHz/cm^2 particle flux
Charge scale shift	<2% / Mrad	change in mean with radiation
Threshold scale shift	<15 e^- / Mrad	change in mean with radiation
Threshold dispersion	<60 e^- / Mrad	added in quadrature
Charge meas. dispersion	<0.1 MIP/Mrad	added in quadrature

Critical performance specs (innermost layer)

Input capacitance

Johnson-Nyquist theorem*:
because of thermal noise, the charge on a capacitance fluctuates with

$$\langle Q \rangle = 0 \qquad \sqrt{\langle Q^2 \rangle} = \sqrt{kTC}$$

C	$\sqrt{\langle Q^2 \rangle}$
1 nF	12500
10 pF	1250
100 fF	125
1 fF	12.5

**one of the many specific cases of the fluctuation-dissipation theorem*

For a **single-sided** pn-junction:

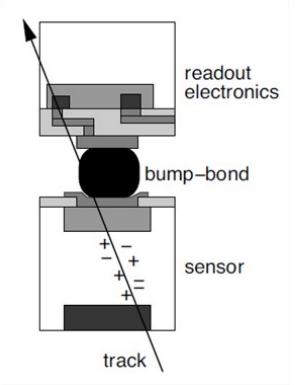
$$C = \frac{\epsilon A}{W}$$

surface of the junction

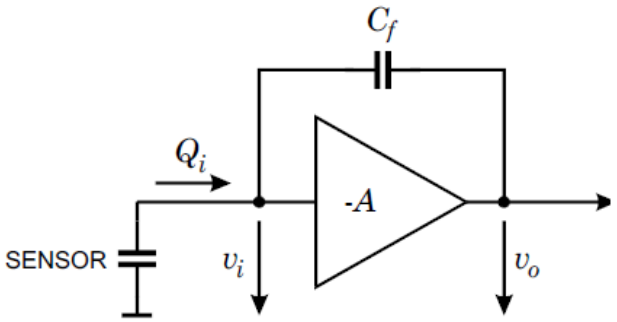
width of the depletion region

For a **hybrid detector**:

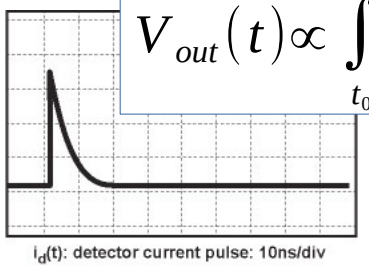
$$\frac{1}{C_{tot}} = \frac{1}{C_{sensor}} + \frac{1}{C_{bb}} + \frac{1}{C_{ro}}$$

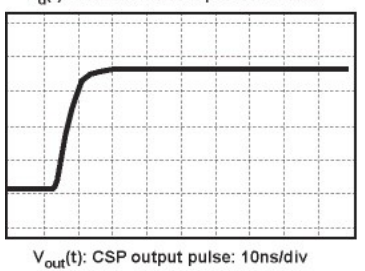


Charge sensitive amplifiers

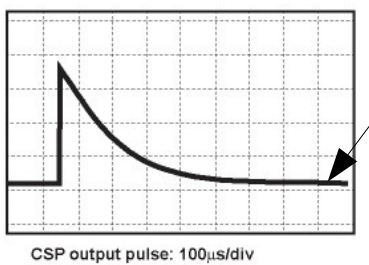


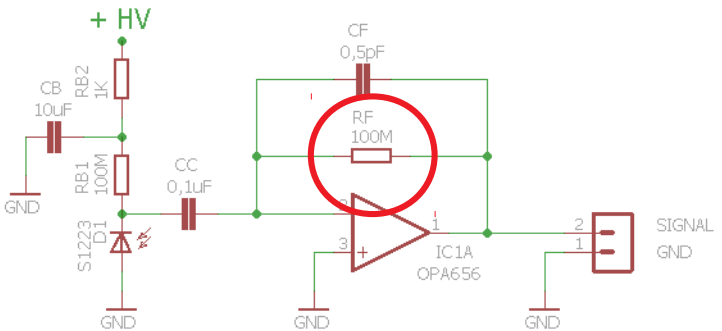
$$V_{out}(t) \propto \int_{t_0}^{t_0+t} I_{in}(t')\,dt'$$


i_d(t): detector current pulse: 10ns/div


V_{out}(t): CSP output pulse: 10ns/div

On a longer time scale

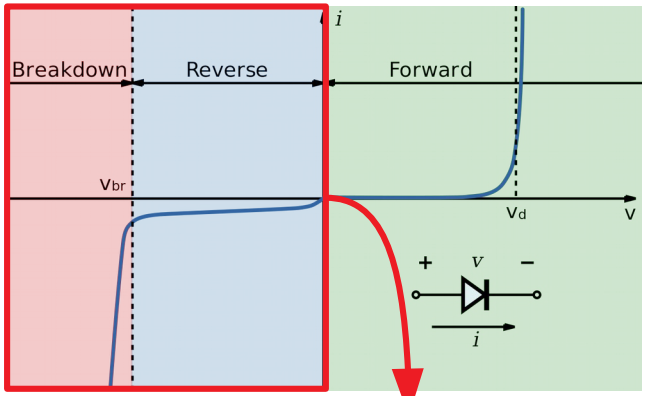

CSP output pulse: 100μs/div

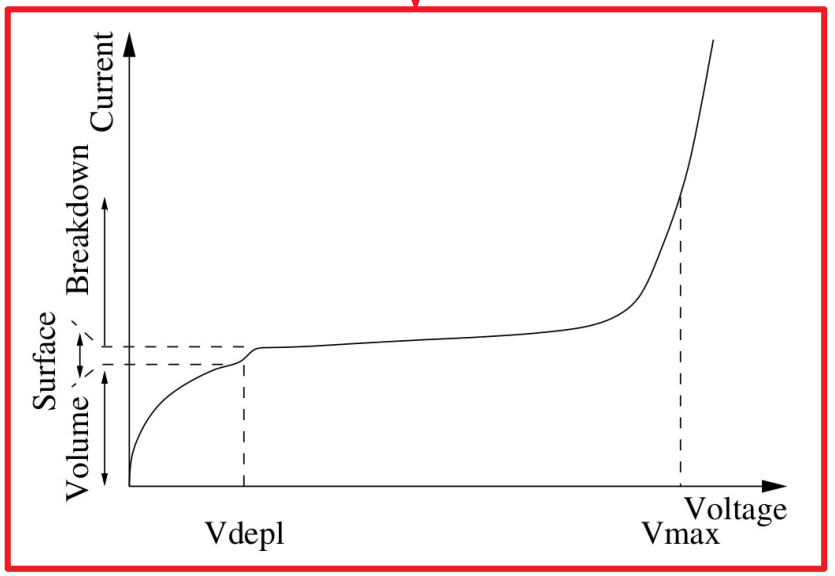


The easiest way to control the reset time

Now the circuit is ready for a new input

Leakage current





- In the depletion region, the only process that injects charge into the (reverse biased) junction is thermal generation
- The generation rate is something like

$$g = \frac{n_i}{\tau_g}$$

temperature dependence (exponential...)

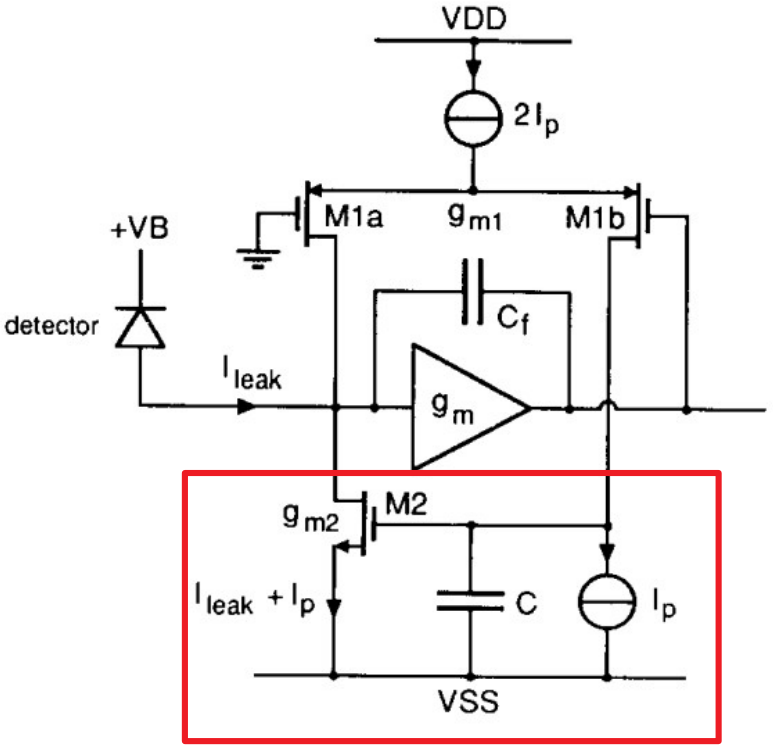
- The leakage current density is (just by dimensions)

$$J_{leak} = -e\frac{n_i}{\tau_g}W$$

where (single sided pn-junction)

$$W = \sqrt{\frac{2e\left(V_{bi}+V_{bias}\right)}{eN_{D/A}}}$$

The Krummenacher feedback circuit

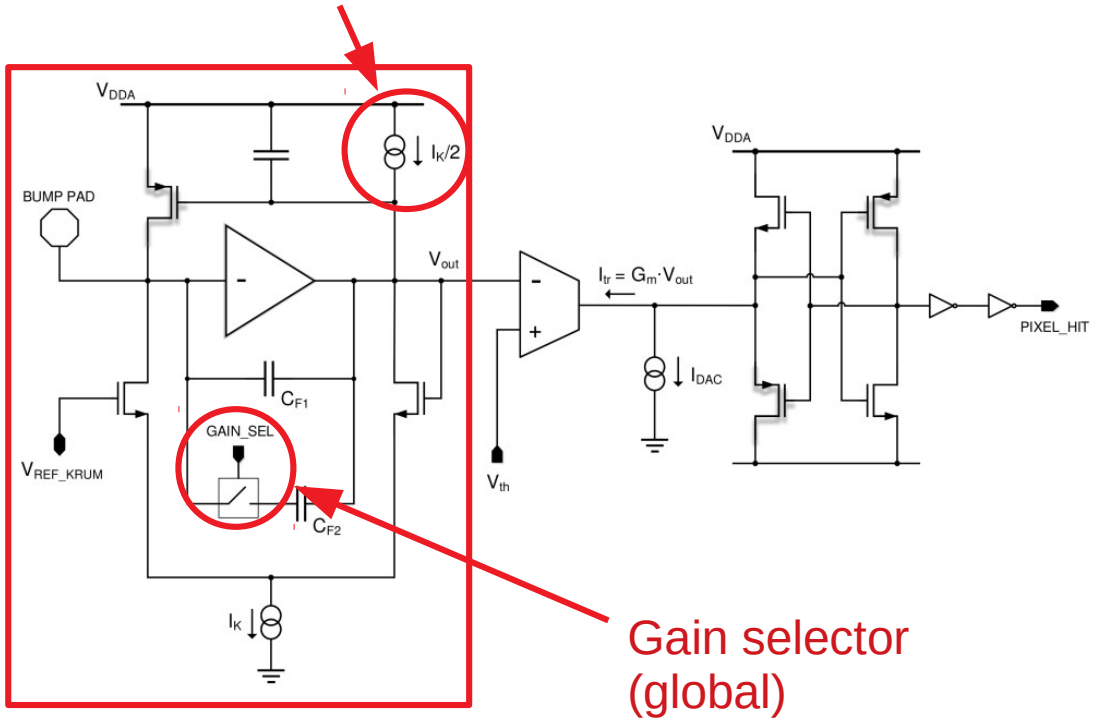


F. Krummenacher, Pixel detectors with local intelligence: an IC designer point of view, NIM A305 (1991) 527-532

- Add a second feedback loop to a CSA
- The leakage current is forced to flow through M2, and not through the first loop

The RD53 linear frontend

Global DAC in the periphery



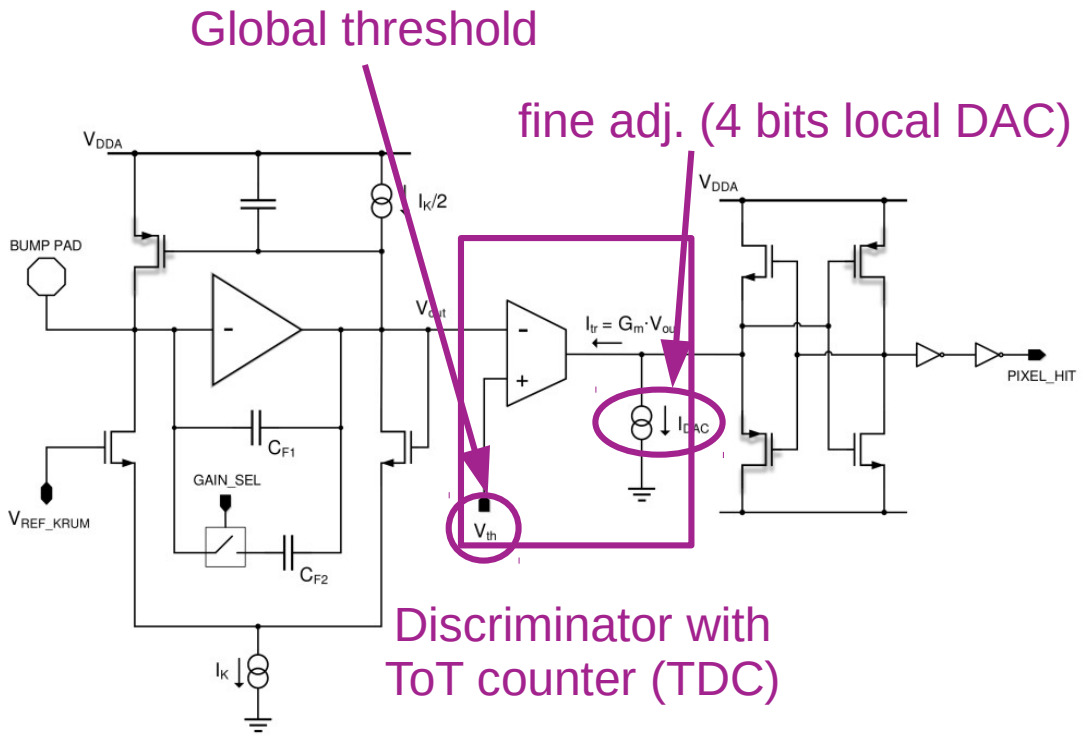
Gain selector (global)

Single stage with Krummenacher feedback

CSA:

- Low power (single stage)
- Q_{max} = 30ke-
- Current conspn. = 4uA (most of the full FE)
- I_k = 25nA @ high gain
  → ToT=400ns @ 30ke-
- High gain = 15mV/ke-
- Low gain = 7.5mV/ke-
- ENC = 87e- @ C_{in}=50fF

The RD53 linear frontend

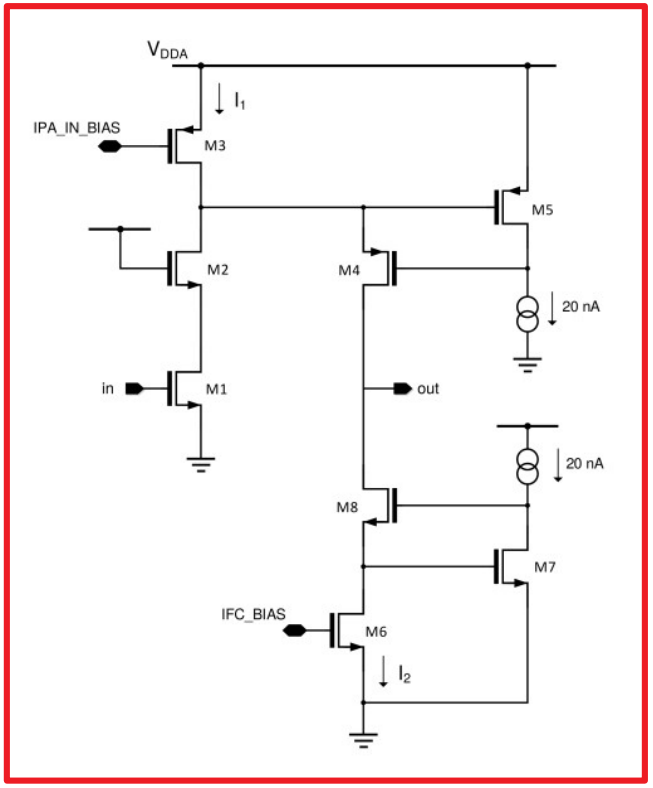


Discriminator

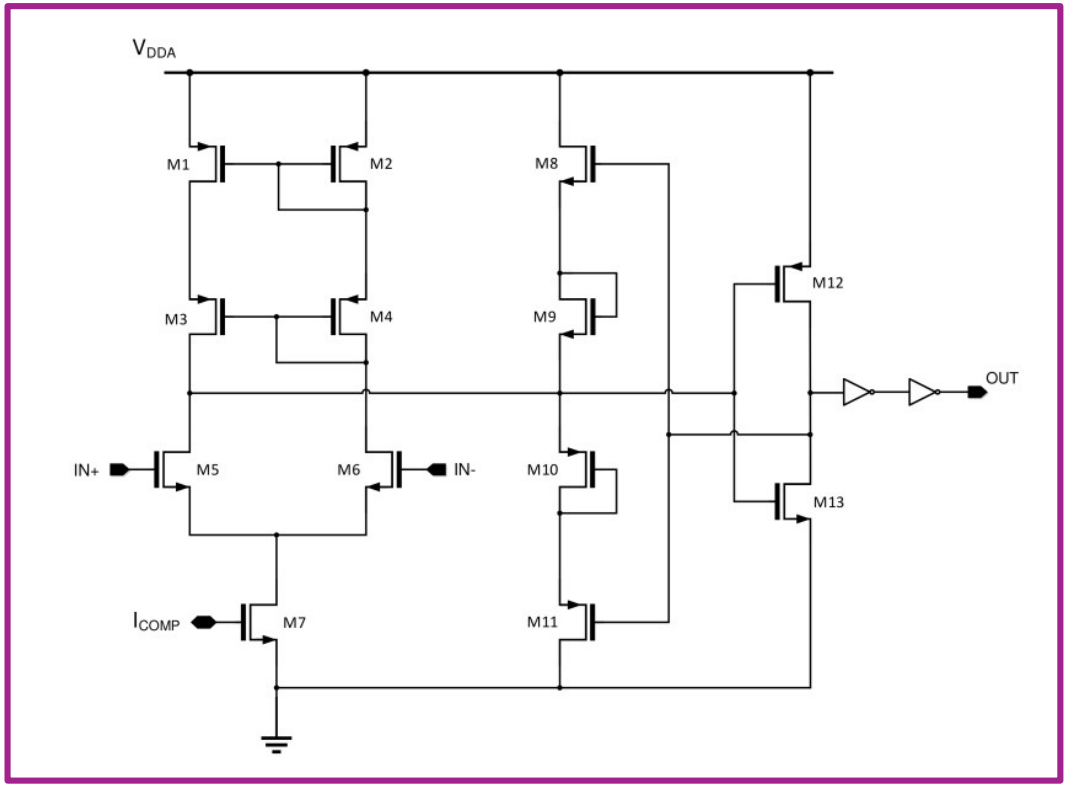
- High speed (fast switching)
- Low power
- Current comparison
- Threshold dispersion:
  - 380 e- before tuning
  - ISSUE: this value is huge
  - 35 e- after tuning

The RD53 linear frontend

CSA forward gain stage

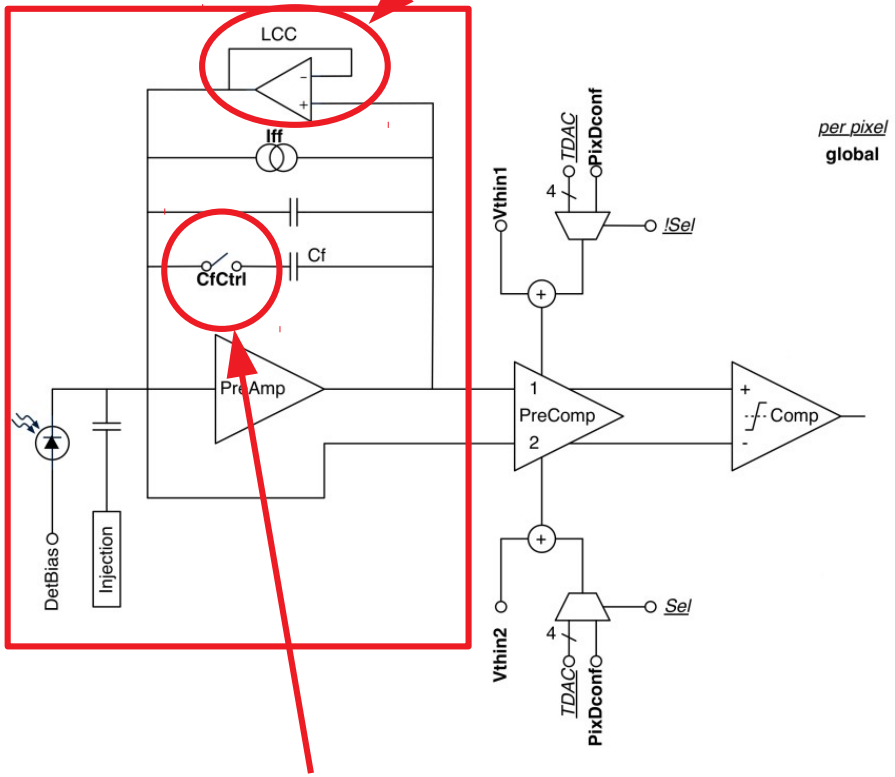


Threshold discriminator



The RD53 differential frontend

Leakage current compensation
(enabled/disabled globally)



Gain selector (global)

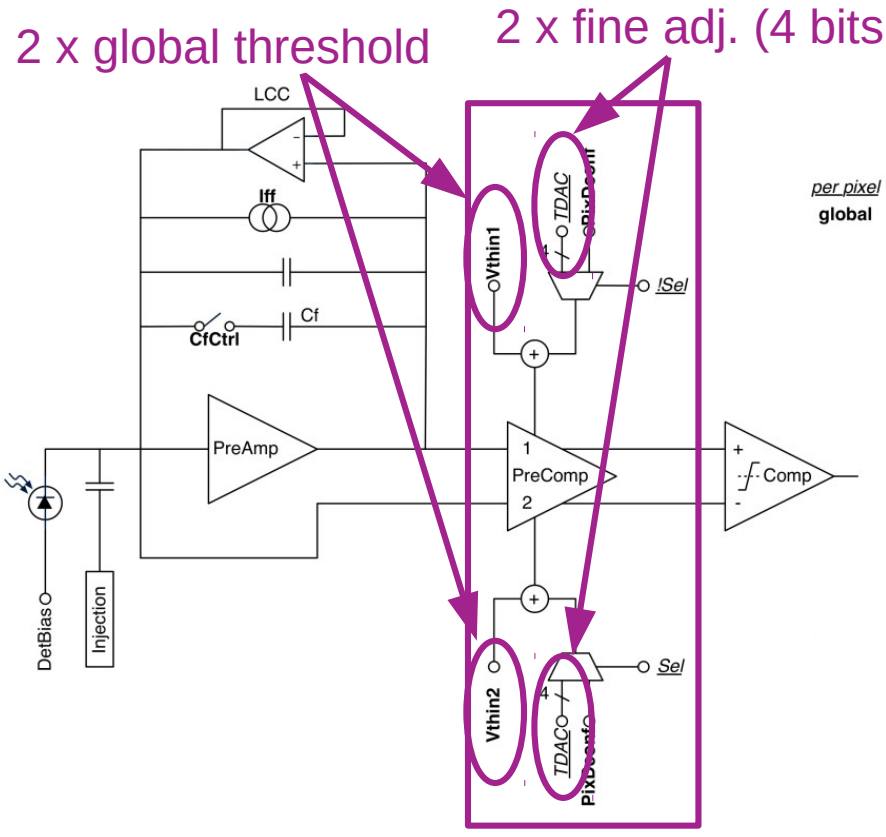
FE:

- Low power
- Small area
- Free running
- Purely analog
- Th_{min} = 500e-
- Current conspn. = 4uA @ C_{in}=50fF, I_{leak}=10nA

Preamplifier:

- Low current
- Continuous reset
- Small fall-time dispersion → no local feedback current adjustment
- The LCC is not needed (no saturation) when I_{leak}<10nA

The RD53 differential frontend

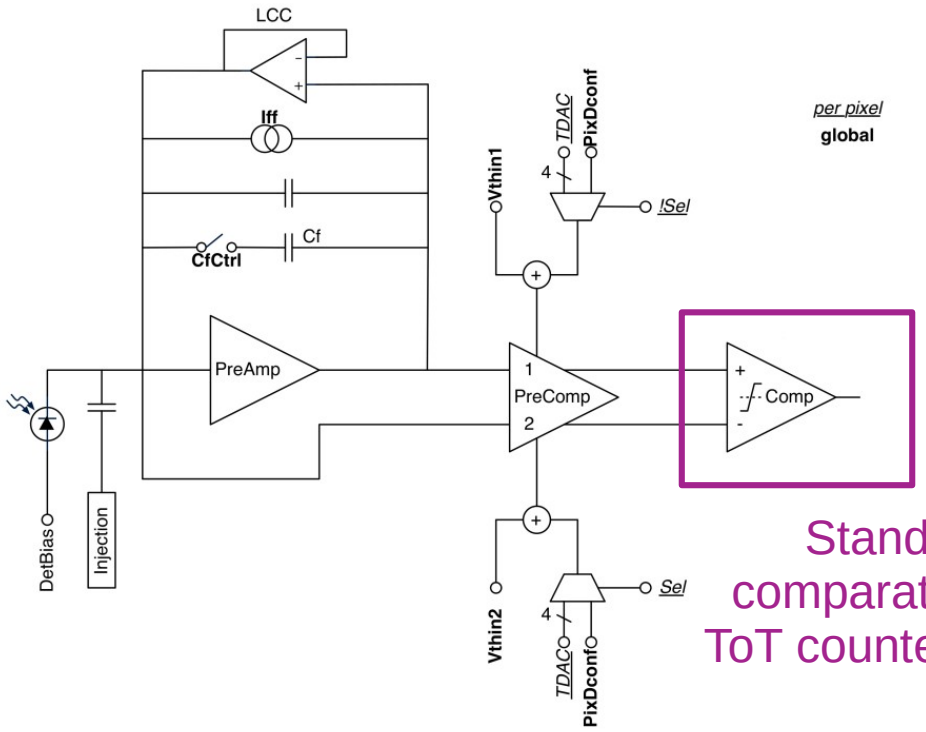


Pre-comparator

Pre-comparator

- Additional amplification
- Only one branch can be adjusted at a time (Sel bit, the other branch is set to all 0 or all 1 globally)
- Optimized for low threshold
- Differential = small mismatch variations
- Good power supply rejection (?)

The RD53 differential frontend

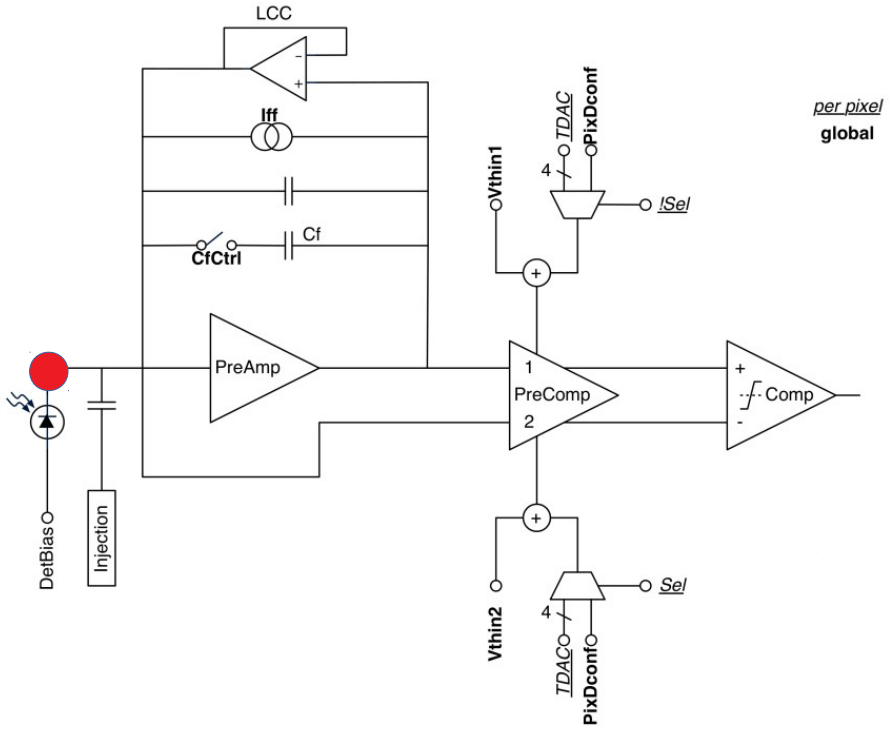


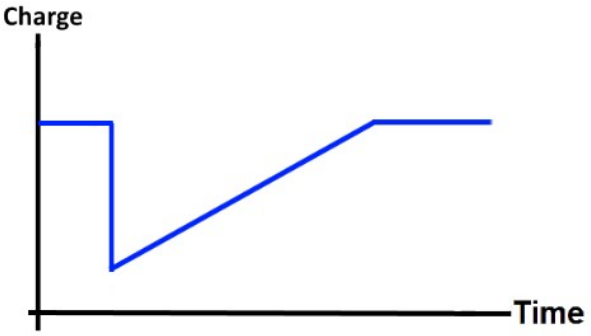
Standard comparator with ToT counter (TDC)

Comparator

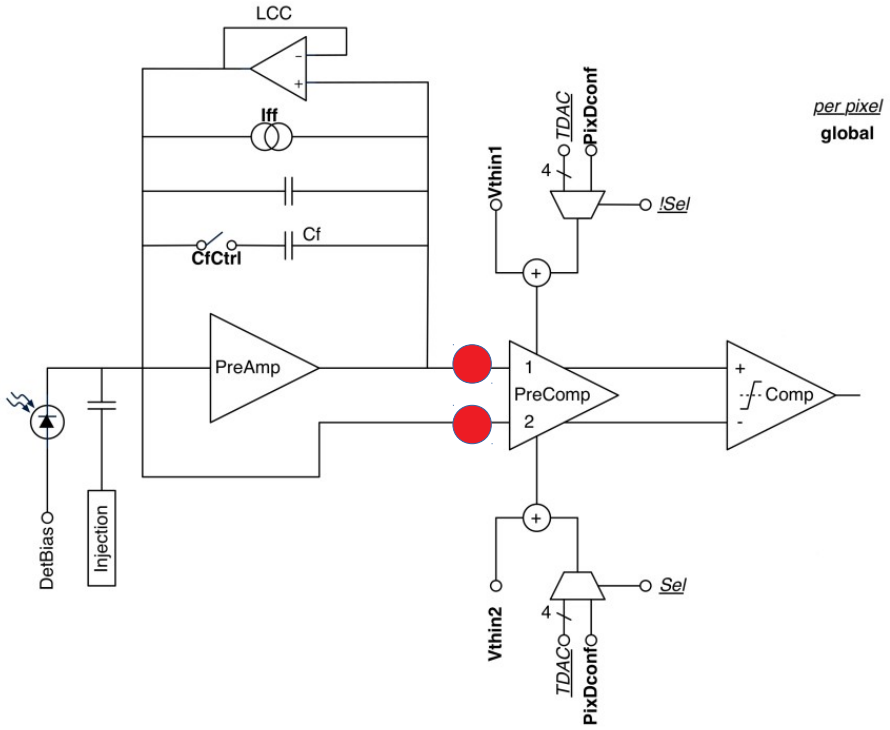
- ISSUE: Design bug → delay and ToT are not reliable for a sub-section of pixels → there exists a “good pixels mask” (for timing measurements)

The RD53 differential frontend

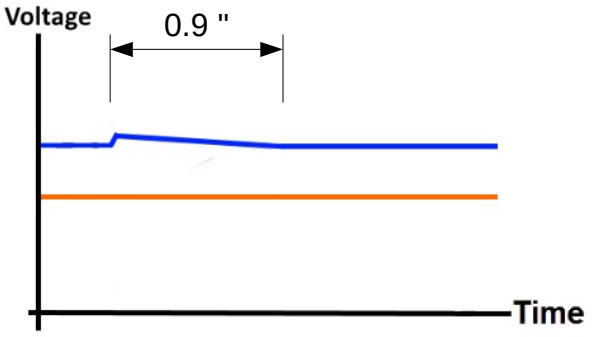




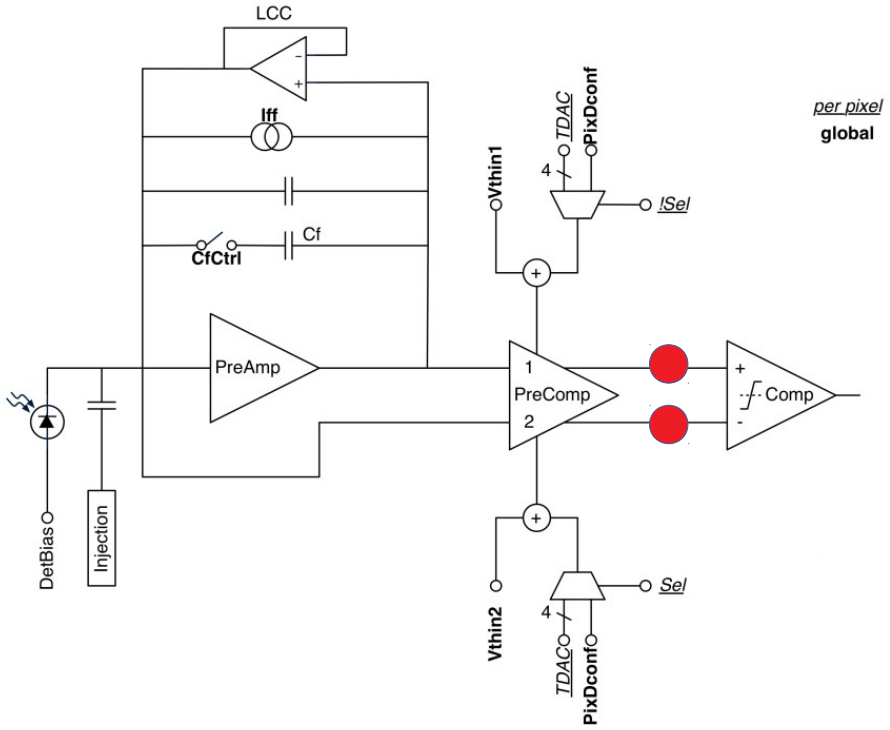
The RD53 differential frontend

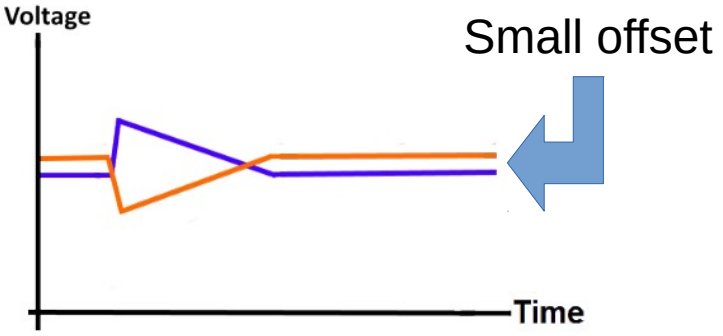


Signal length is proportional to Q

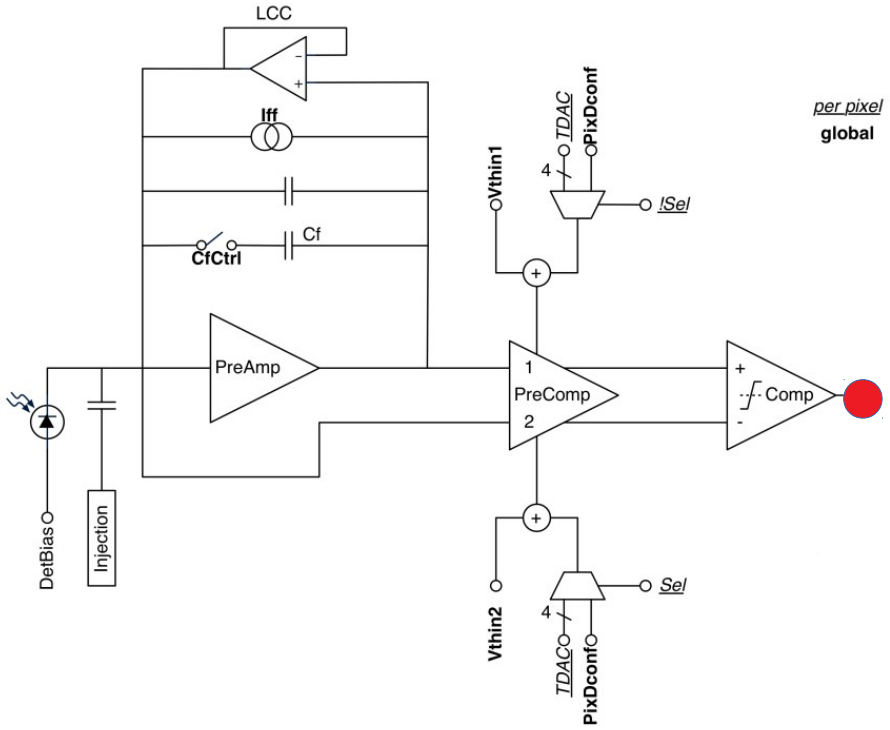


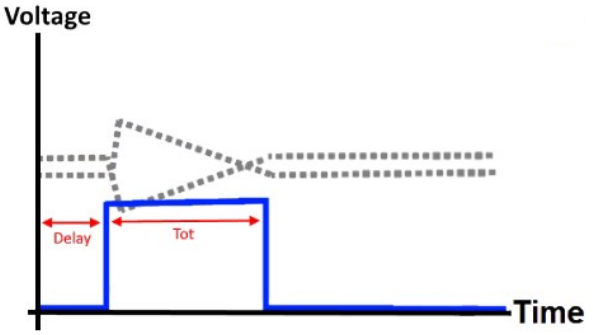
The RD53 differential frontend





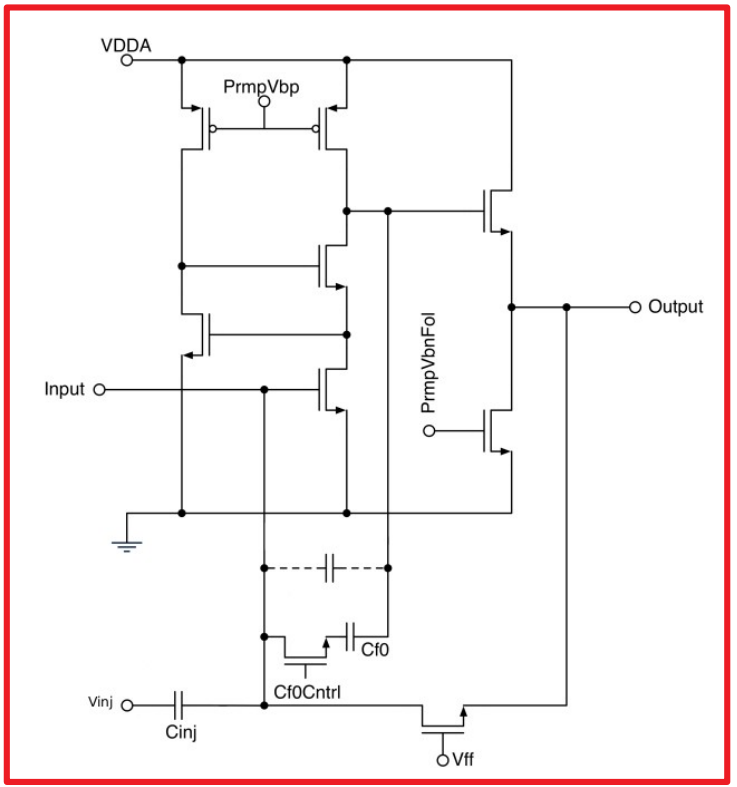
The RD53 differential frontend



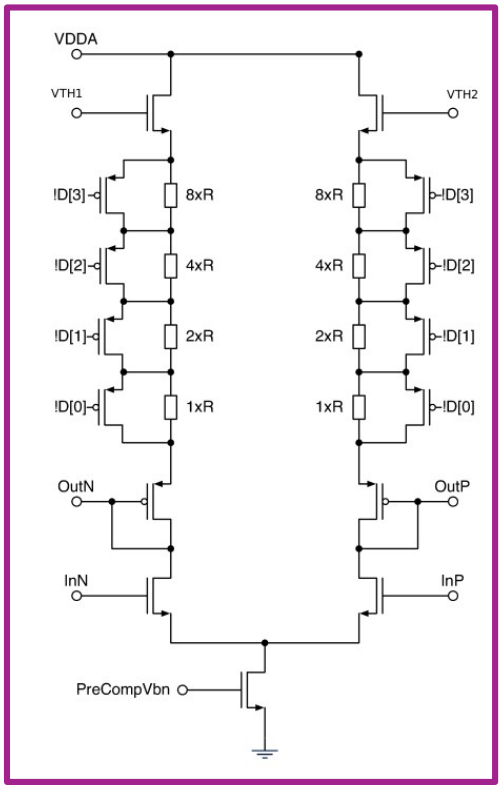


The RD53 differential frontend

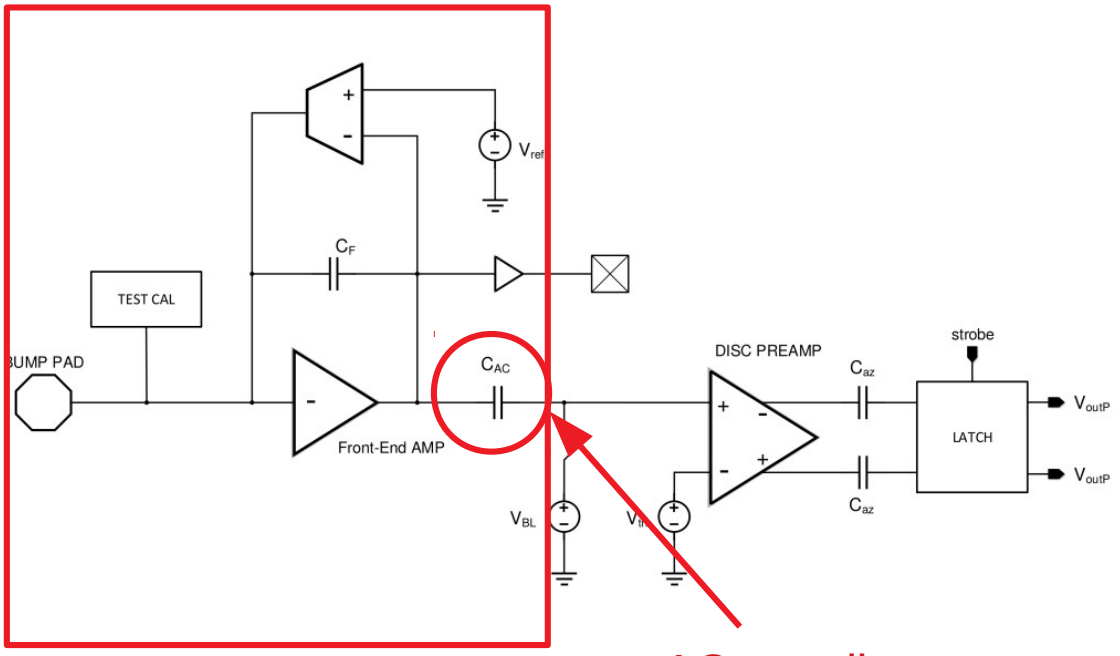
Preamplifier



Pre-comparator



The RD53 synchronous frontend

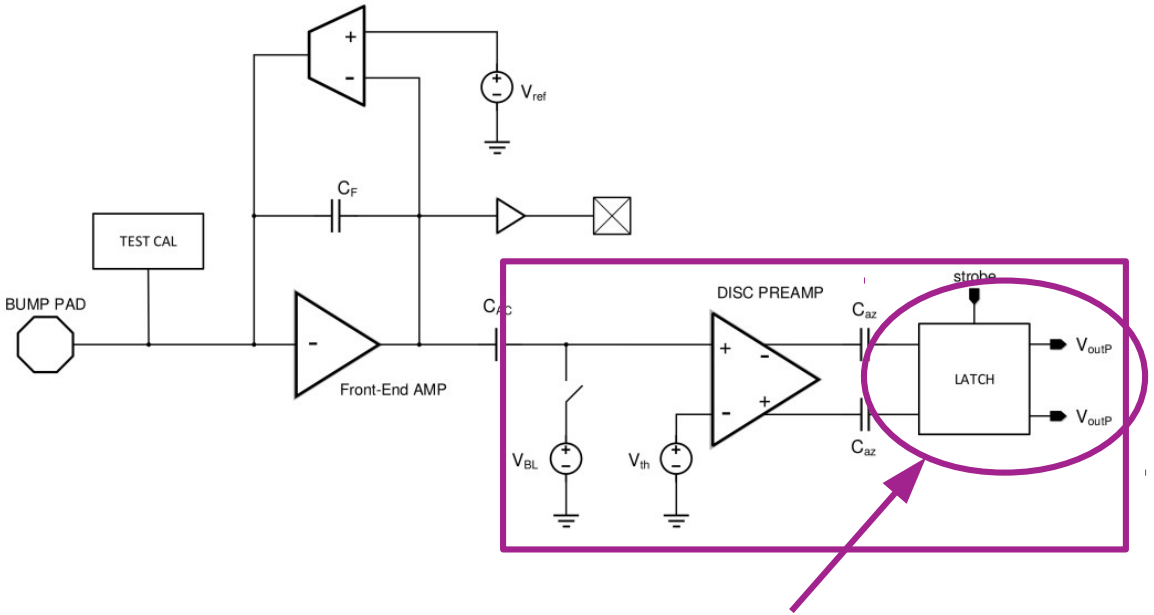


Single stage with Krummenacher feedback

CSA:

- I_k = 10nA → ToT=400ns @ 10ke-
- 2 possible gains (2.5 fF and 4 fF)

The RD53 synchronous frontend



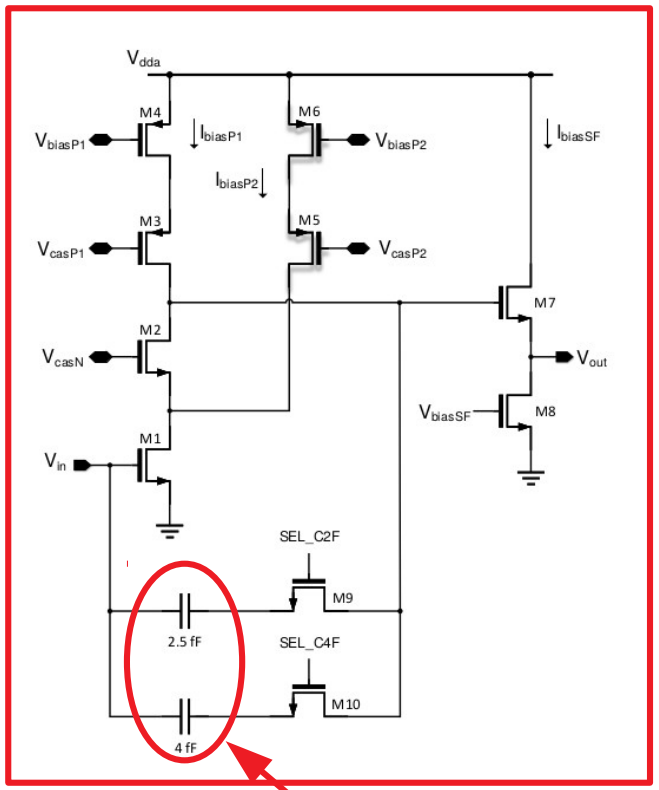
Auto-zeroing

Discriminator

- AC coupling removes the fluctuations from process mismatch
- Provides an additional gain (around x2)
- No adjustment bits → residual offset at output
- This is compensated by a latch circuit for auto-zeroing:
  - During LHC abort gaps, acquire 100ns baseline every 100us
  - Store the baseline value
  - Subtract baseline from signal
  - ISSUE: this induces noise on the power lines
- The latch can also be operated as ToT logic (working as a 800 MHz local oscillator)

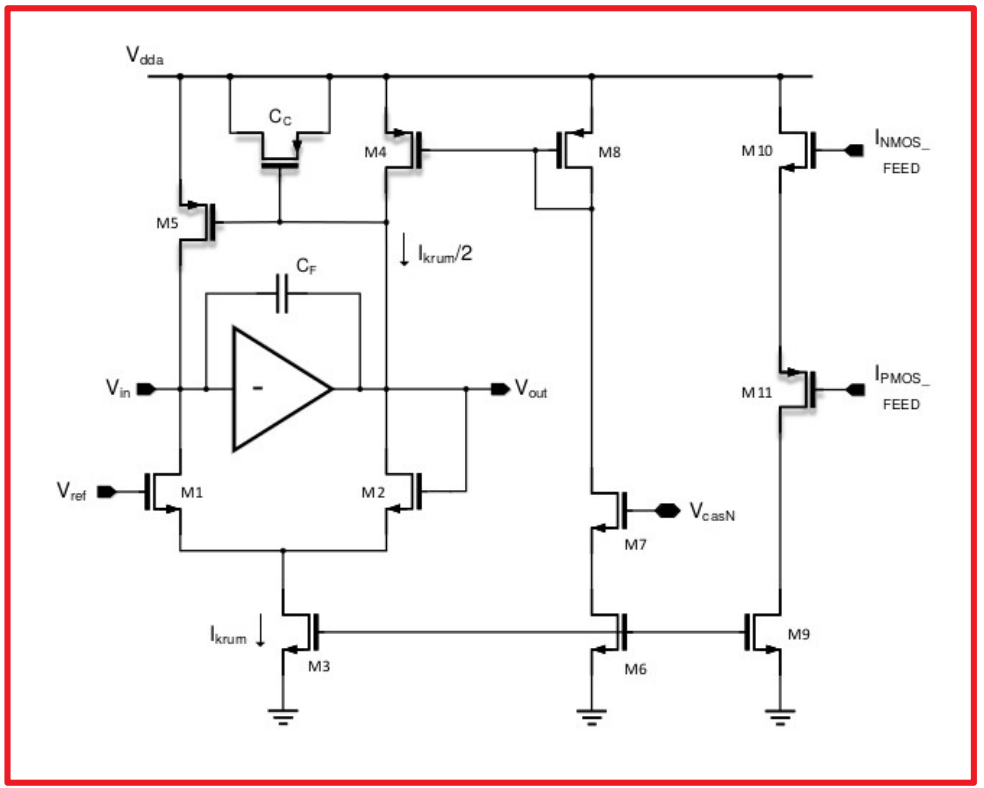
The RD53 synchronous frontend

Preamplifier



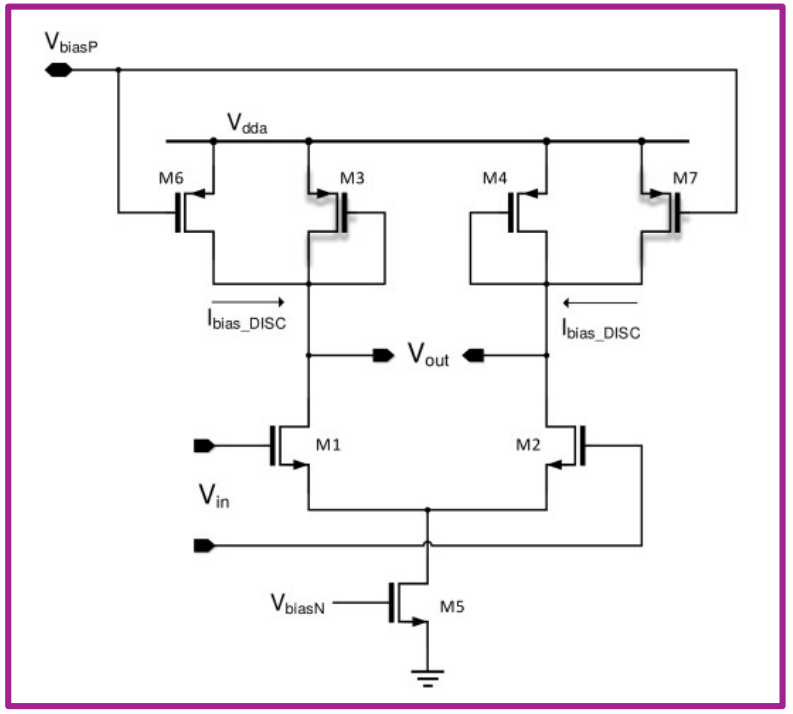
Two gains

Krummenacher loop

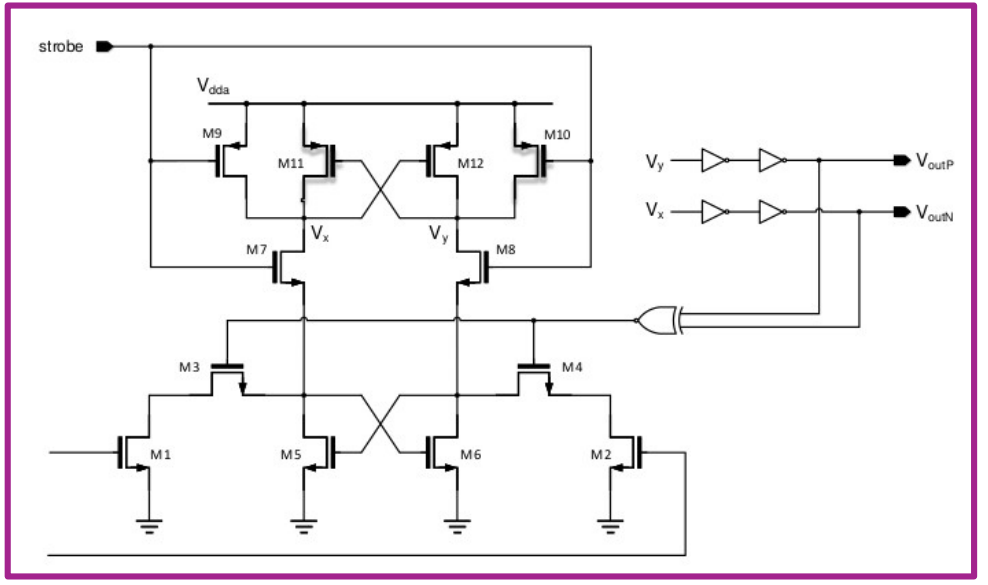


The RD53 synchronous frontend

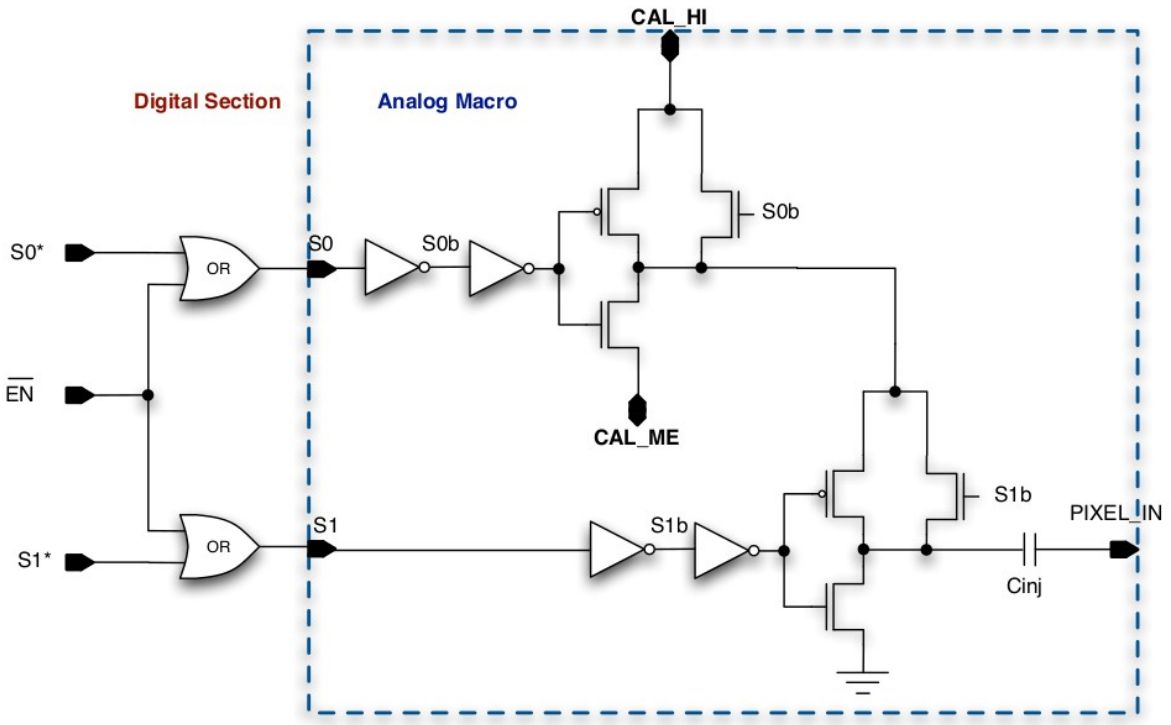
Discriminator



Latch (auto-zeroing circuit)



Calibration injection circuit

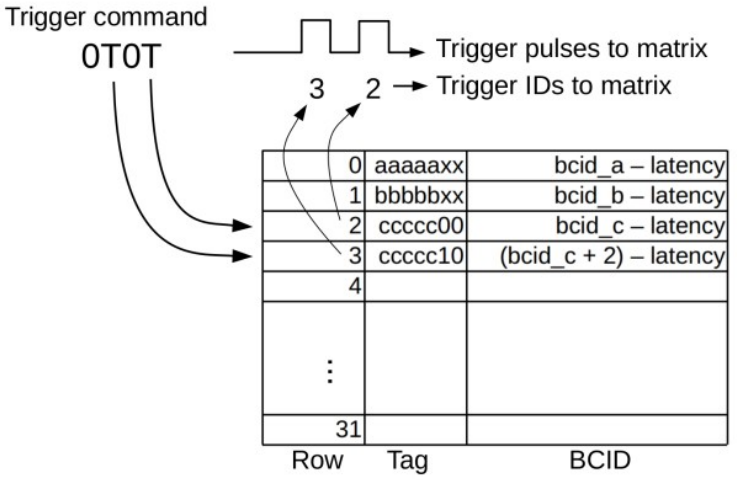


- Same for all frontend flavours
- Differential DC voltages, to reduce noise
- Linearity confirmed by measurements

Trigger

Triggering
- One trigger pulse allowed in each 40MHz BX_CLK cycle
- Two possibilities:
  - User-generated via the command decoder in the periphery
  - External
  - No internal self-trigger

Book keeping
- Trigger pulse
  → periphery: new entry in the TT
  → matrix: store hits within (programmed) latency
- Pixels also receive TT row number (trigger ID)
- The TT entry has: trigger ID, tag (5 bits set by user + 2 bits from BC counter*), BCID (internal counter)
- The user can reset the BCID
- Readout is data driven (FIFO): empty the TT as fast as possible



The trigger table (TT) is 32-words deep (5 bits row number)

** the trigger signal covers 4 BC*

Bonus slide: a gem from the web

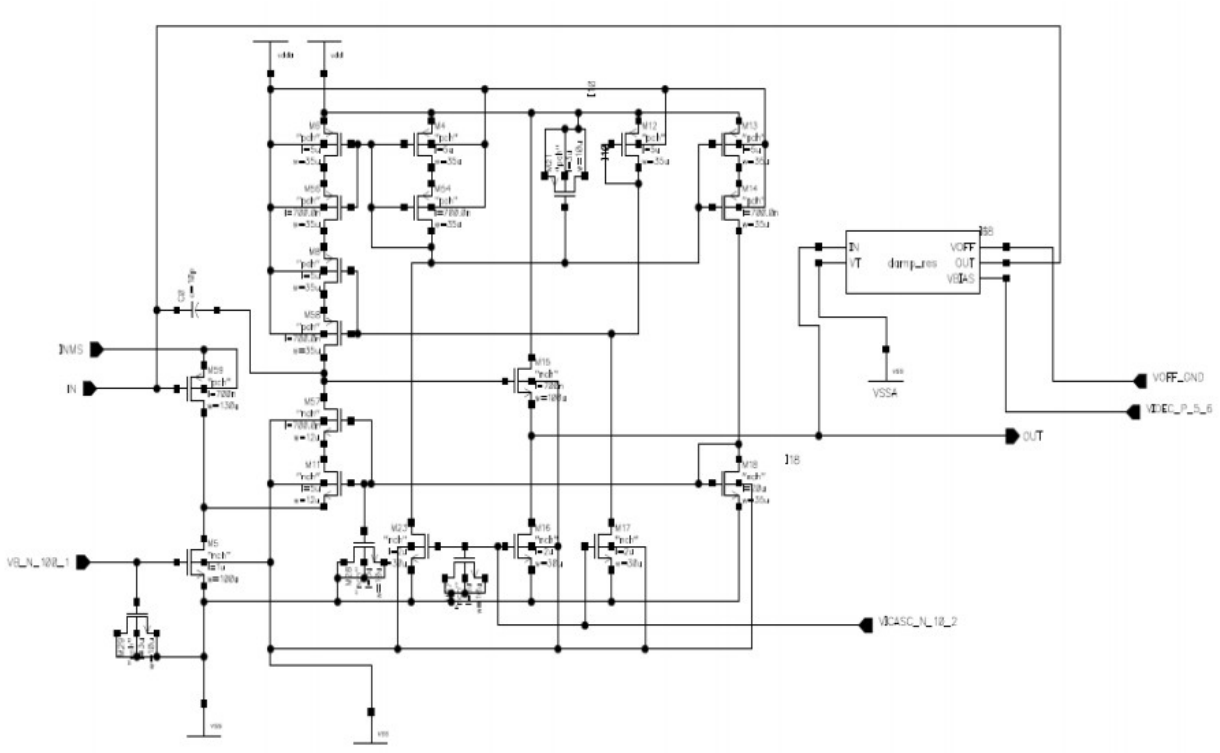


Figure 1.3: Schematic of preamplifire