



## Strip detectors: ROC, DAQ & dE/dx:

### Updates on Trieste activities

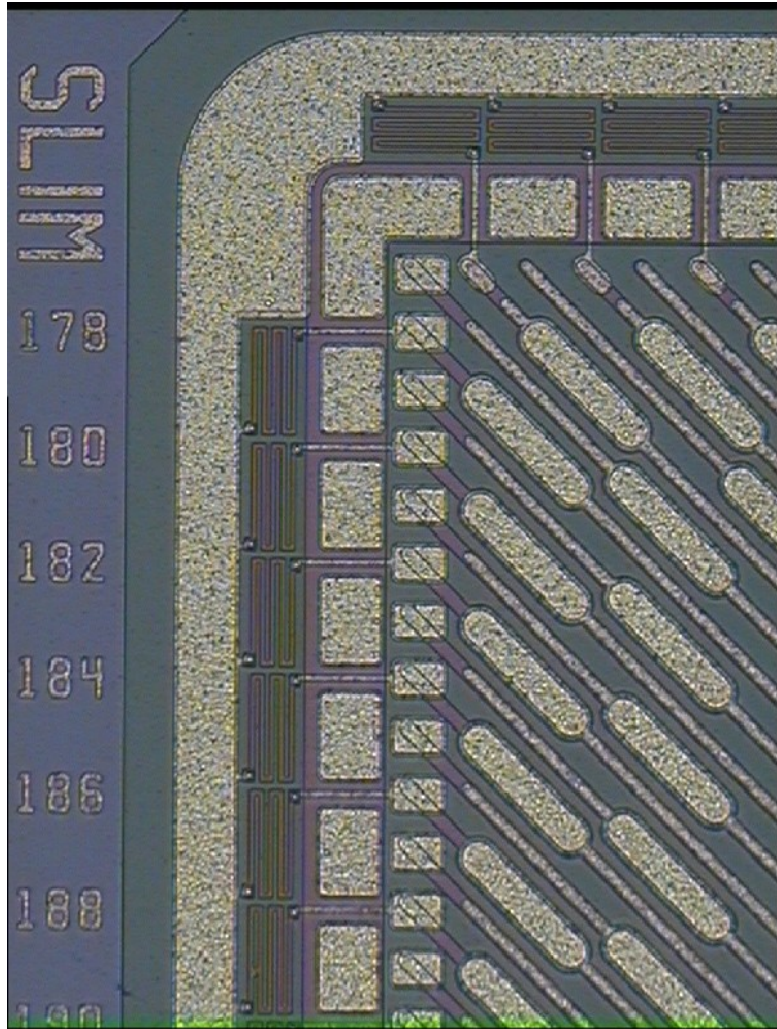
**Marco Bomben**

(on behalf of Luciano Bosisio, Pietro Cristaudo, Livio Lanceri, Irina Rashevskaya, Carlo Stella, Lorenzo Vitale)

Università degli Studi di Trieste & INFN – Trieste

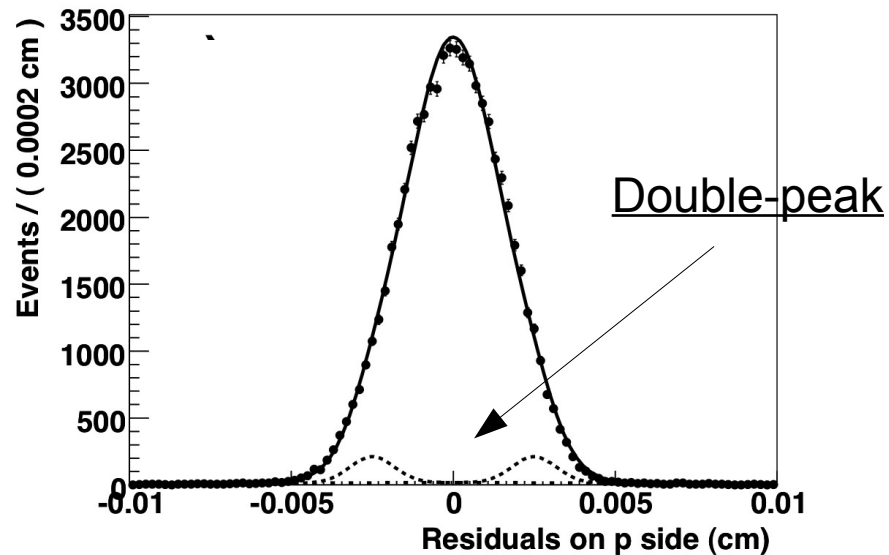
- What are we working on
  - Triplets & Strip detectors
  - FSSR2 chip
  - DAQ
  - $dE/dx$  in SVT ← **NEW**
- Noise measurements
  - temperature scan
  - Integrator, shaper & BLR parameters
- Update on new DAQ chain
- $dE/dx$  studies
- Plans & conclusions

## Sensor for L0 & inner layers



- 200  $\mu\text{m}$ -thick double-sided strip detector
  - $\pm 45^\circ$  oriented strips
- the design allows a long double-sided detector with short strips on both sides
- Active area = 27 x 12.9 mm<sup>2</sup>
  - $\sim 2.7$  cm read per side
- 50  $\mu\text{m}$  pitch on p-side
- 50  $\mu\text{m}$  pitch on n-side
- Strip capacitance  $\sim 4$  pF

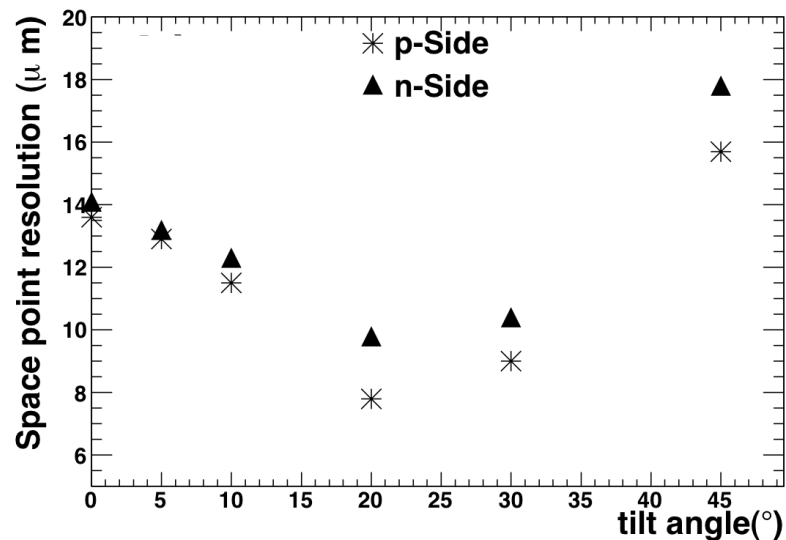
## Spatial resolution



- p-Side: Space Point resolution:  $13.6 \mu\text{m}$
- n-Side: Space Point resolution:  $14.1 \mu\text{m}$
- Pitch =  $50 \mu\text{m}$  on both sides

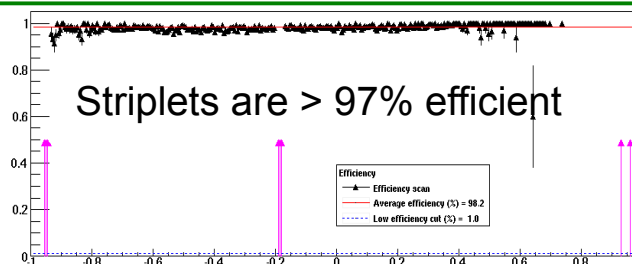


## Spatial resolution Vs tilt angle

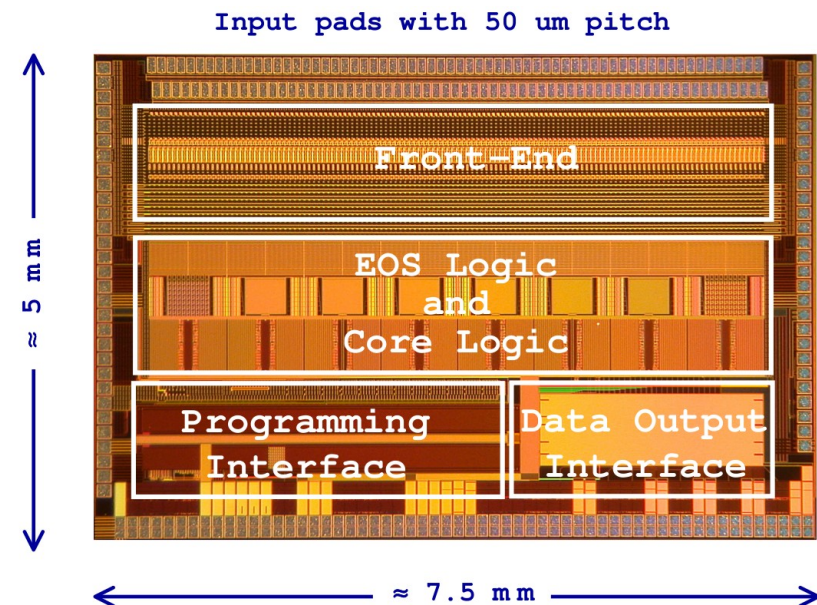


- Double-peak effect in resolution plot
- It helped in improving resolution of almost 10%

## Efficiency along the detector



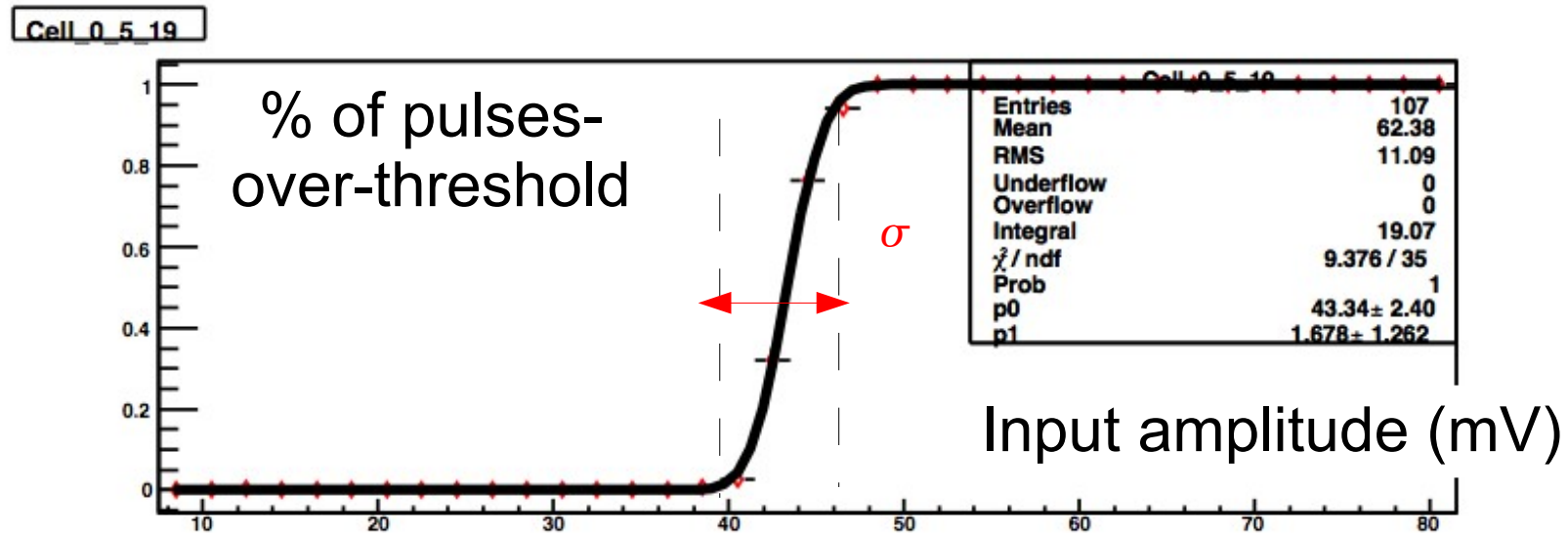
- Fermilab Silicon Strip Readout chip v2
  - The chip has been developed by an INFN Pavia & Bergamo and Fermilab for the BTeV strip detectors
- 128 analog channels, with address and time information for all hits
- Self-triggered readout architecture, with digital output only
- Read out up to 70 MHz
  - Operated at 20 MHz @ testbeam



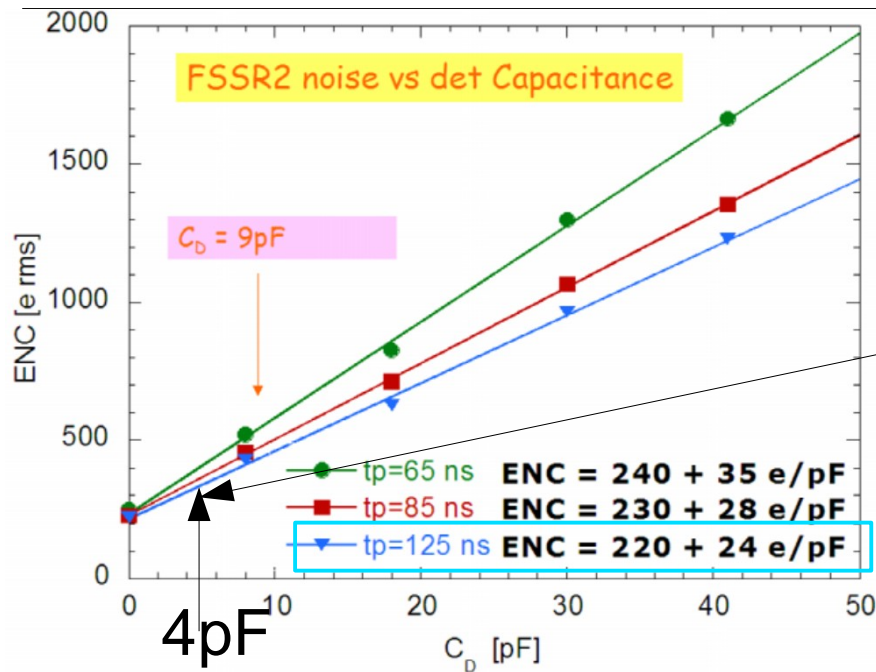


- 8 programmable thresholds, with the 0<sup>th</sup> one acting as hit/no hit discriminator
  - Each channel has its own set of 8 comparators
- 3-bit ADC information is provided for each hit
- Programmable gain and peaking time
- Baseline restorer available
- Optimized for positive signals
  - Limited dynamic range for n-side: just hit/no hit information for negative signals
- **News** from Valerio Re about FSSR2 (talk earlier today)

- Noise was estimated using FSSR2 internal-calibrator, during beam test
- At fixed threshold, input amplitude was increased, and fraction of pulses-over-threshold recorded
- The result is fitted with an erf function, where  $\sigma$  is the estimated noise



Detector	Striplets		Telescope	
	p side	n side	p side	n side
Noise ( $e^-$ RMS)	560	978	400	742
S/N	29	16	60	32
Gain (mV/fC)	96	67	97	67



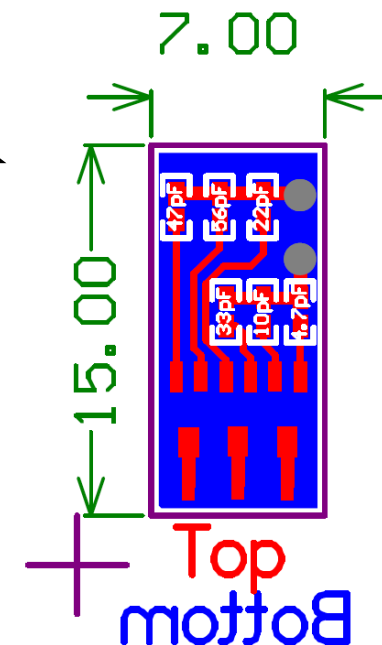
About 316 enc\*

At test-beam we were very close to benchmark for telescope detector on p-Side

\* = expected for p-Side of telescope



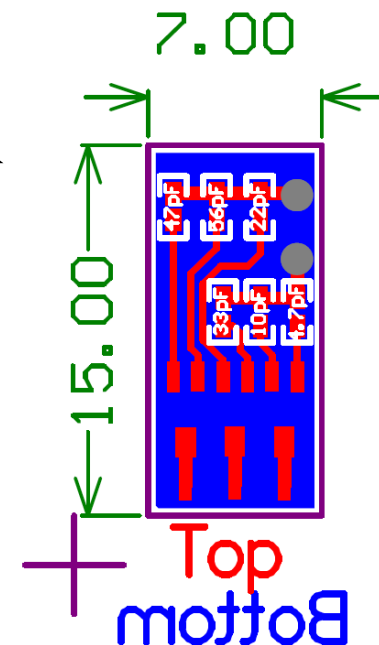
- More temperature points
- Change shaper parameters
- Measure triplets-module capacitance
  - Sensor + fanout + ecc
- Bond FSSR2 channels to capacitors to measure noise as a function of capacitance
- A new DAQ... (see next slide)

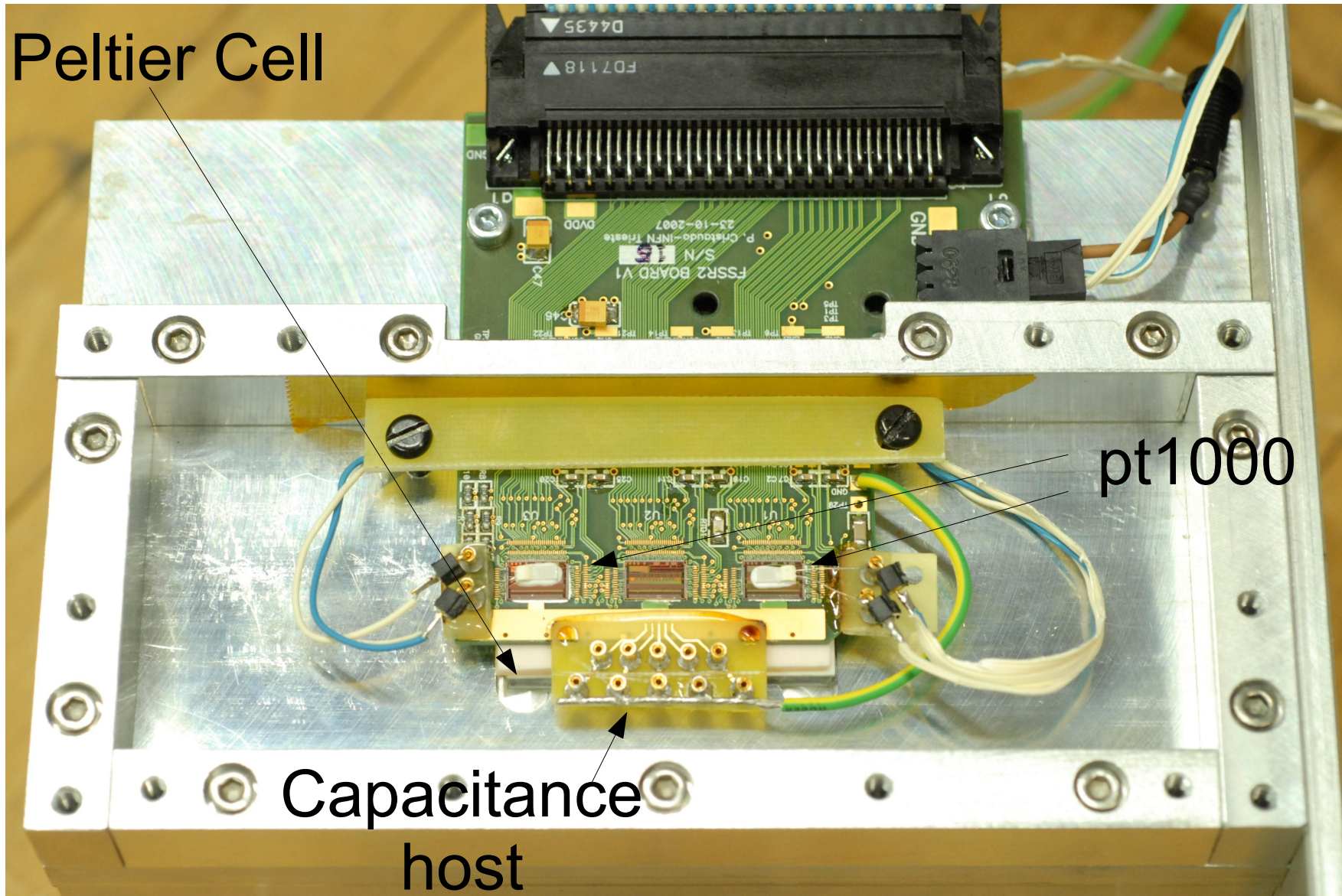


# To Do List

- More temperature points
- Change shaper parameters
- Measure triplets-measured capacitance
  - Sensor + fanout + ecc
- Bond FSSR2 channels to capacitors to measure noise as a function of capacitance
- A new DAQ... (see next slide)

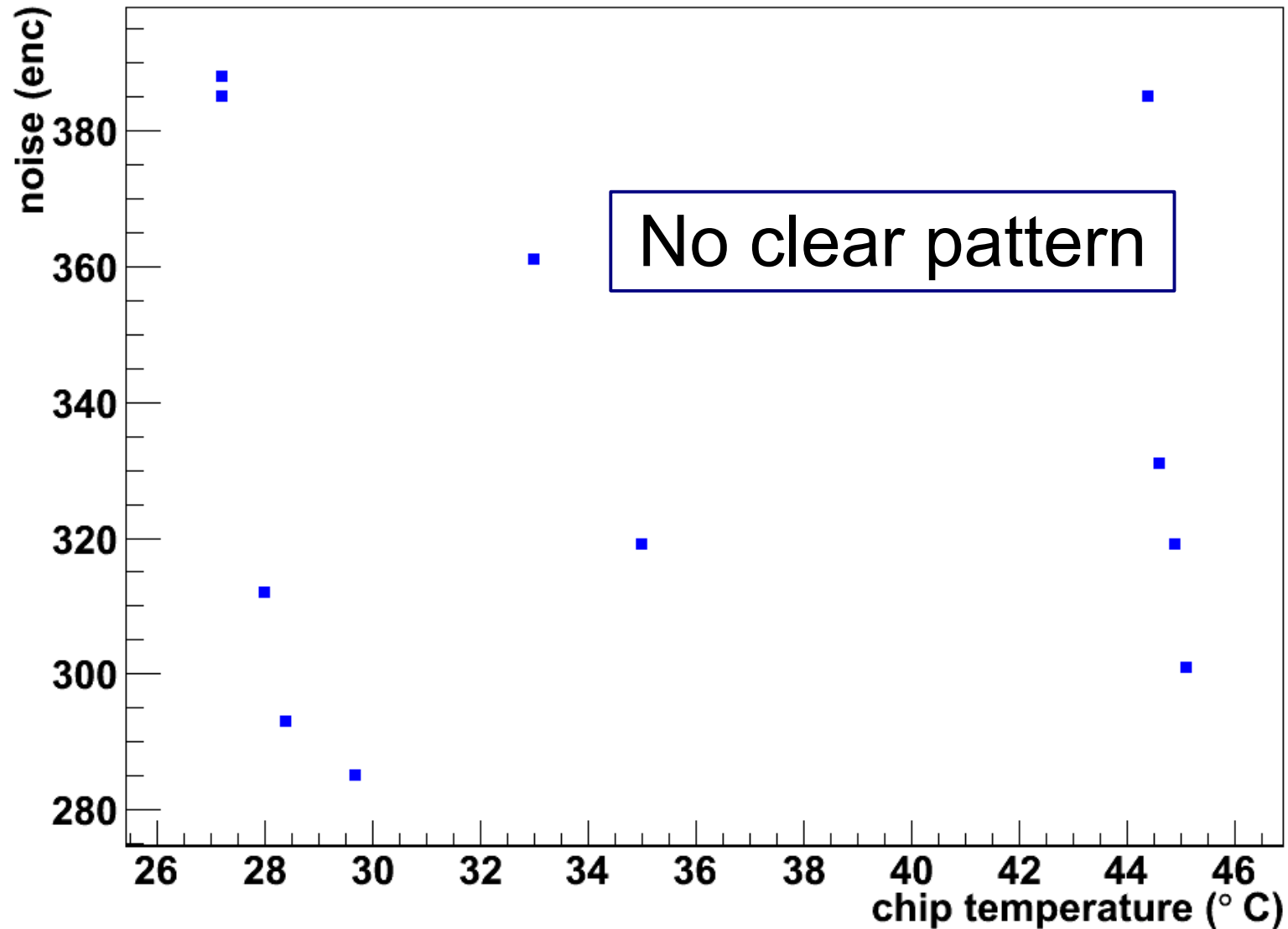
As seen in Annex





# Noise Vs Temperature

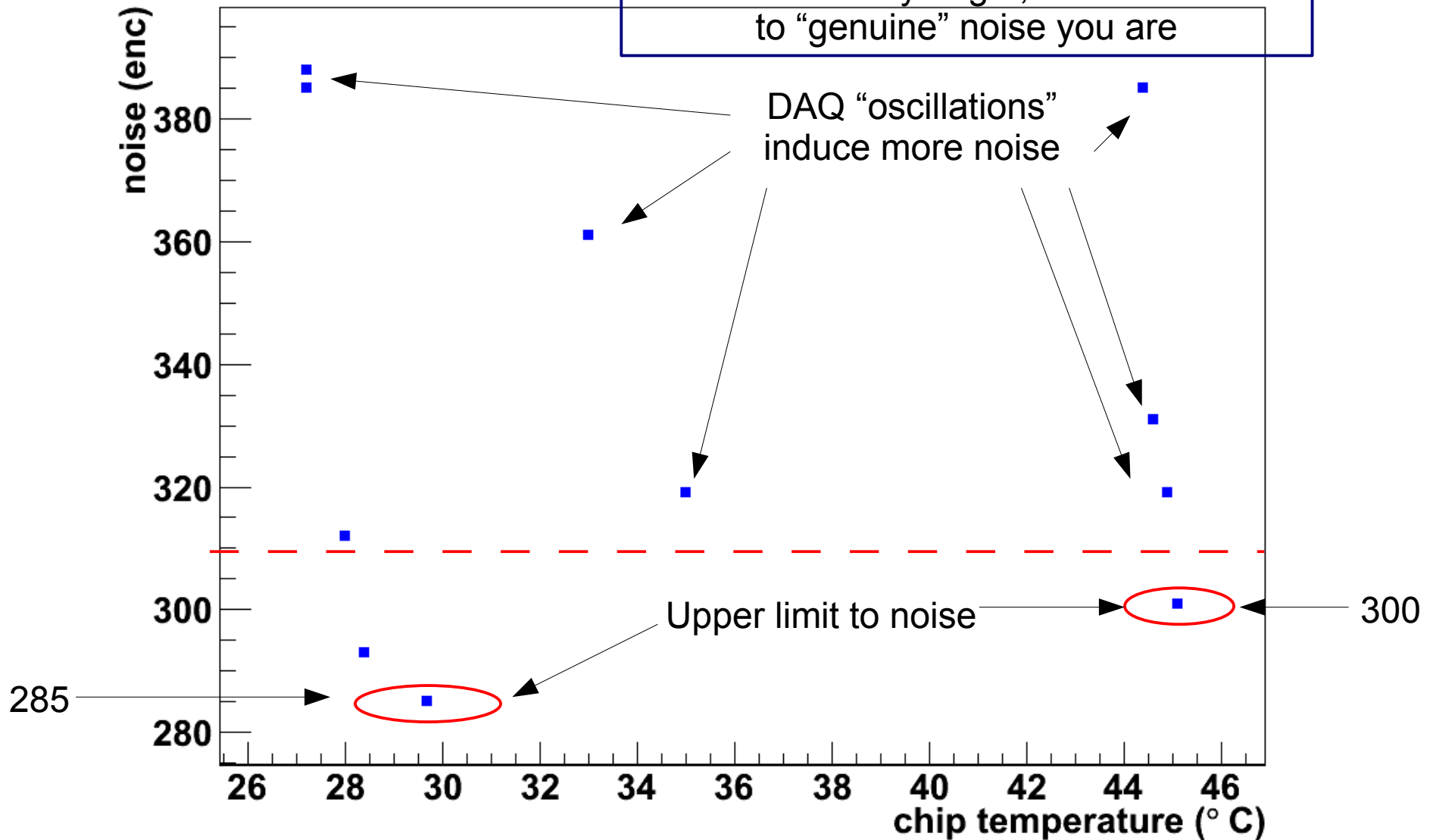
noise vs temperature



# Heuristic caveat

noise vs temperature

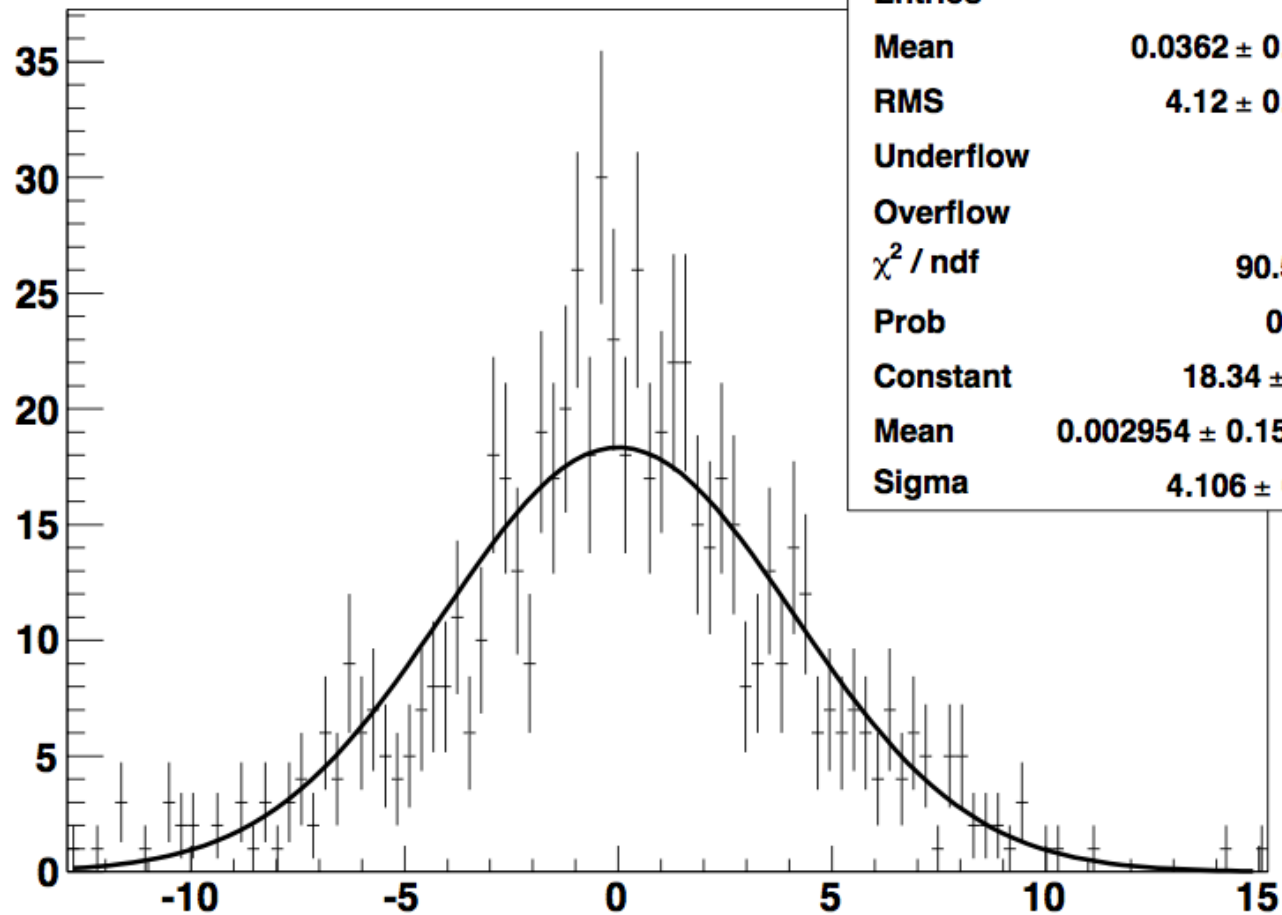
For a given configuration, the smaller noise estimate you get, the more close to "genuine" noise you are





# Threshold dispersion

Threshold dispersion = 981 enc



allDisp	
Entries	673
Mean	$0.0362 \pm 0.1589$
RMS	$4.12 \pm 0.1124$
Underflow	1
Overflow	0
$\chi^2 / \text{ndf}$	90.5 / 96
Prob	0.6391
Constant	$18.34 \pm 0.87$
Mean	$0.002954 \pm 0.159422$
Sigma	$4.106 \pm 0.116$

We strongly suspect its a POMONE related feature



# The BTeV DAQ chain



- We used Pomone to test FSSR2 chips and all strip detectors
- We received the whole chain with practically no written instructions
  - But we received “online” support
- One piece only
- We put it back to work
  - Tough reverse-engineering
- Not always reproducible behaviour
- We observe non-negligible variations in noise measurements
- Roughly half of the calibrations got aborted...

# Noise Vs shaper, integrator, BLR parms

- We would like to study the noise performance as a function of the shaper, integrator and BLR parameters
  - 4 8-bit registers
  - Each controls a current in a section of the logic of FSSR2
- We started varying default values
- But...
- ... but due to old DAQ, quantitative results couldn't be reached
- Massimo Manghisoni is looking into FSSR2 projects to understand better what each DAC does in detail
- We (re)discovered functionality ranges for each register

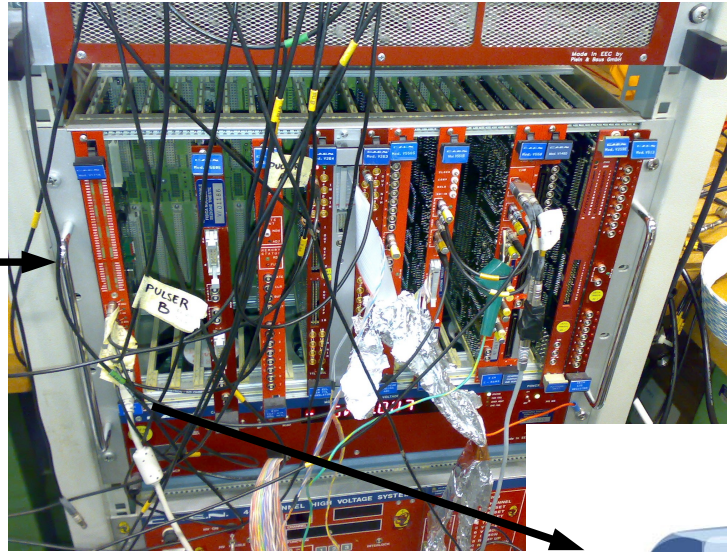
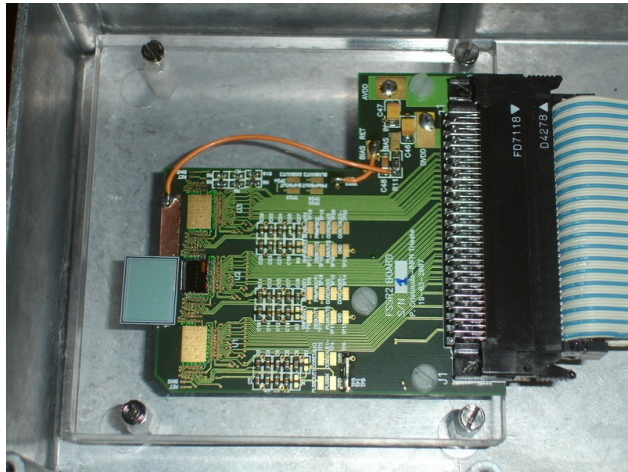


# New DAQ



- We are developing a new DAQ, which is based on a CAEN board which has FPGAs
- We will program chips and read data through a VME-USB bridge and a Labview-based acquisition program
- Status: FPGA is programmed (many thanks to Mauro Villa)
- First tests ← **NEW**
  - See next slides...

# New DAQ scheme



run\_control.vi

File Edit View Project Operate Tools Window Help

Run Number File  
C:\Documents and

log files directory  
C:\Documents and Settings\Administrator\Desktop\Marco\statemachines\log\

config file directory  
C:\Documents and Settings\Administrator\Desktop\Marco\statemachines\config\

data files directory  
C:\Documents and Settings\Administrator\Desktop\Marco\statemachines\data\

STOP

RUN

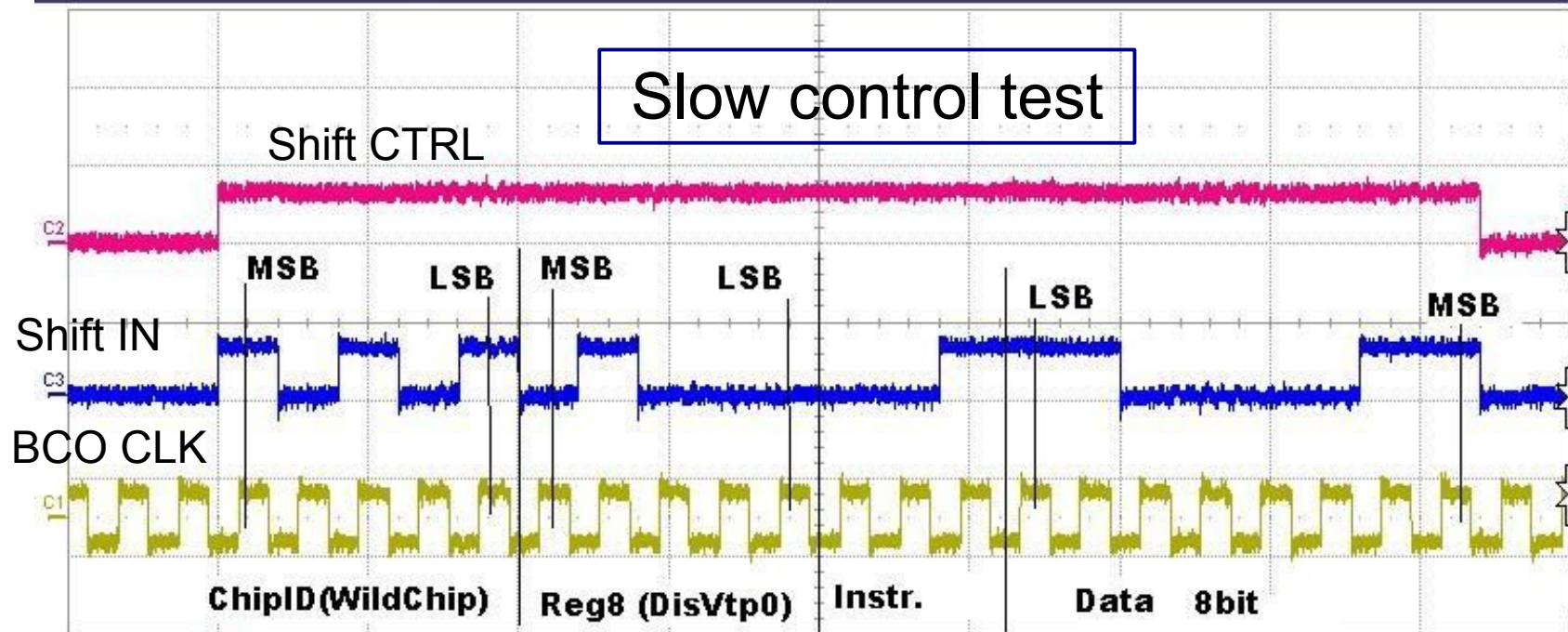
log file status		error for data file		error for config file	
status	code	status	code	status	code
✓	0	✓	0	✓	0
source		source		source	

```
Marco/fssr2_ro/rl/v1495usr_EPMC - v1495usr_EPMC - [c:/src/v1495/v1495usr_EpmCore.vhdl]
Help
./src/v1495/v1495usr_EpmCore.vhdl

2  ---
3  --- Company: CAEN SpA - Viareggio - Italy
4  --- Model: V1495 - Multipurpose Programmable Trigger
5  --- FPGA Part. Name: V1495USR_EPMC
6  --- Device: ALTEPA EP1C4F400C6
7  --- Author: MB - PC - LV
8  --- Date: 01-03-2010
9  ---
10 --- Module: from CAEN V1495 COIN_REFERENCE
11 --- Description: Reference design to use the V1495 board
12 --- as interface to Mauro Villa Epmc Mainin
13 --- We used two layer (L0, L1) of the board
14 --- the EPMC.
15 --- This document is realized from CAEN/COIN/
16 ---
17 ---
18 --- *****
19 --- Revision History:
20 ---
21 --- Date Author Revision Comment
22 --- 02 Mar 06 LC 1.0 Creation
23 --- *****
24 ---
25 LIBRARY ieee;
26 USE ieee.std_logic_1164.all;
27 USE ieee.std_logic_arith.all;
28 USE ieee.std_logic_unsigned.all;
29 USE ieee.std_logic_misc.all; -- Use OR_REDUCE function
30
31 USE work.v1495pkg.all;
32 USE work.EpmcPackage.all;
33 USE work.MyPackage.all;
34
35 ENTITY v1495usr_EpmCore IS
36 PORT(
37 nLBRES : IN std_logic; -- Async Reset (active low)
38 LCLK : IN std_logic; -- Local Bus Clock
39
40 --- REGISTER INTERFACE
```



File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help



Measure P1:freq(C1) P2:--- P3:--- P4:--- P5:--- P6:---

value 1.25001 MHz  
 mean 5.1738076 MHz  
 min 240.07 kHz  
 max 501.41248 MHz  
 sdev 26.4116727 MHz  
 num 952  
 status

Dis. Vtp0

C1	C2	C3
ACIM	ACIM	ACIM
500 mV/div	500 mV/div	500 mV/div
-1.250 V ofst	500 mV offset	-470 mV ofst
↓ 149 mV	↓ 19 mV	↓ -6 mV
↑ 149 mV	↑ 19 mV	↑ -6 mV
Δy 0 mV	Δy 0 mV	Δy 0 mV

Timebase	-8.00 μs	Trigger	C2/AC
	2.00 μs/div	Normal	255 mV
20.0 kS	1.0 GS/s	Edge	Positive

X1= 17.999 μs ΔX= 0 ns  
 X2= 17.999 μs 1/ΔX= ---

Waiting for Trigger

LeCroy



# New studies with new DAQ



- Thanks to new DAQ, we plan to study the hit-efficiency as a function of channel occupancy
  - Test will be (slightly) limited by RAM size
- The idea is to use few events but very close in time
- We will use the IR laser to “light” several strips and study the efficiency as a function of FSSR Clock and Readout Clock

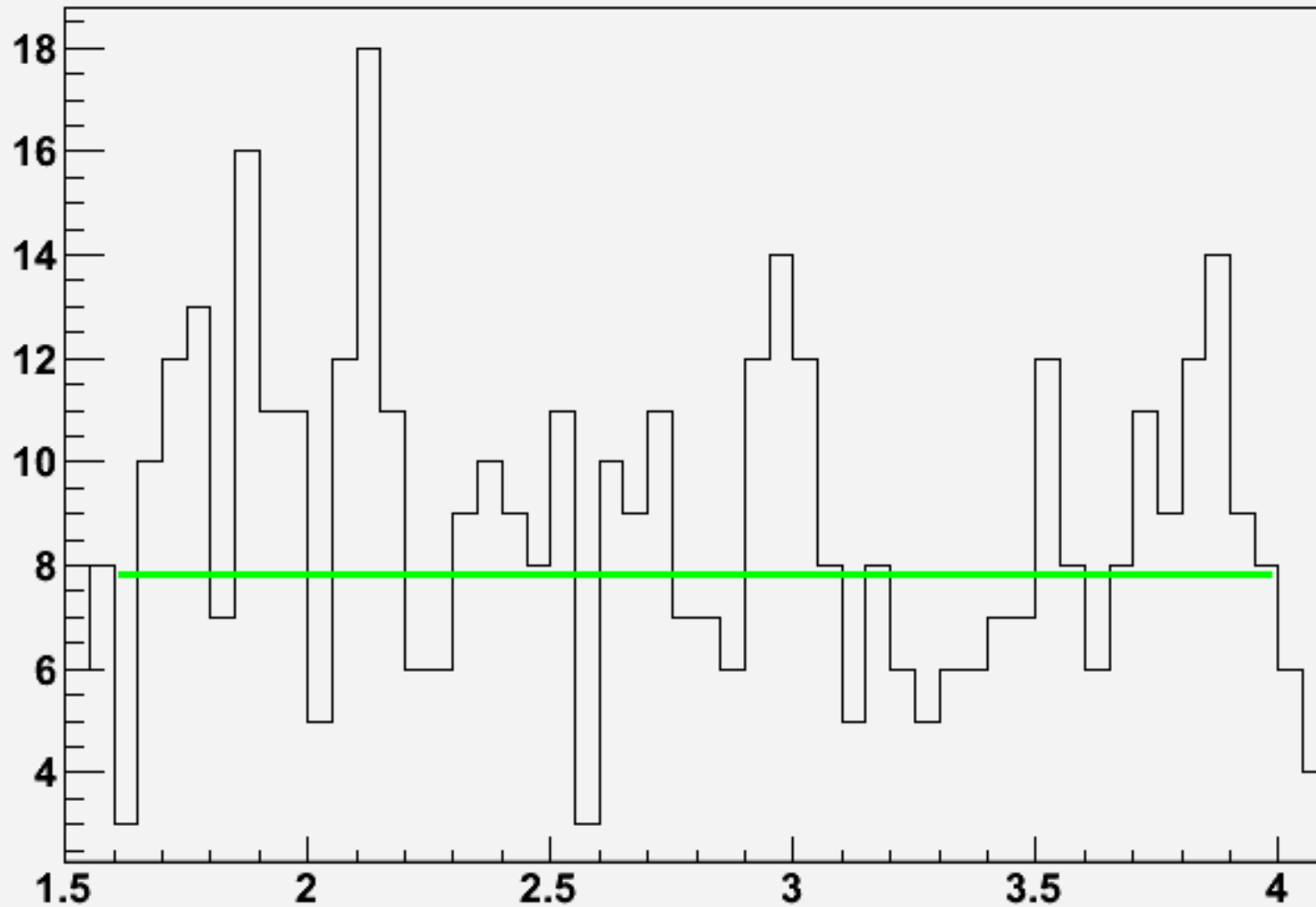
# dE/dx in SVT

- Increasing interest in dE/dx capabilities in SVT
  - “Pairs” could possibly be rejected on a dE/dx basis
- FSSR2 provides a 3-bit ADC information for each hit
- How to set the 8 thresholds?
  - 0<sup>th</sup> threshold acts as hit/no-hit discriminator
  - 7<sup>th</sup> threshold contains limited information
  - Range Vs Granularity



- We started looking at full simulated events
  - Pairs
  - Single particle (e.g.  $\pi$ , for a given energy range)
- We will “digitize” the released energy in SVT layers by using a scheme a la FSSR2
- We will try to understand several things
  - How thresholds need to be set
  - What is the optimal number of adc bits
    - 3? More than 3?

Fit delle energie dei  $\pi$





- There is a lot of activity about triplets and the FSSR2 RO-chip in Trieste
- Oscillation of old DAQ prevented us to unambiguously measure electronic noise
- We will use new DAQ for studying noise versus
  - Temperature
  - Load capacitance
  - Shaper parameters
- We will study also hit-efficiency Vs occupancy
- dE/dx study started
  - using simulated data



# That's it



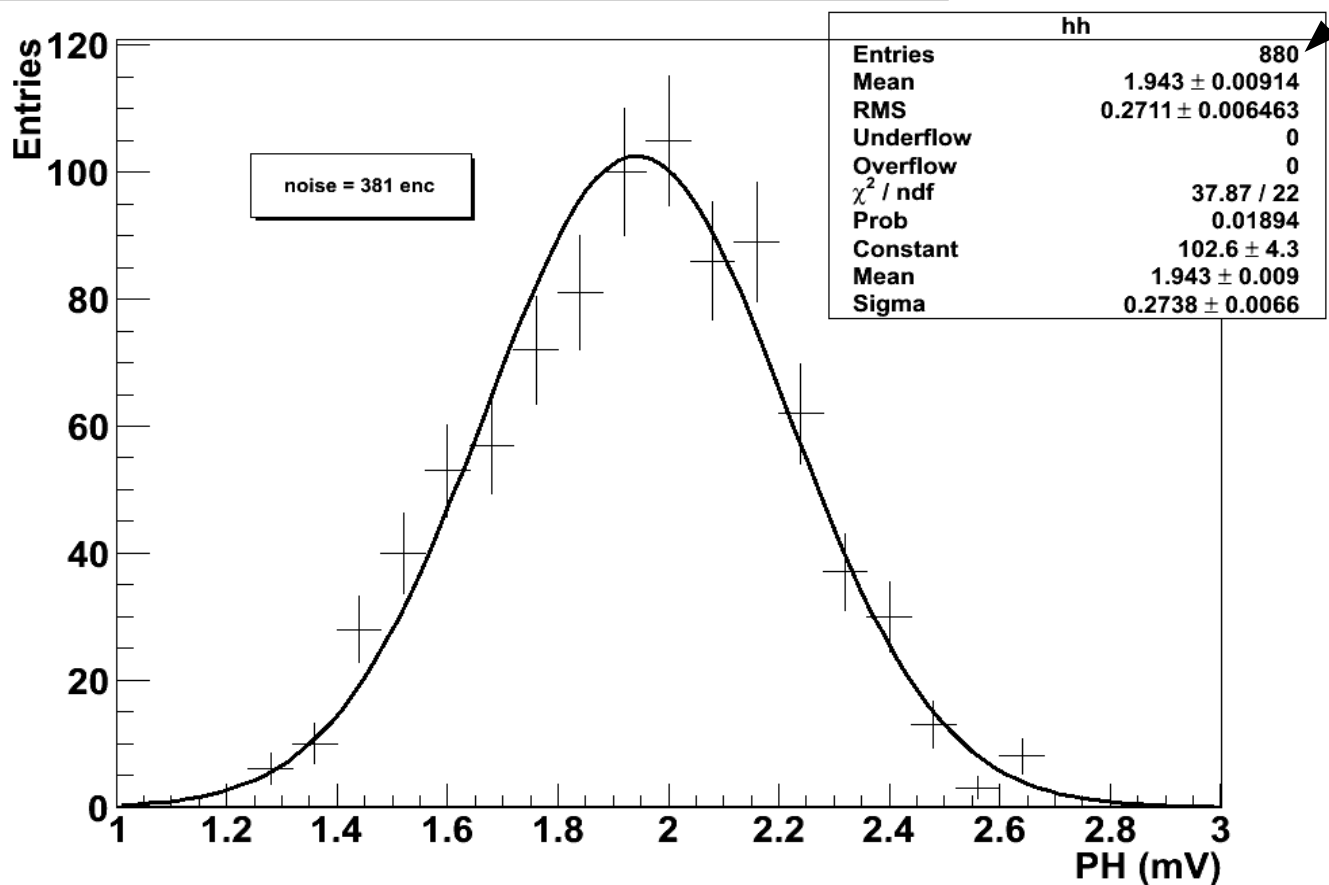


# Backup slides



- Calibration performed with FSSR2 internal pulser and old BTeV test-beam DAQ chain
- 8 (thresholds ) x 128 (channels) injected
  - Not all fits do converge
  - Some extra-counts enter the fit

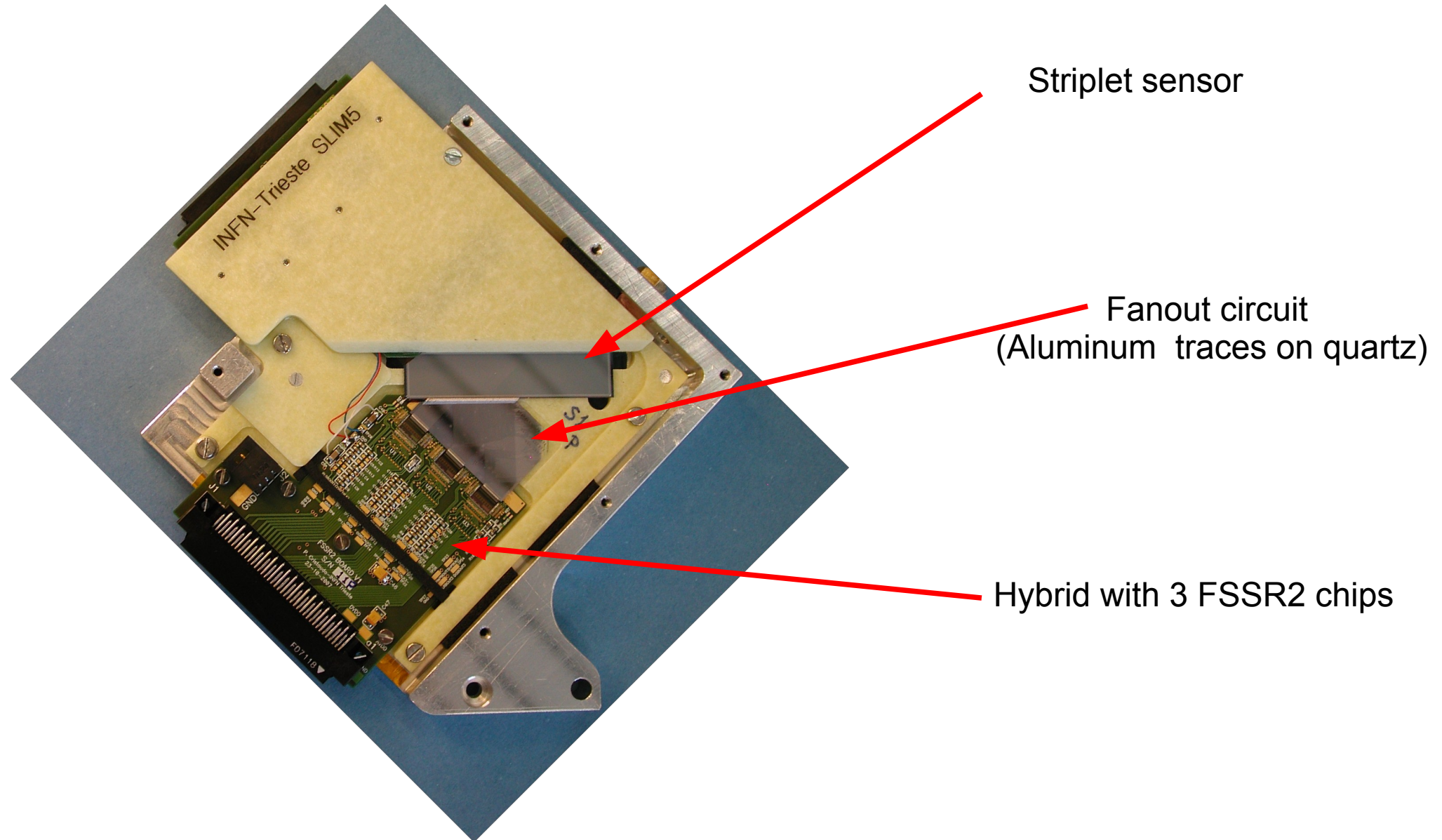
noise dispersion for M16, chip19, t=43.0C





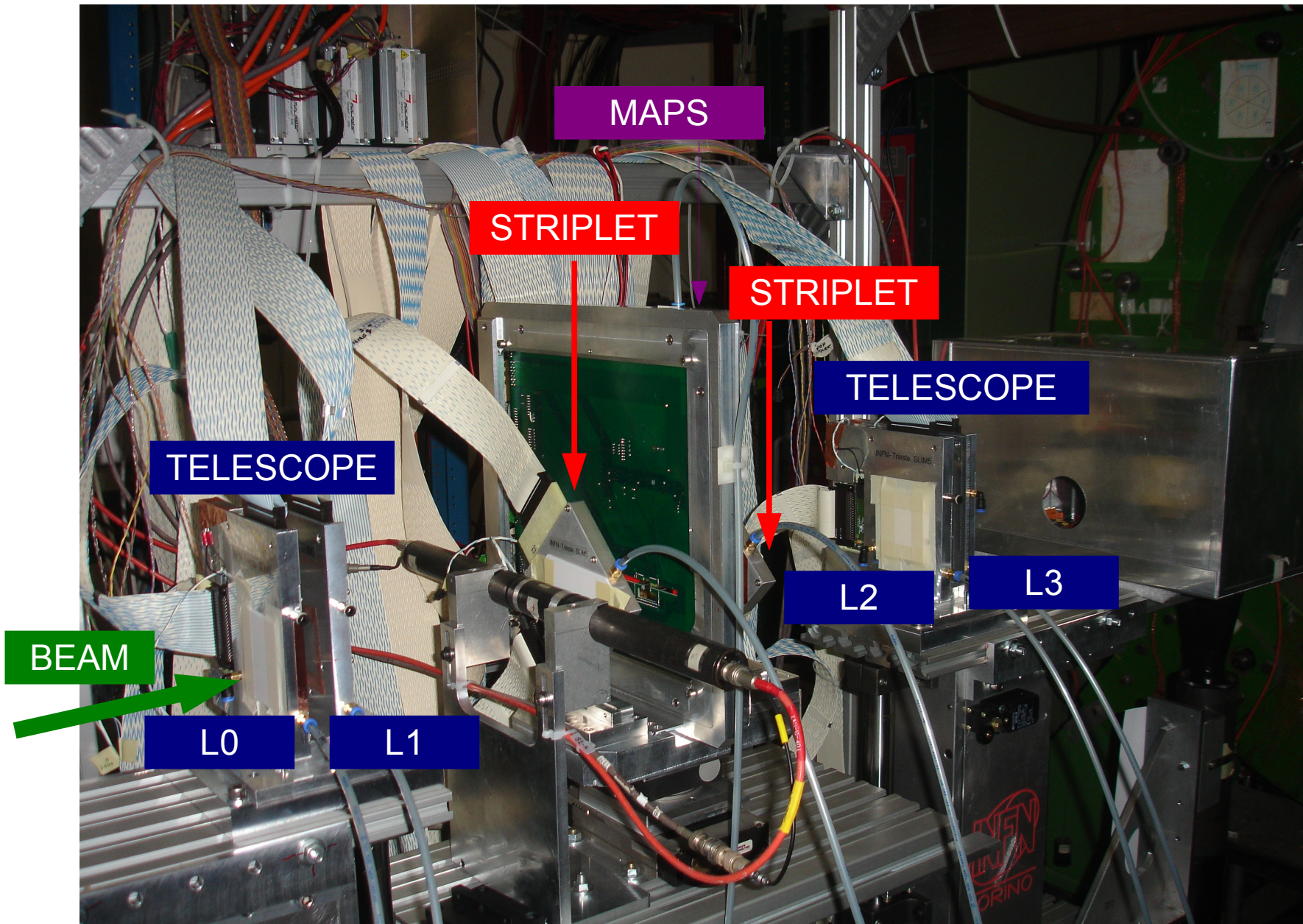
- R&D Italian collaboration
- Mission: “Pushing thin tracking-devices state-of-the-art for High Energy Physics”
- Highlights:
  - MAPS → not in this talk!
  - Triplets
  - Double sided telescope
  - Data-driven DAQ-architecture
  - Test beam in 2008 @ CERN – PS
- Paper ready for submission





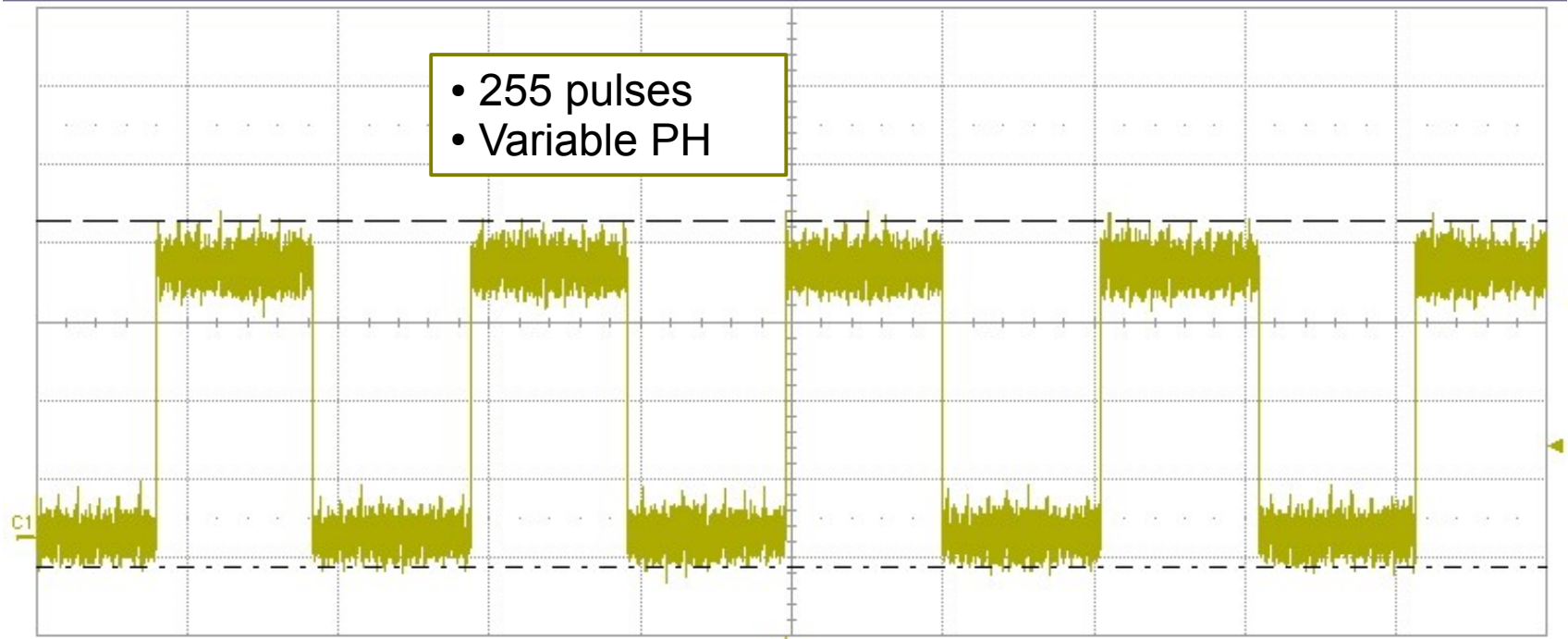


# Slim5 – Test beam setup





File Vertical Timebase Trigger Display Cursors Measure Math Analysis Utilities Help



Measure	P1:pkpk(C1)	P2:rms(C1)	P3:max(C1)	P4:---	P5:---	P6:---
value	94.4 mV	48.49 mV	83.1 mV			
mean	93.939 mV	47.6669 mV	83.712 mV			
min	91.9 mV	31.18 mV	82.5 mV			
max	97.5 mV	48.66 mV	86.3 mV			
sdev	1.245 mV	3.4910 mV	1.043 mV			
num	33	33	33			
status	✓	✓	✓			

C1 DCIM  
20.0 mV/div  
-55.00 mV  
---- -7.6 mV  
----- 80.6 mV  
Δy 88.2 mV

300 enc

Timebase -400 μs  
10.0 ms/div  
2.00 MS 20 MS/s

Trigger C1 DC  
Normal 23.2 mV  
Edge Positive

LeCroy

3/11/2010 10:33:31 AM

