Strip detectors: ROC, DAQ & dE/dx:

Updates on Trieste activities

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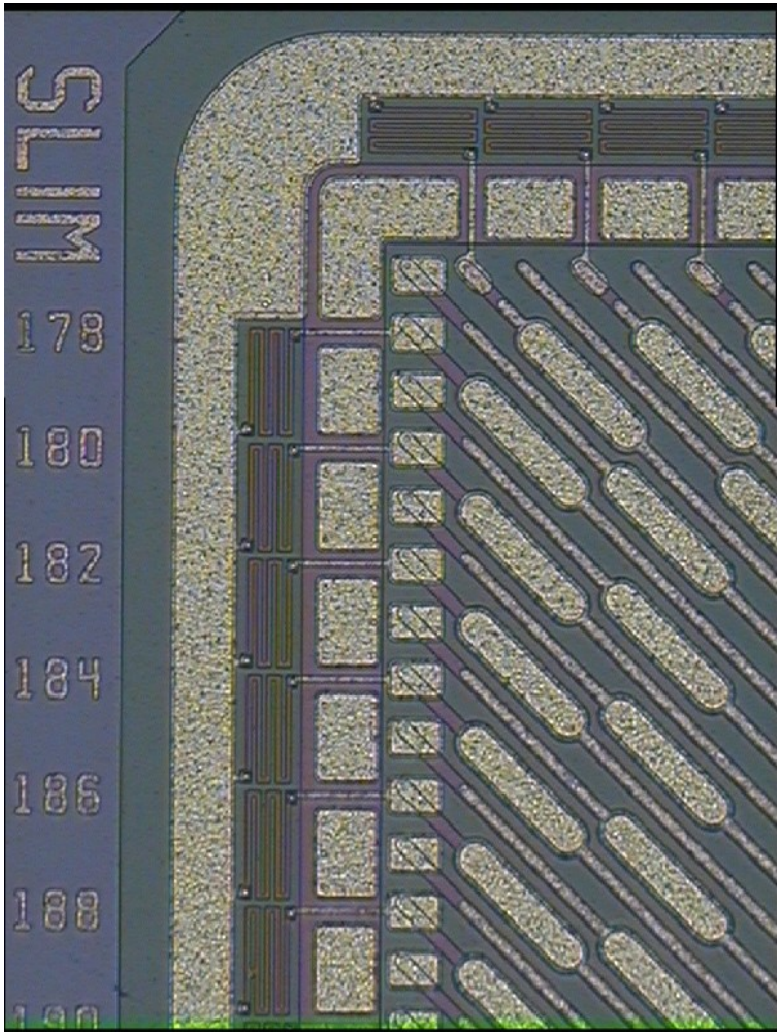
Outline

- What are we working on
  - Striplets & Strip detectors
  - FSSR2 chip
  - DAQ
  - dE/dx in SVT ← NEW
- Noise measurements
  - temperature scan
  - Integrator, shaper & BLR parameters
- Update on new DAQ chain
- dE/dx studies
- Plans & conclusions

Slim5 – Striplets sensors

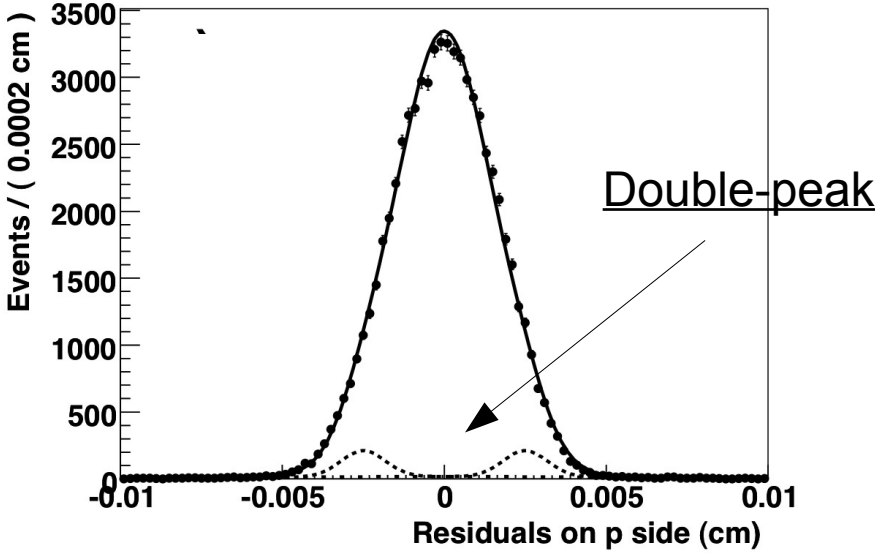
Sensor for L0 & inner layers



- 200 μm-thick double-sided strip detector
  - ± 45° oriented strips
- the design allows a long double-sided detector with short strips on both sides
- Active area = 27 x 12.9 mm^2
  - ~ 2.7 cm read per side
- 50 μm pitch on p-side
- 50 μm pitch on n-side
- Strip capacitance ~ 4 pF

Slim5 – Results from Test beam

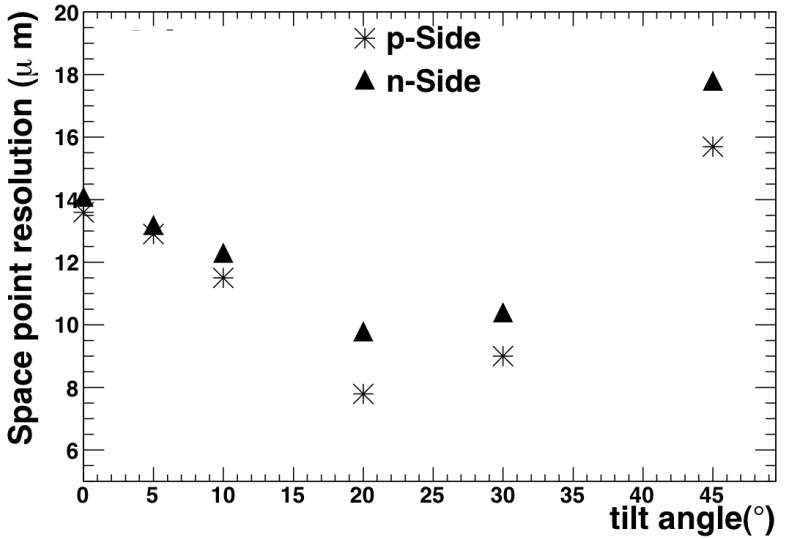
Spatial resolution



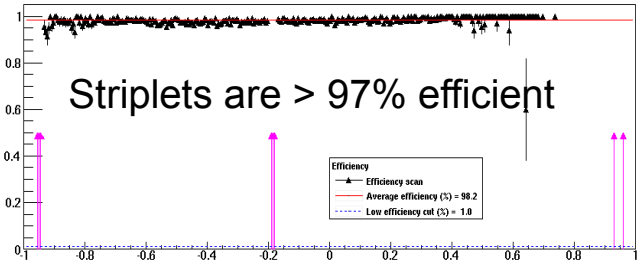
- Double-peak effect in resolution plot
- It helped in improving resolution of almost 10%

- p-Side: Space Point resolution: 13.6 μm
- n-Side: Space Point resolution: 14.1 μm
  - Pitch = 50 μm on both sides

Spatial resolution Vs tilt angle

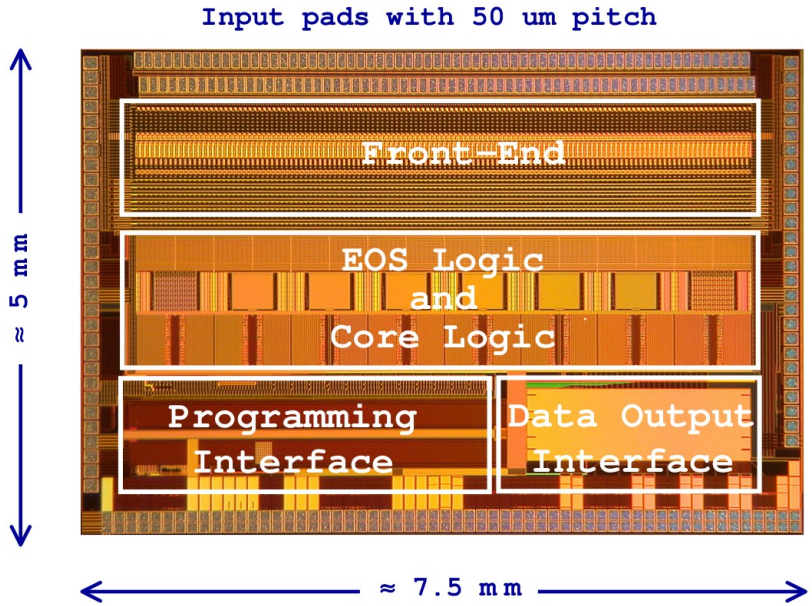


Efficiency along the detector



FSSR2 RO chip

- Fermilab Silicon Strip Readout chip v2
  - The chip has been developed by an INFN Pavia & Bergamo and Fermilab for the BTeV strip detectors
- 128 analog channels, with address and time information for all hits
- Self-triggered readout architecture, with digital output only
- Read out up to 70 MHz
  - Operated at 20 MHz @ testbeam

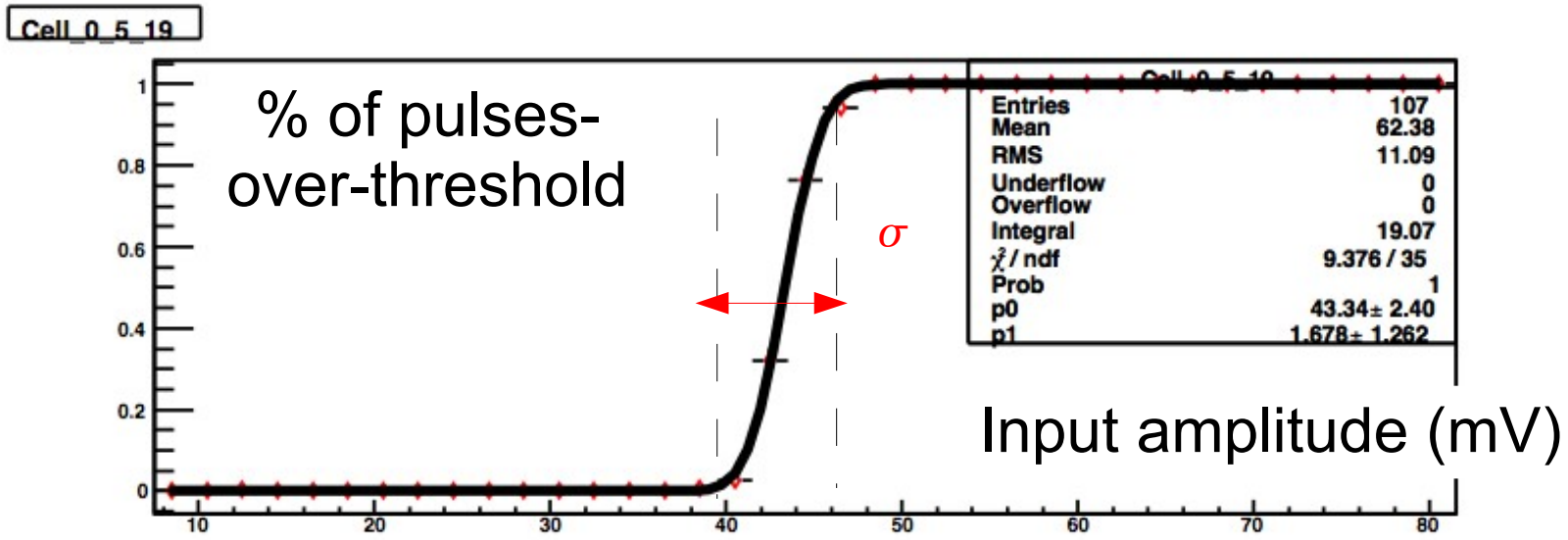


FSSR2- cont'd

- 8 programmable thresholds, with the 0^{th} one acting as hit/no hit discriminator
  - Each channel has its own set of 8 comparators
- 3-bit ADC information is provided for each hit
- Programmable gain and peaking time
- Baseline restorer available
- Optimized for positive signals
  - Limited dynamic range for n-side: just hit/no hit information for negative signals
- News from Valerio Re about FSSR2 (talk earlier today)

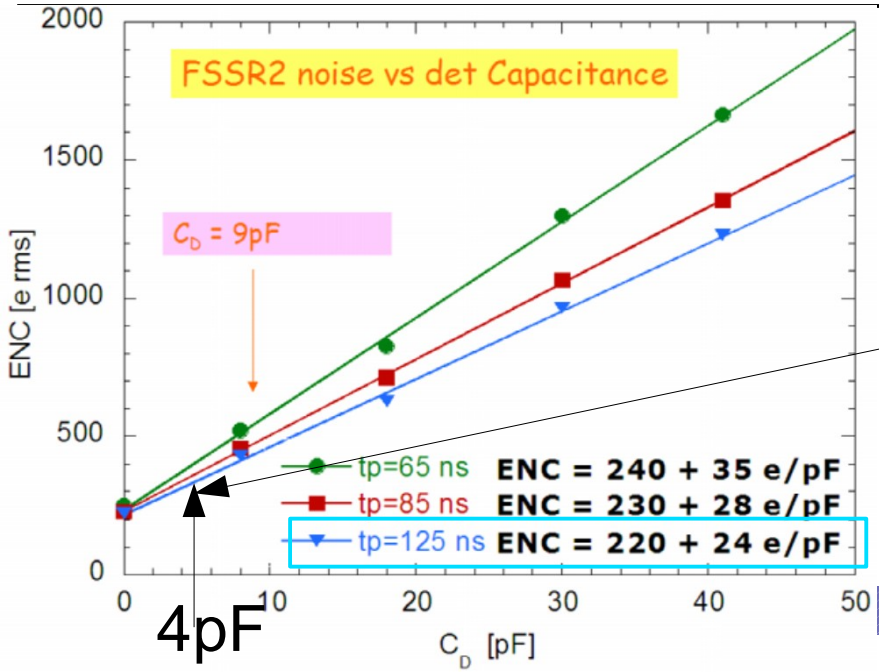
FSSR2 calibration

- Noise was estimated using FSSR2 internal-calibrator, during beam test
- At fixed threshold, input amplitude was increased, and fraction of pulses-over-threshold recorded
- The result is fitted with an erf function, where σ is the estimated noise



Noise measured @ Slim5 2008 test-beam

Detector	Striplets		Telescope	
Polarity	p side	n side	p side	n side
Noise (e^- RMS)	560	978	400	742
S/N	29	16	60	32
Gain (mV/fC)	96	67	97	67



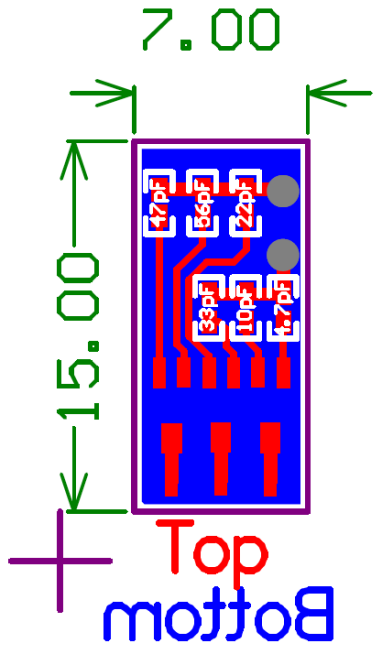
About 316 enc*

At test-beam we were very close to benchmark for telescope detector on p-Side

*= expected for p-Side of telescope

To Do List

- More temperature points
- Change shaper parameters
- Measure striplets-module capacitance
  - Sensor + fanout + ecc
- Bond FSSR2 channels to capacitors to measure noise as a function of capacitance
- A new DAQ… (see next slide)



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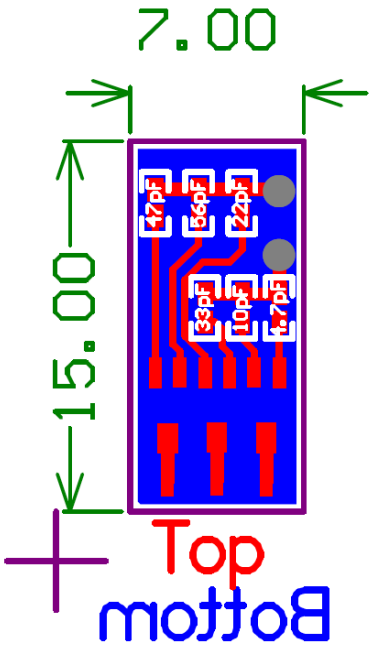
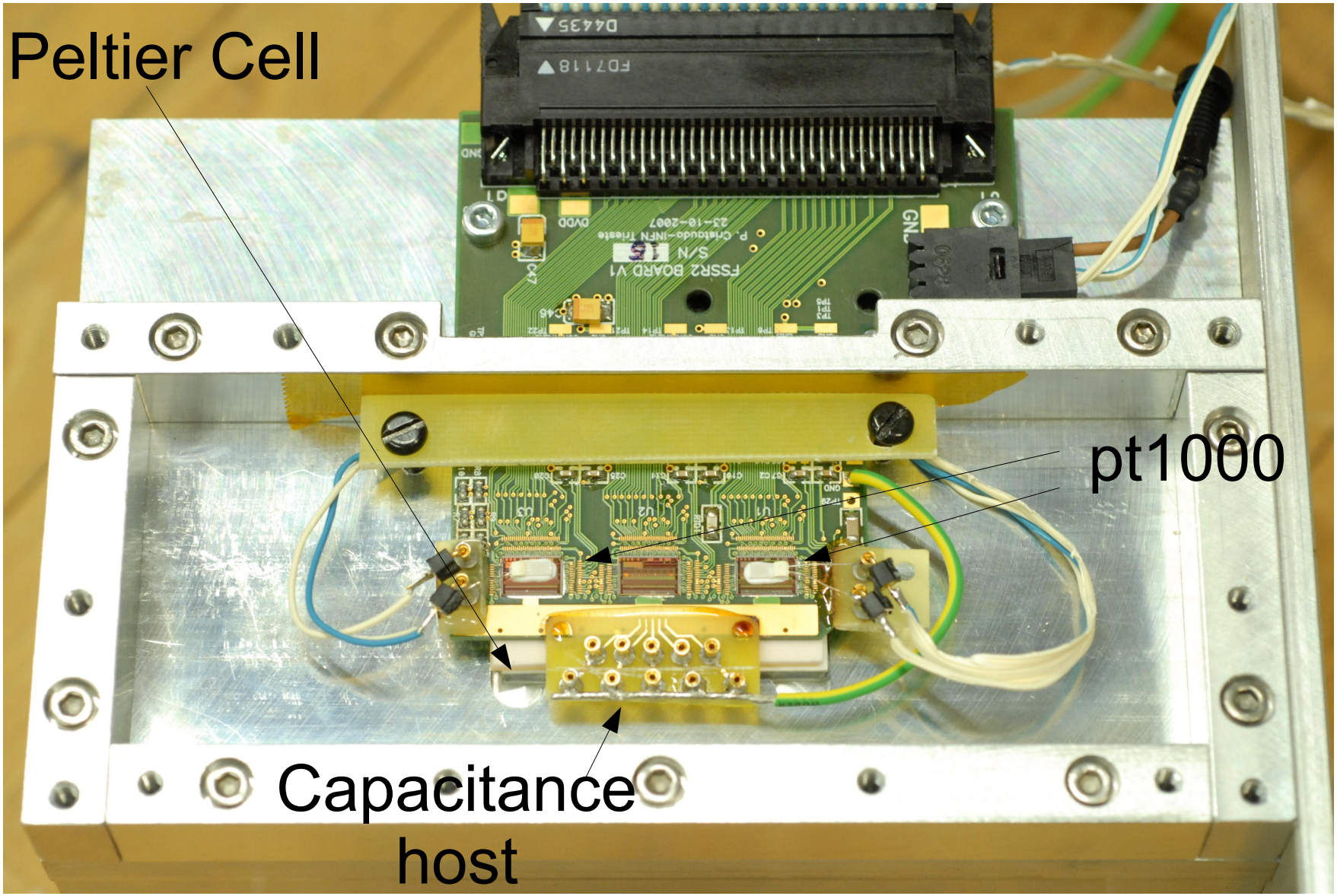
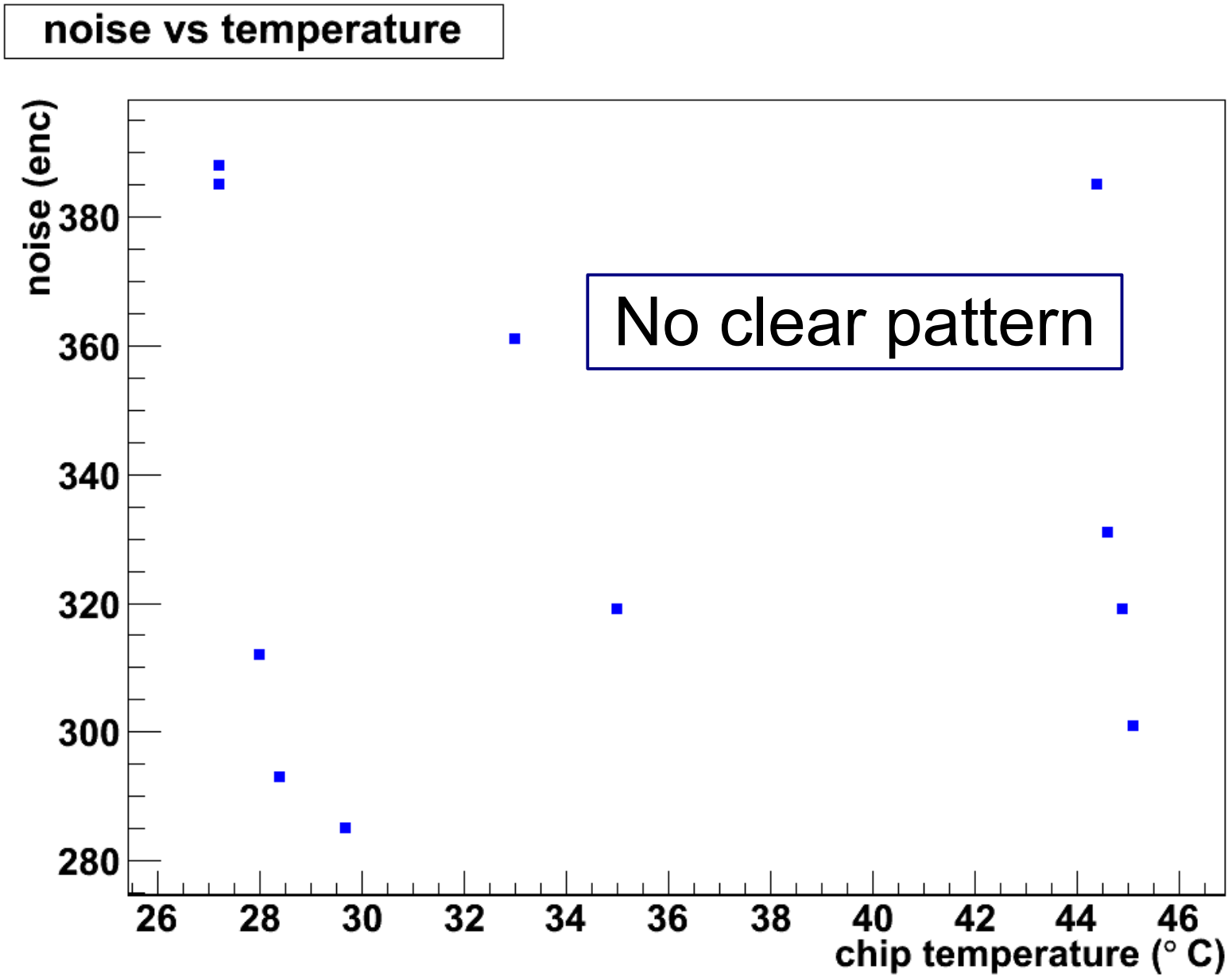
As seen in Annecy



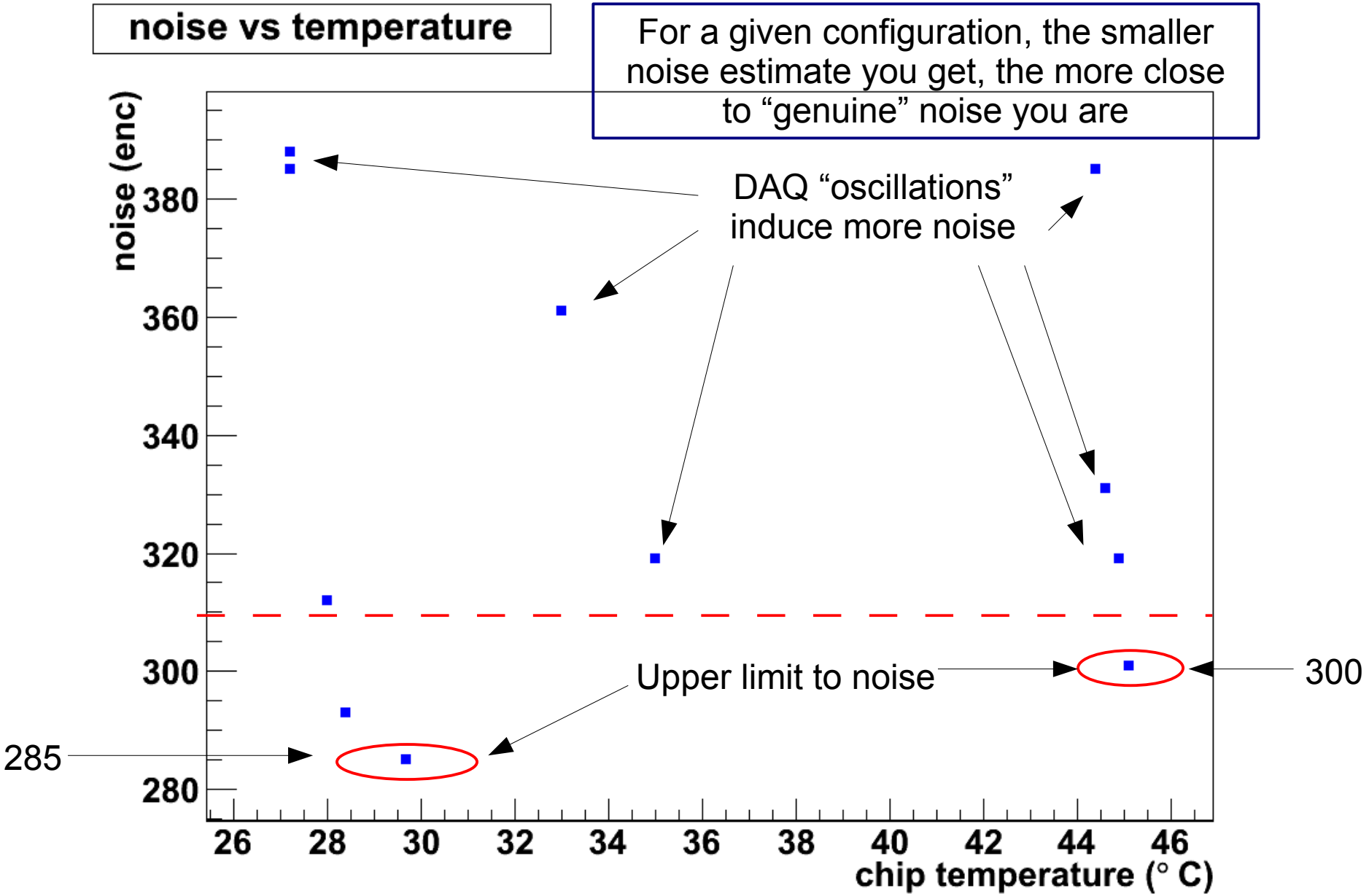
Setup in Trieste lab



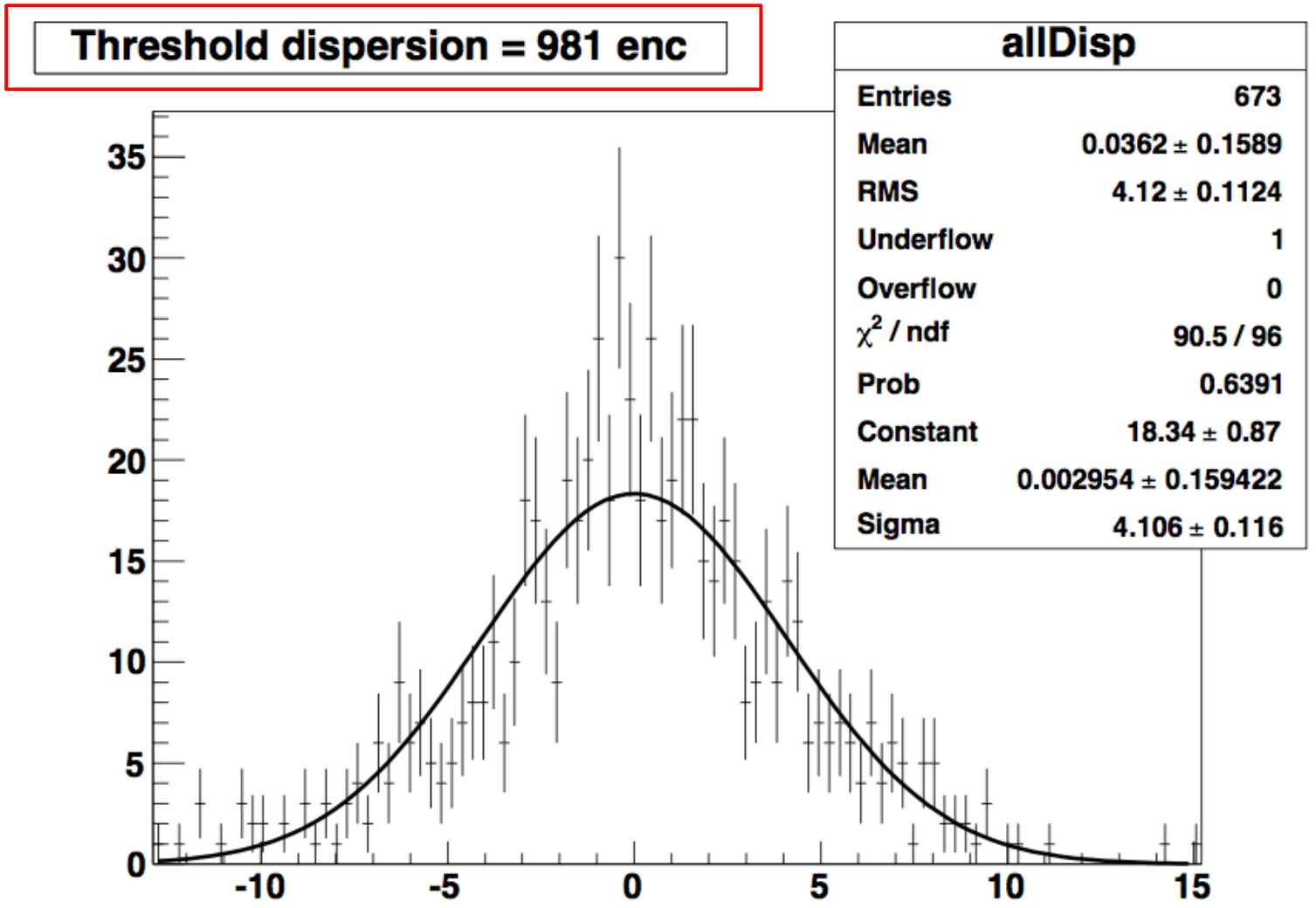
Noise Vs Temperature



Heuristic caveat



Threshold dispersion



We strongly suspect its a POMONE related feature

The BTeV DAQ chain

- We used Pomone to test FSSR2 chips and all strip detectors
- We received the whole chain with practically no written instructions
  - But we received “online” support
- One piece only
- We put it back to work
  - Tough reverse-engineering
- Not always reproducible behaviour
- We observe non-negligible variations in noise measurements
- Roughly half of the calibrations got aborted...

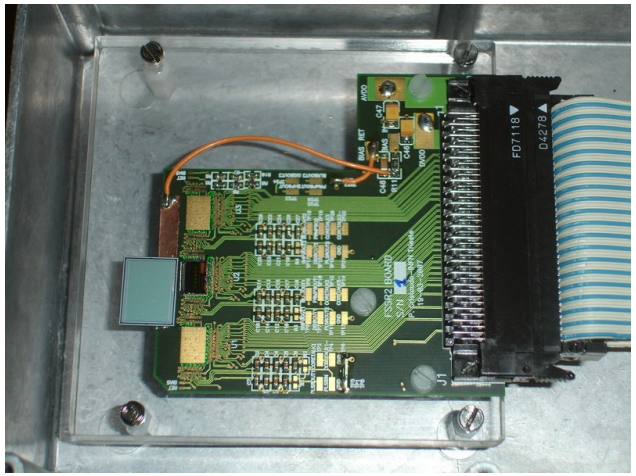
Noise Vs shaper, integrator, BLR parms

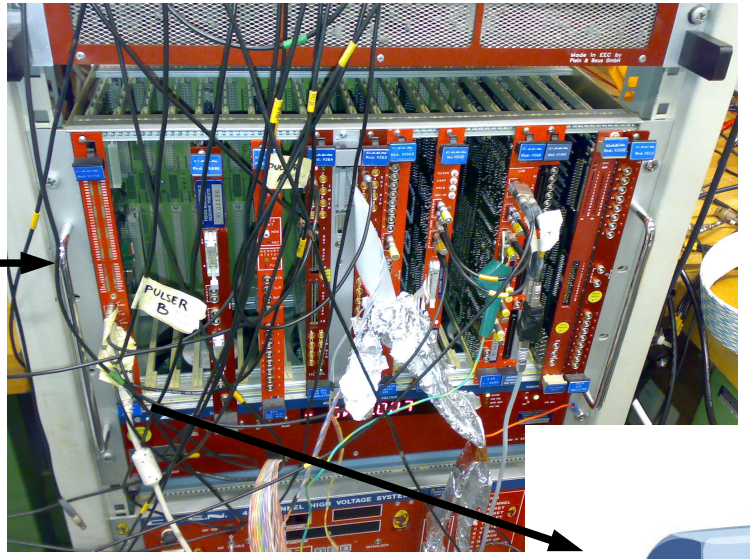
- We would like to study the noise performance as a function of the shaper, integrator and BLR parameters
  - 4 8-bit registers
  - Each controls a current in a section of the logic of FSSR2
- We started varying default values
- But...
- ... but due to old DAQ, quantitative results couldn't be reached
- Massimo Manghisoni is looking into FSSR2 projects to understand better what each DAC does in detail
- We (re)discovered functionality ranges for each register

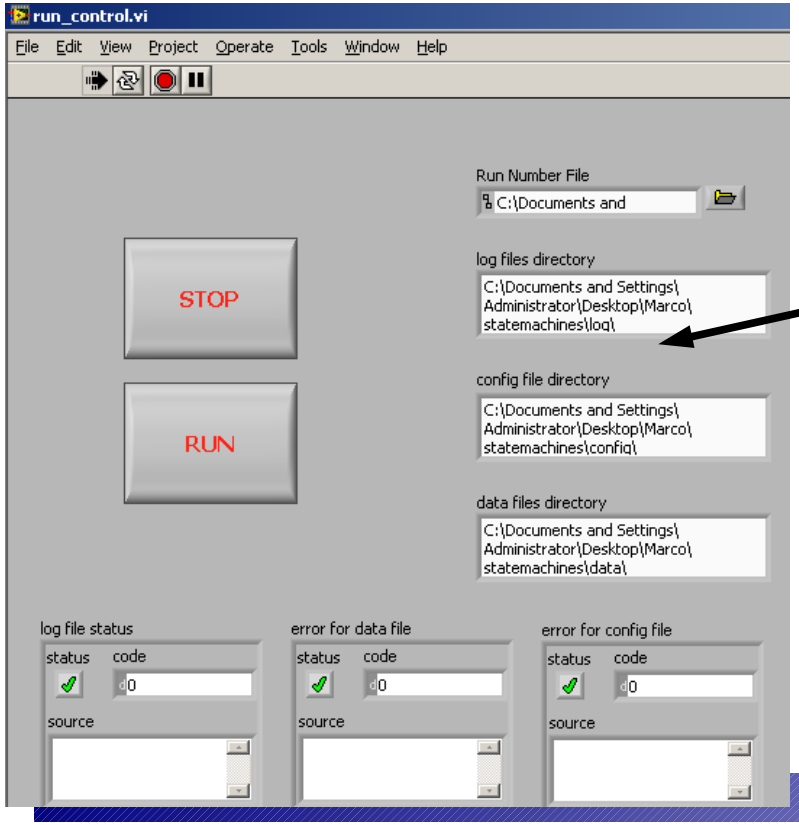
New DAQ

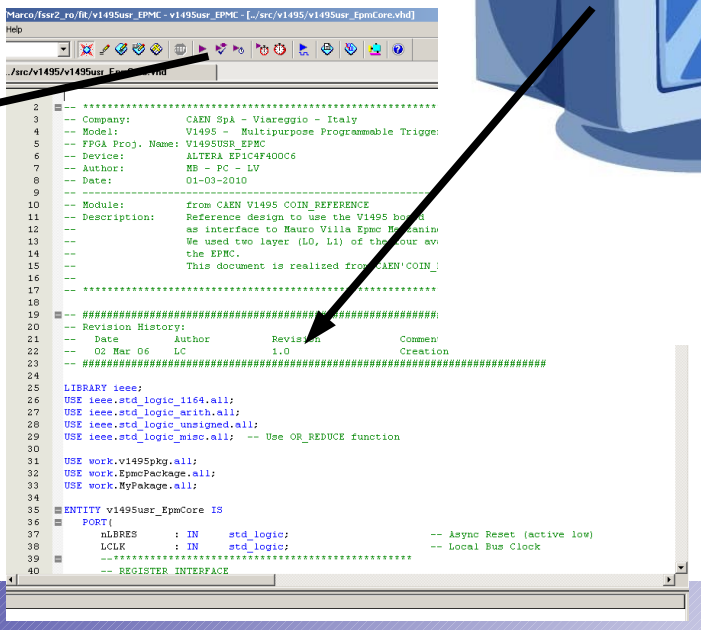
- We are developing a new DAQ, which is based on a CAEN board which has FPGAs
- We will program chips and read data through a VME-USB bridge and a Labview-based acquisition program
- Status: FPGA is programmed (many thanks to Mauro Villa)
- First tests ← NEW
  - See next slides...

New DAQ scheme

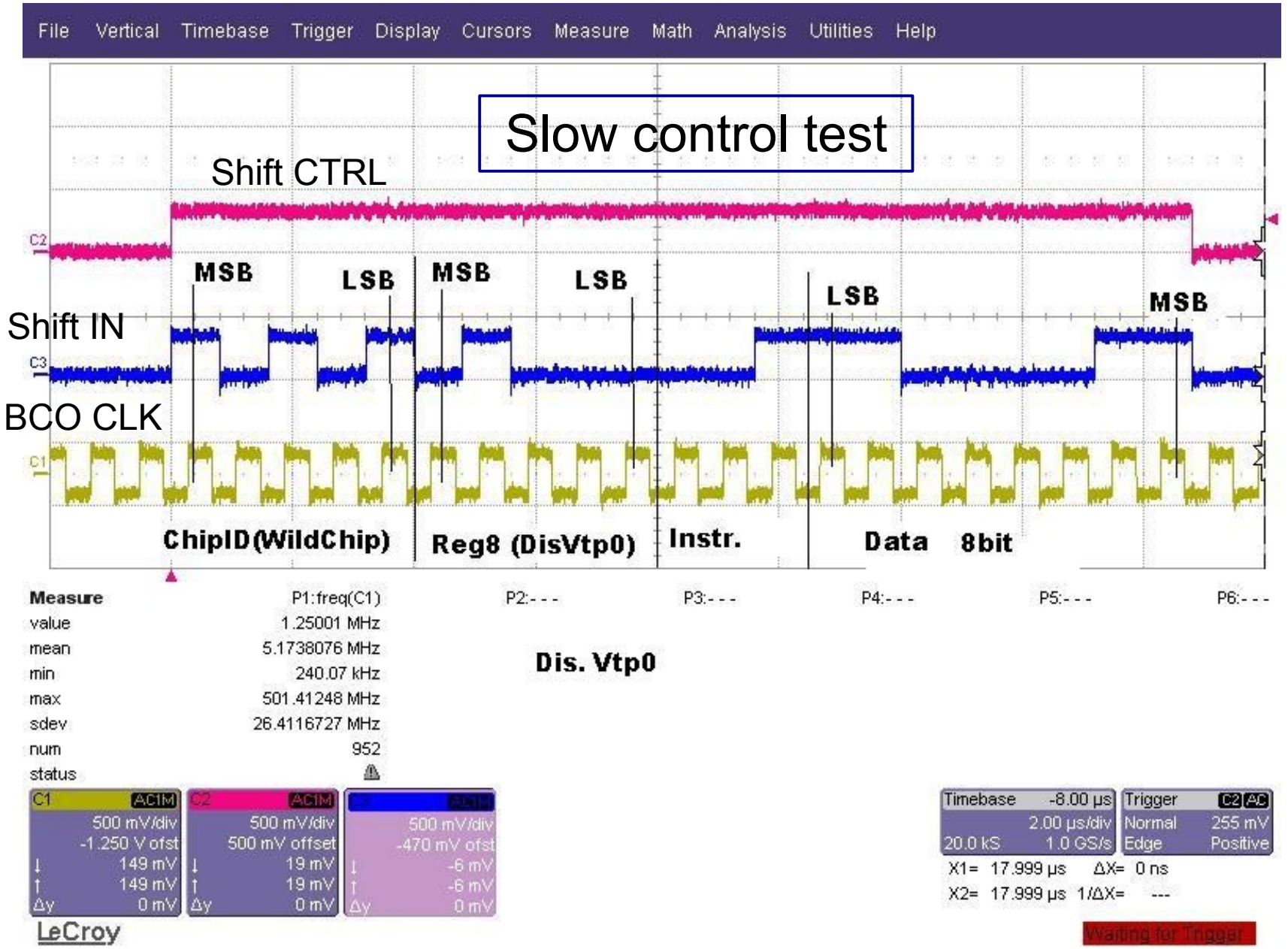








First signals



New studies with new DAQ

- Thanks to new DAQ, we plan to study the hit-efficiency as a function of channel occupancy
  - Test will be (slightly) limited by RAM size
- The idea is to use few events but very close in time
- We will use the IR laser to “light” several strips and study the efficiency as a function of FSSR Clock and Readout Clock

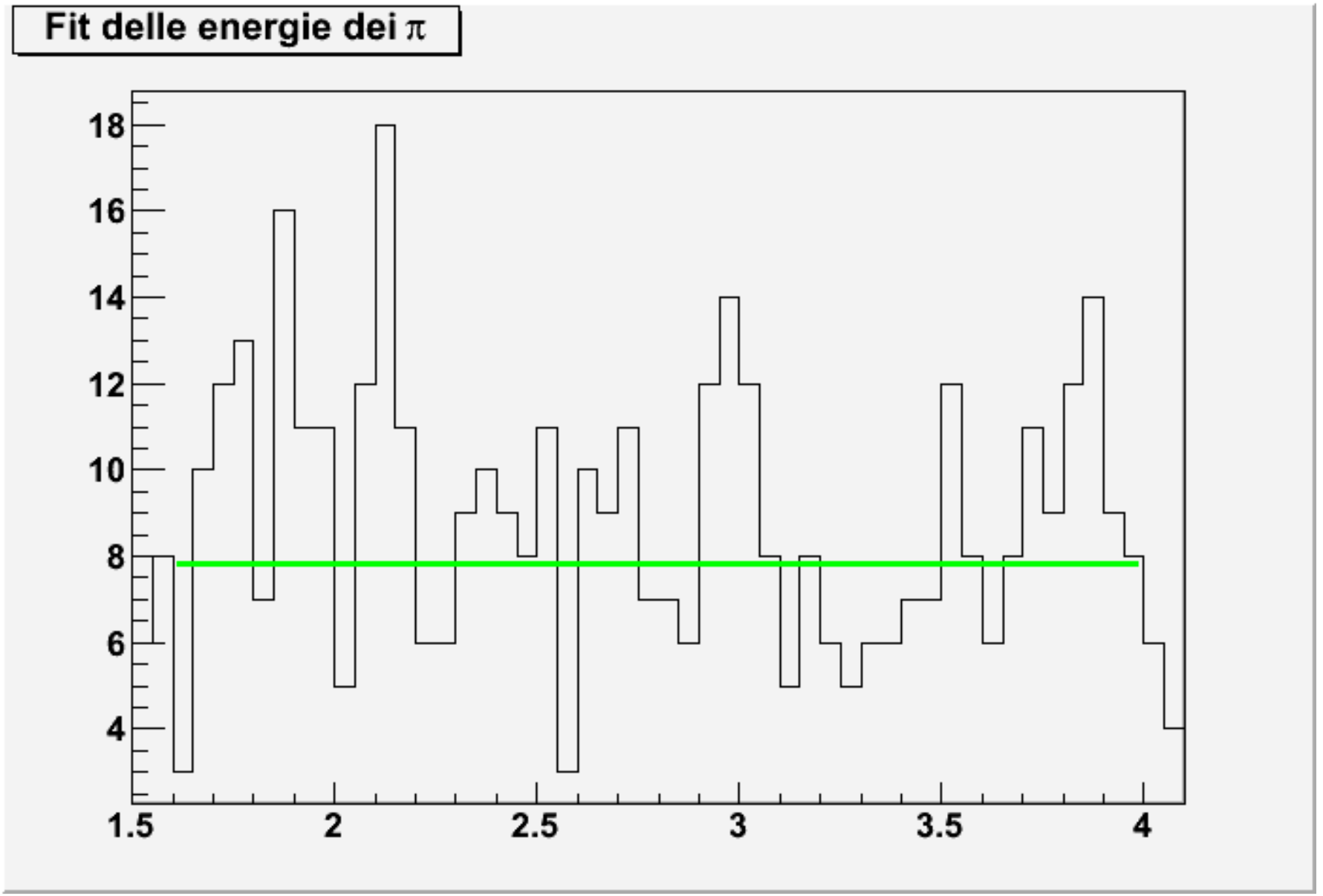
dE/dx in SVT

- Increasing interest in dE/dx capabilities in SVT
  - "Pairs" could possibly be rejected on a dE/dx basis
- FSSR2 provides a 3-bit ADC information for each hit
- How to set the 8 thresholds?
  - 0^{th} threshold acts as hit/no-hit discriminator
  - 7^{th} threshold contains limited information
  - Range Vs Granularity

dE/dx and simulated data

- We started looking at full simulated events
  - Pairs
  - Single particle (*e.g.* π, for a given energy range)
- We will “digitize” the released energy in SVT layers by using a scheme a la FSSR2
- We will try to understand several things
  - How thresholds need to be set
  - What is the optimal number of adc bits
    - → 3? More than 3?

Pion energy spectrum



Conclusions

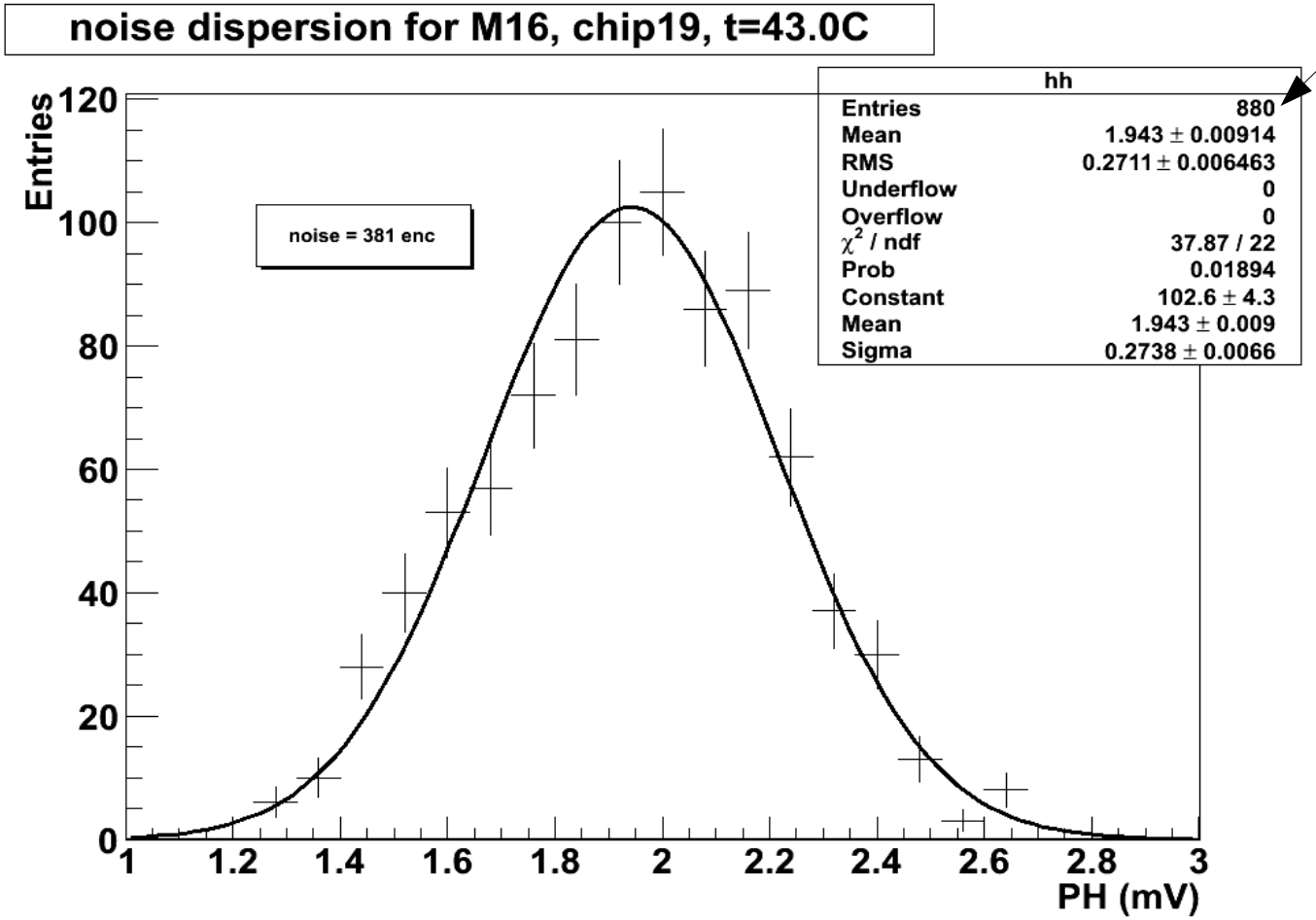
- There is a lot of activity about striplets and the FSSR2 RO-chip in Trieste
- Oscillation of old DAQ prevented us to unambiguosly measure electronic noise
- We will use new DAQ for studying noise versus
  - Temperature
  - Load capacitance
  - Shaper parameters
- We will study also hit-efficiency Vs occupancy
- dE/dx study started
  - using simulated data

That's it

Backup slides

Noise measurements in Trieste

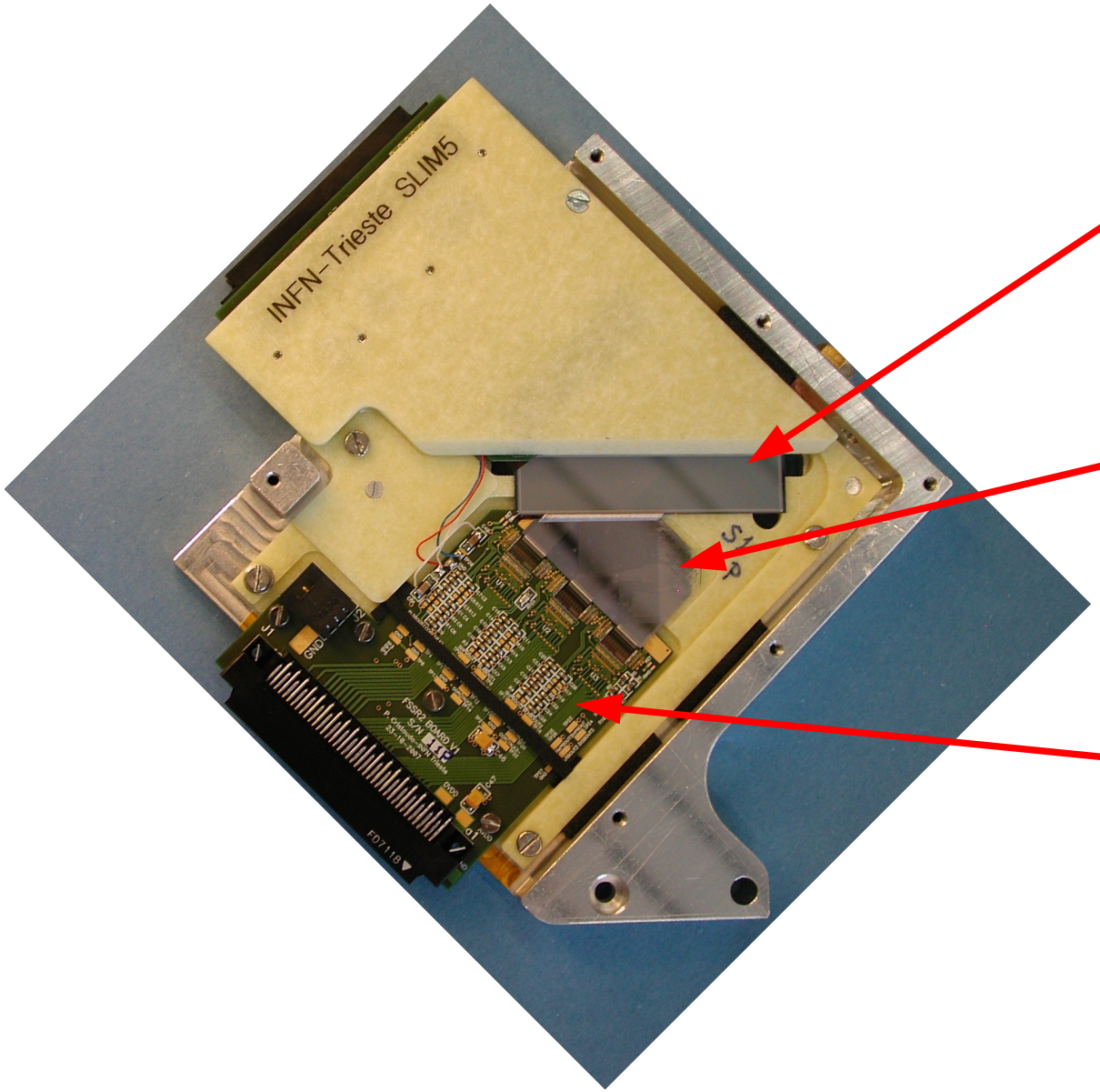
- Calibration performed with FSSR2 internal pulser and old BTeV test-beam DAQ chain
- 8 (thresholds) x 128 (channels) injected
  - Not all fits do converge
  - Some extra-counts enter the fit



Slim5

- R&D Italian collaboration
- Mission: "Pushing thin tracking-devices state-of-the-art for High Energy Physics"
- Highlights:
  - MAPS → not in this talk!
  - Striplets
  - Double sided telescope
  - Data-driven DAQ-architecture
  - Test beam in 2008 @ CERN – PS
- Paper ready for submission

Assembled striplet module

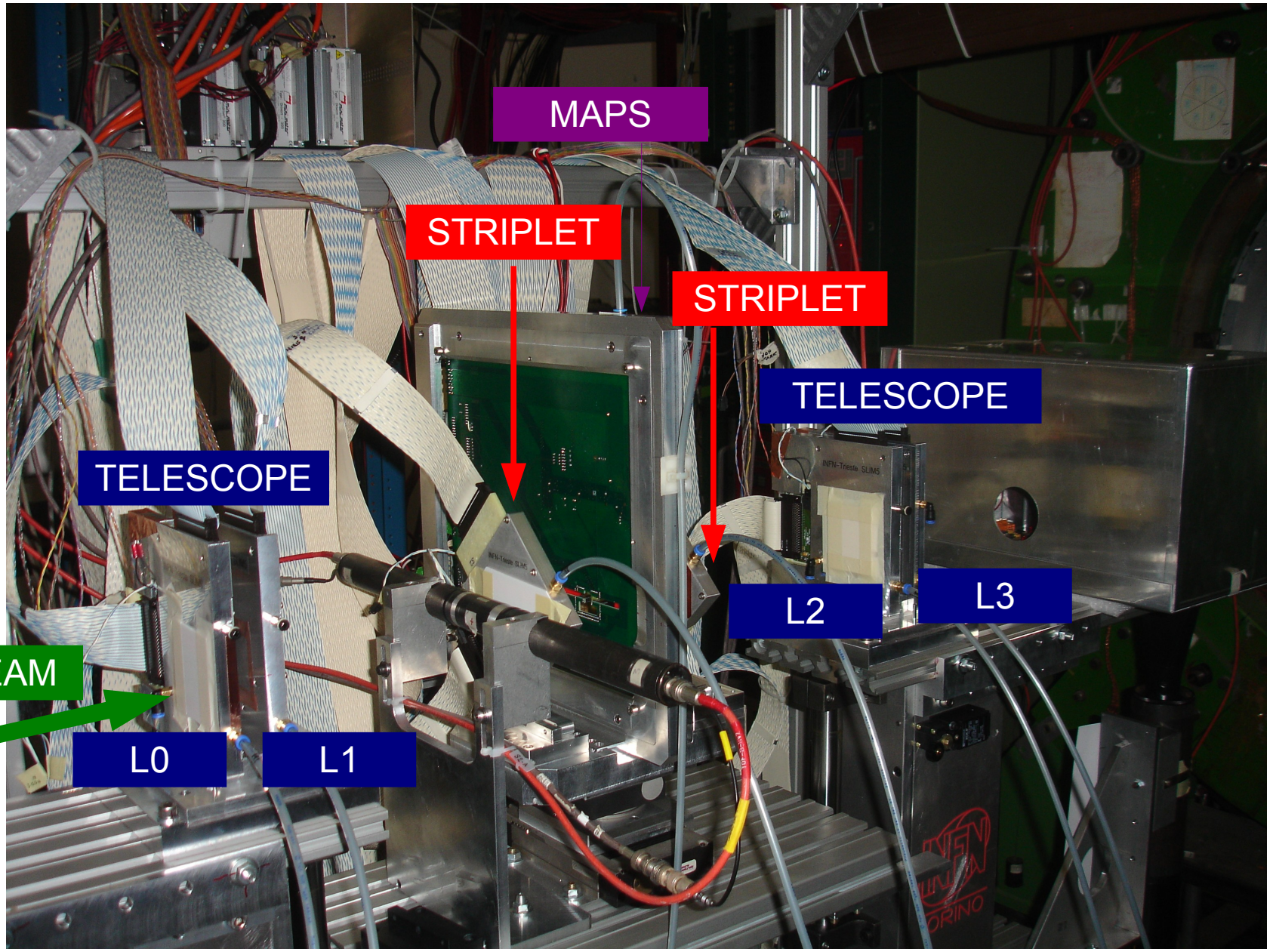


Striplet sensor

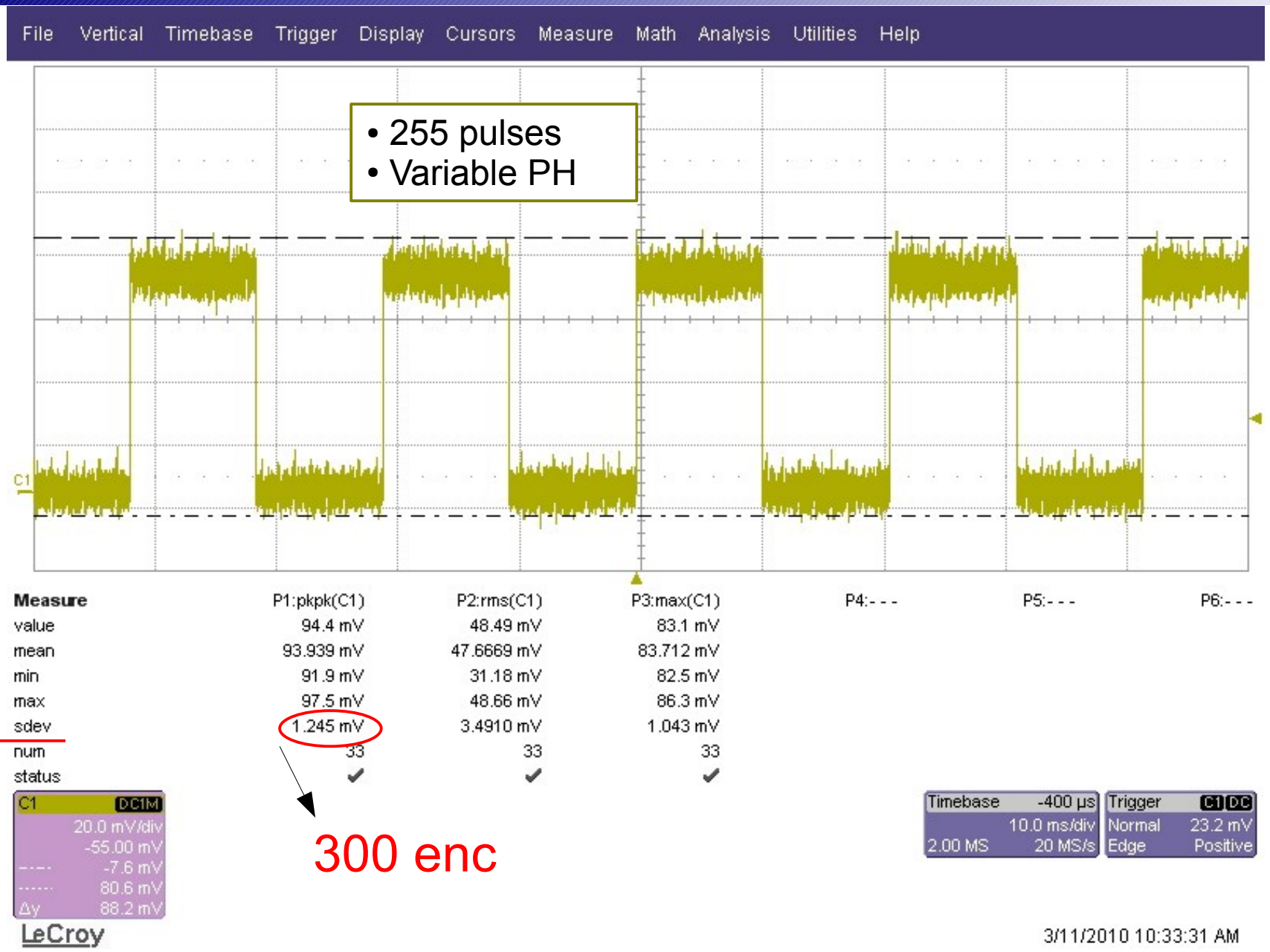
Fanout circuit
(Aluminum traces on quartz)

Hybrid with 3 FSSR2 chips

Slim5 – Test beam setup



NEW: Internal pulser oscillations



dE/dx: preliminary results