PId Front end chip: PIF

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LPNHE/IN2P3 Paris

C. Beigbeder, D. Breton, J. Maalmi, **V. Tocut**,
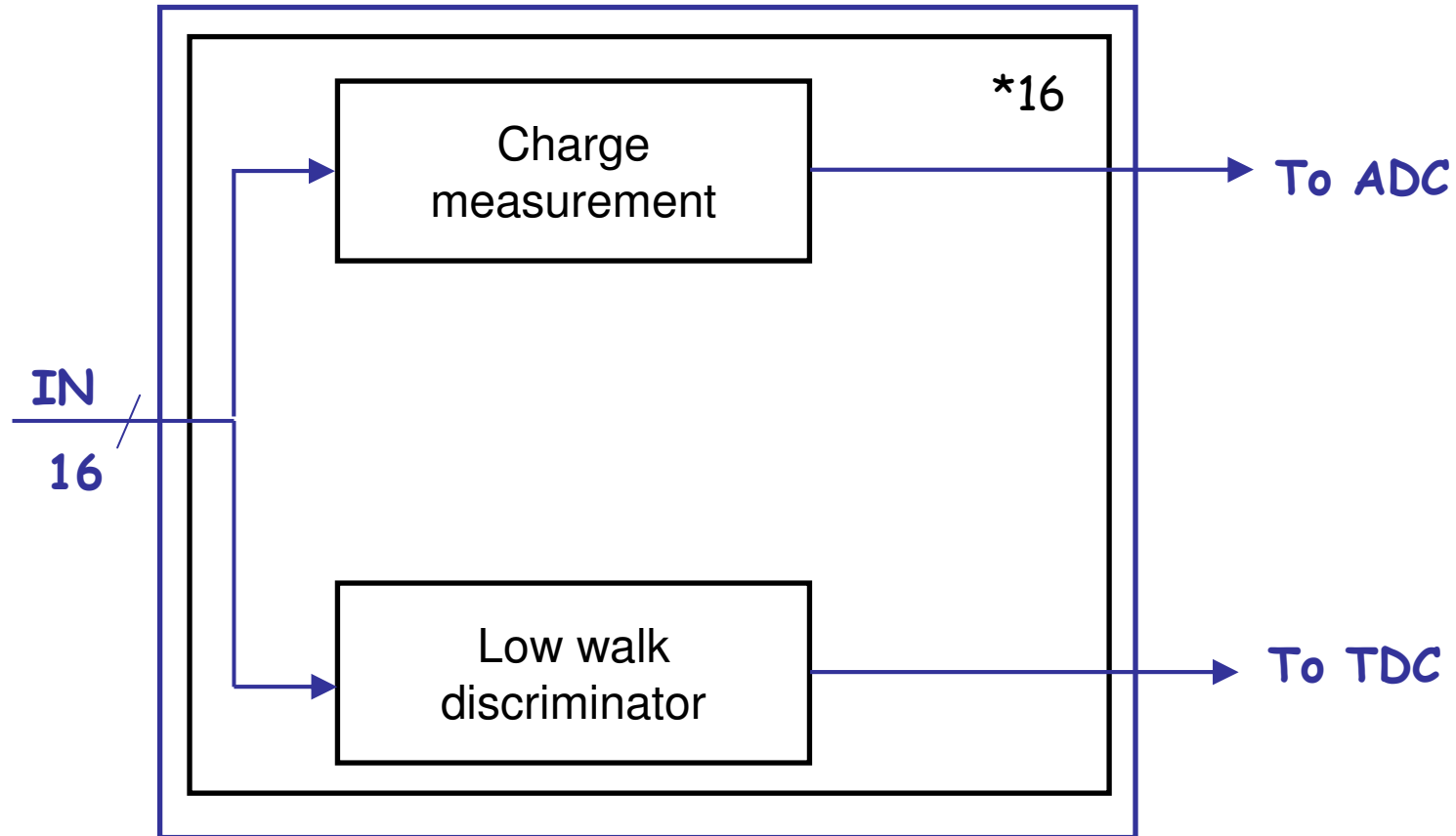LAL/IN2P3 Orsay

Requirement reminder

- Time measurement
  - ⇨ 100ps resolution max
  - ⇨ 1MHz background rate max
  - ⇨ 50ns double pulse resolution min

- Charge measurement
  - ⇨ necessary?
  - ⇨ dynamic range?
  - ⇨ fine or coarse?

- PM monitoring
  - ⇨ fine or coarse? (signal reconstruction or charge measurement)
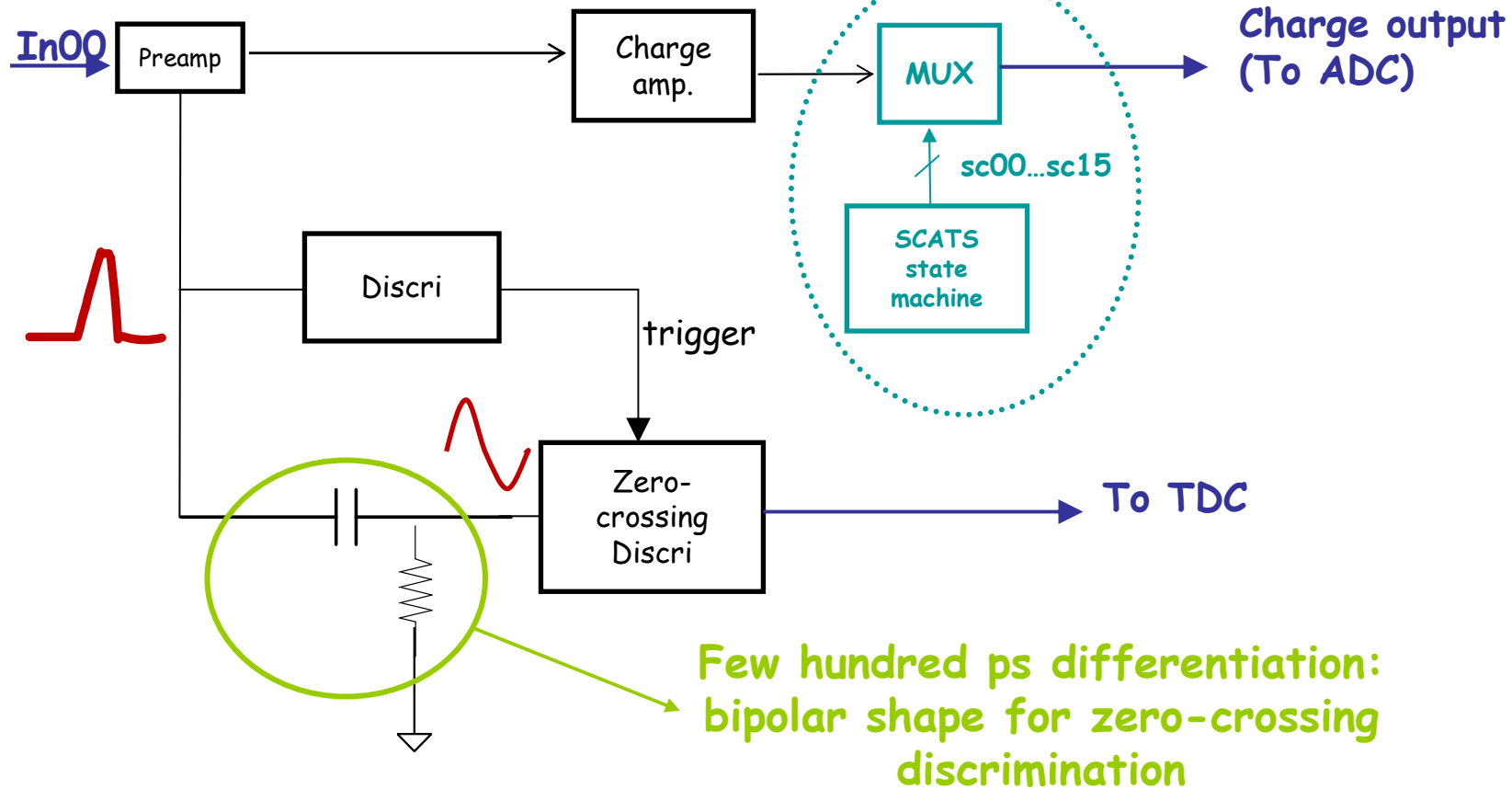 - ⇨ during dedicated runs?

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Proposal #1: Babar like

⇩ 'CFD' like

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Proposal #1: Babar like (cfd)

Needed only if charge measurement is required for physics

Charge output (To ADC)

InOO

Preamp

Charge amp.

MUX

sc00...sc15

SCATS state machine

Discri

trigger

Zero-crossing Discri

To TDC

Few hundred ps differentiation: bipolar shape for zero-crossing discrimination

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Prop. #1: Babar like (cfd)

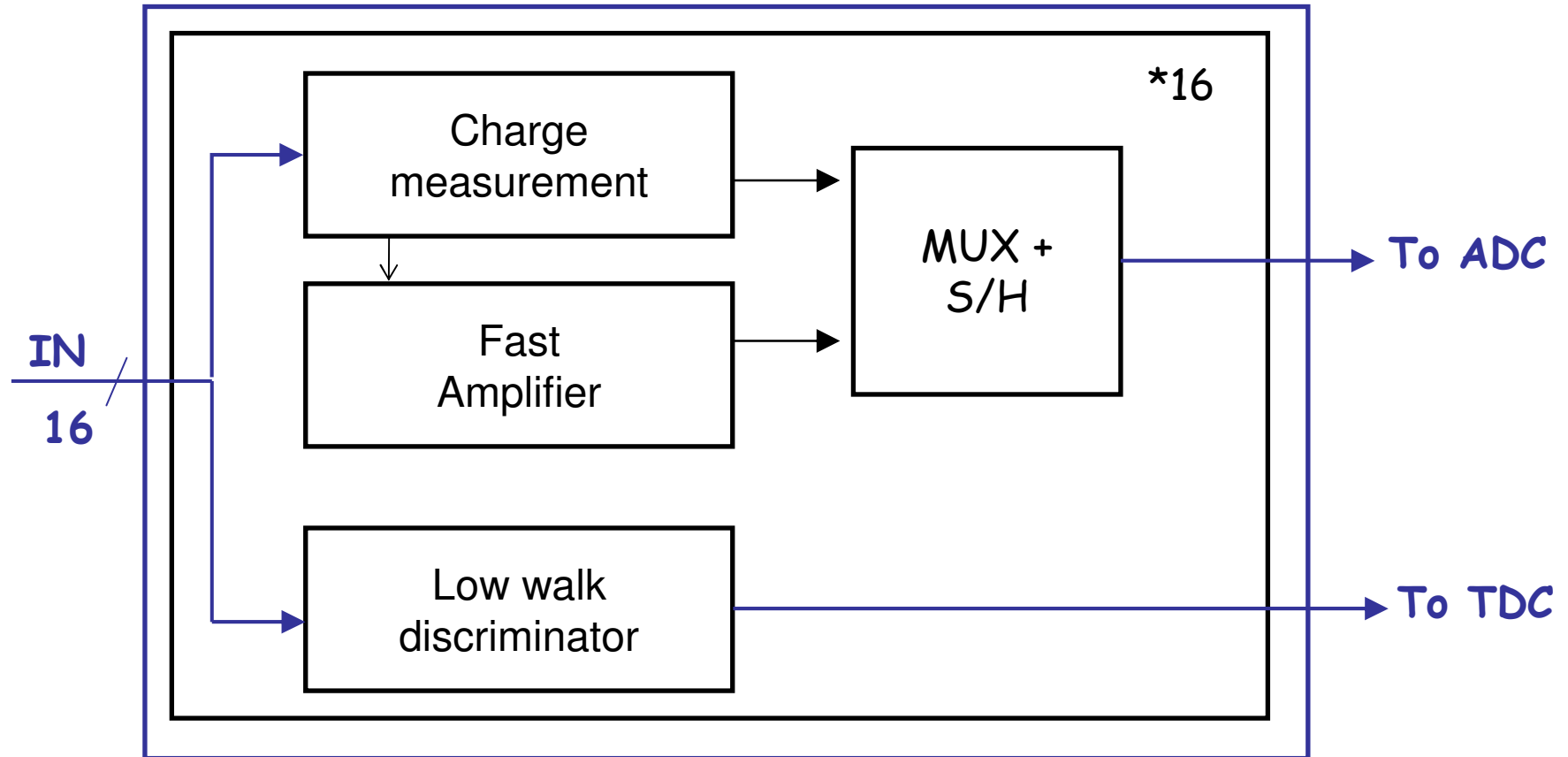| +++	---
• No walk correction if walk < 50ps (depending on PM dynamics)	• « Time + charge » data synchronization (if charge is required for physics) • Coarse charge measurement • Necessity to know the peak jitter • No fine PM monitoring

2 different chips developed:

❶ analog front end {PIF}: ↳ **simple** zero-crossing design but discrimination at the
                                            peak
                                      ↳ could be available soon in a well-known (and existing)
                                            technology
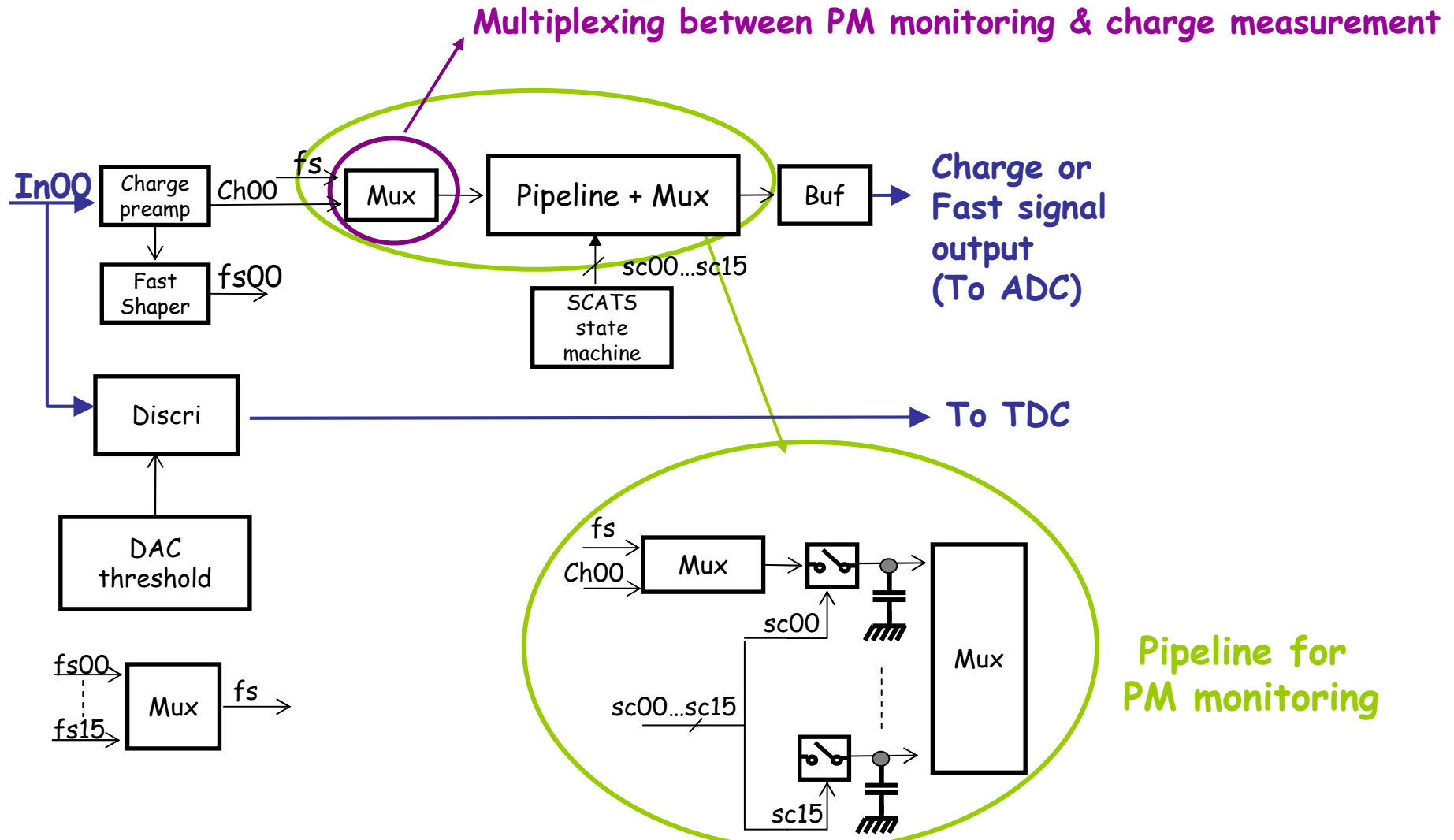
❷ time measurement {SCATS}

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Prop. #2: upgraded prop #1

Charge measurement

Fast Amplifier

MUX + S/H

Low walk discriminator

*16

IN

16

To ADC

To TDC

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Prop. #2: upgraded prop #1

Multiplexing between PM monitoring & charge measurement

In00

Charge preamp → Ch00

Fast Shaper → fs00

fs → Mux → Pipeline + Mux → Buf → **Charge or Fast signal output (To ADC)**

SCATS state machine → sc00…sc15

Discri → **To TDC**

DAC threshold

fs00 ⋯ fs15 → Mux → fs

fs / Ch00 → Mux → sc00 / sc00…sc15 / sc15 → Mux

Pipeline for PM monitoring

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Prop. #2: upgraded prop #1

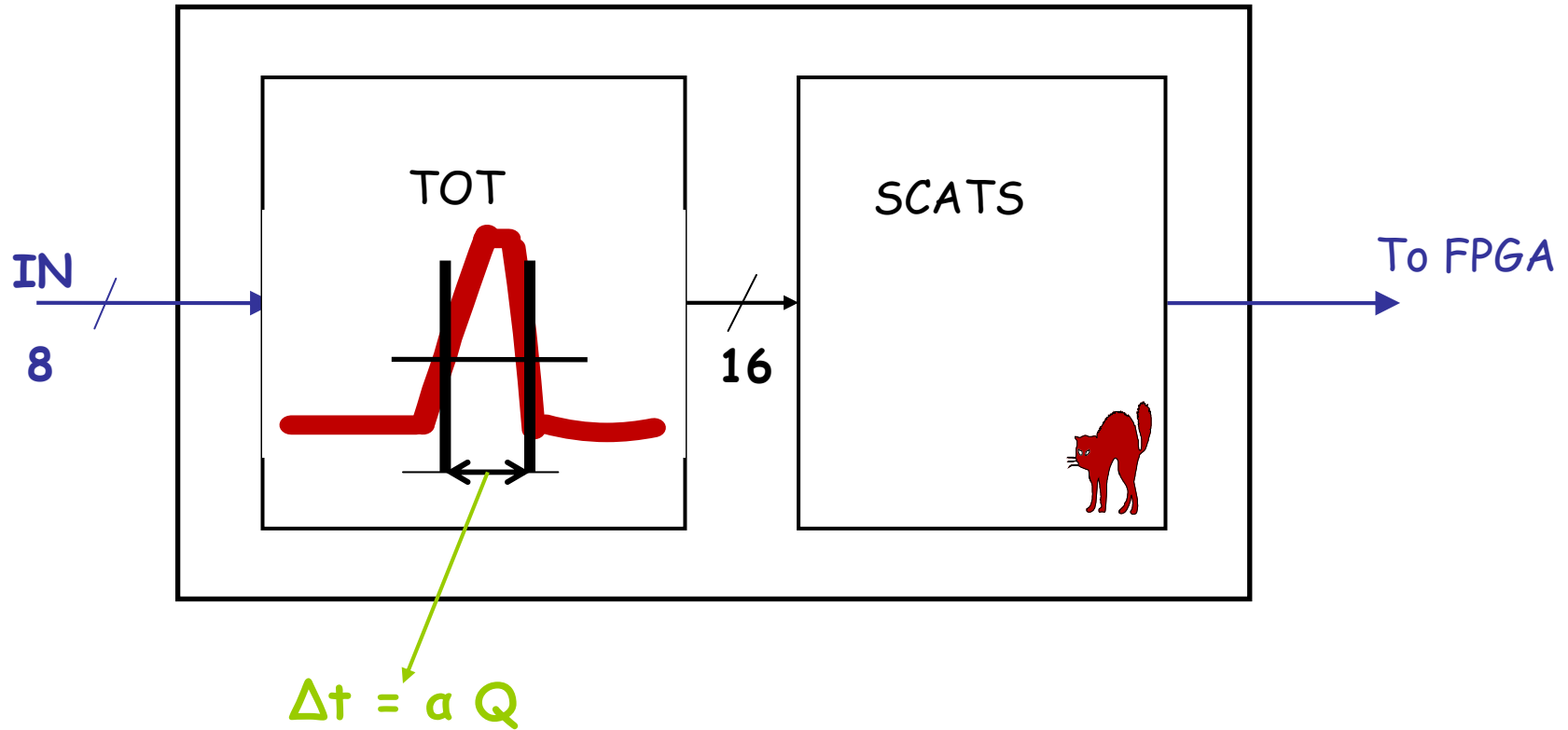| +++	---
• Fine charge measurement • PM monitoring • No walk correction if walk < 50ps (depending on PM dynamics)	• « Time + charge » data synchronization

2 different chips developed:

❶ analog front end + monitoring **{PIF}**
❷ time measurement **{SCATS}**
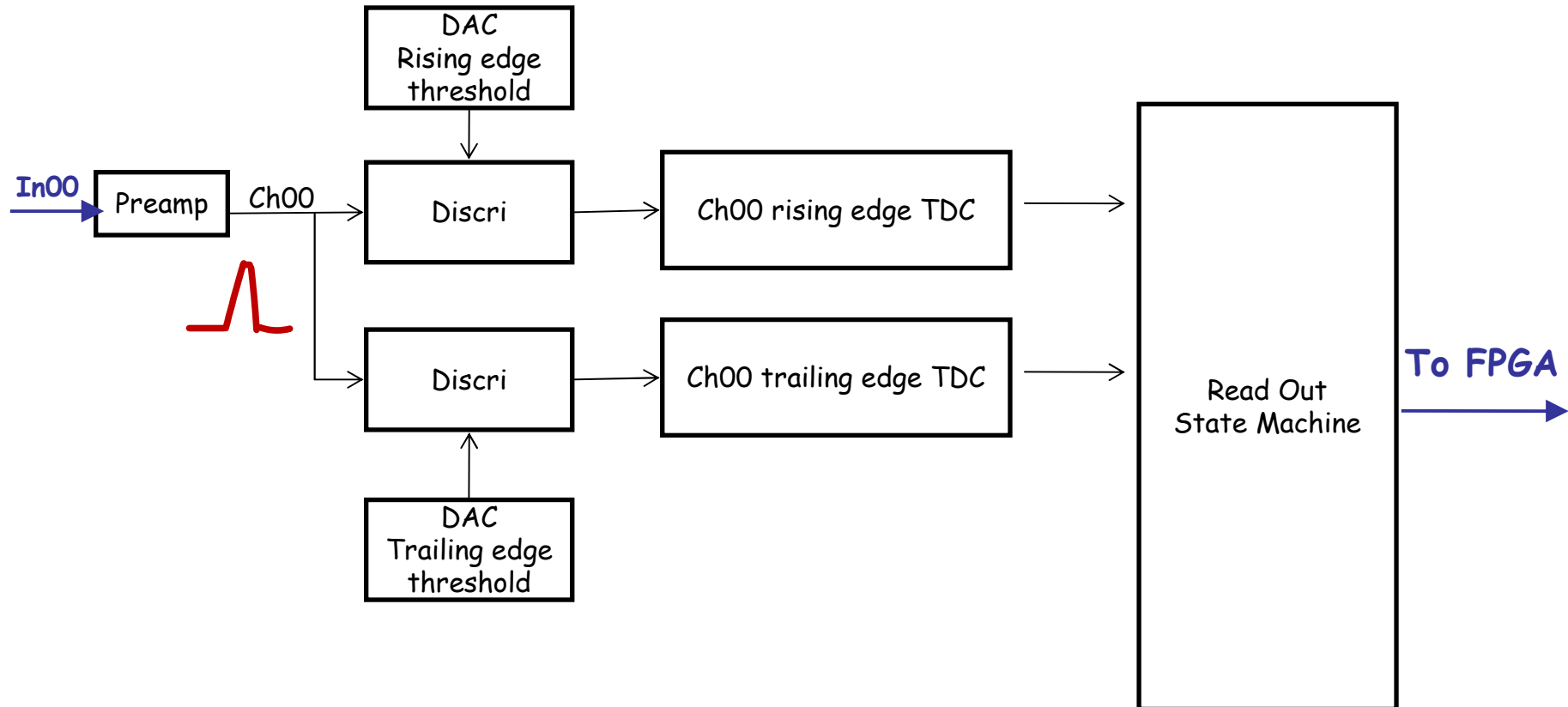
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Proposal #3: Time over Threshold (TOT)

IN

8

TOT

16

SCATS

To FPGA

$\Delta t = \alpha\, Q$

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Proposal #3: TOT

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Proposal #3: TOT

+ + +	**- - -**
• No « Time + charge » data synchronization problem • Only 1 chip (discri + time in SCATS)	• PM signals need to be very reproductible • No PM monitoring or very coarse • No precise charge measurement • Number of channels for time measurement has to be doubled

2 different chips developed:

❶ Physic dedicated **{TOT+SCATS}**: ↪ **simple** (SCATS almost already exists)
↪ available soon in a well-known (and existing) technology

❷ Monitoring dedicated IC

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Summary on decisions to be taken

↳ Charge measurement

↳ PM dynamic range

↳ PM monitoring: precise or not?

↳ Signal reproductibility

↳ Peak jitter

➤ **To be defined ASAP**

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Milestones

- ## In case of prop.#1 or 2:

  - ➢ first simulations with XFAB 0.18μm CMOs tech.: end of June
  - ➢ design with AMS 0.18μm CMOS tech.: unknown (tech not available for the moment)

- ## In case of prop.#3:

  - ➢ first simulations with AMS 0.35μm CMOs tech.: end of June
  - ➢ design with AMS 0.35μm CMOS tech.: autumn (in collaboration with LPC Caen)

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