Characterization of the FE chips for the hybrid pixels



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XIII SuperB General Meeting La Biodola, Isola d'Elba (Italy) May 30 - June 4, 2010

outline

- → main features of the FE chip
 - analog cell
 - readout architecture
- → tests in lab
 - noise scans and injection scans
- → conclusions and plans

overview

- GOAL \rightarrow matrix of 256x200 pixels (50x50 μ m² pitch, active area of 1.3 cm²) bump-bonded to a sensor matrix (200 μ m thick)
- WE HAVE TESTED → several front-end prototype chips of 32x128 pixels with a data-push readout architecture, no sensor connected



analog cell



- comparator threshold common to all pixels
- possibility to inject a charge up to 12fC in selected pixels
 - MIP on 200 μ m Si \rightarrow 2.6fC
 - Cinject = 10fF
- the output of the preamplifier is carried out and it is accessible (for 2 pixels only)

readout architecture (1)

F. Giorgi

MP (x,y)

(x+1)

column enable (X)

(x)

- the matrix is divided in 2 submatrices with independent and parallel readout;
- each submatrix is divided in macropixels (MP) 2x8 pixels; each pixel is identified by two lines: data out and column enable
- the MP is active if the latch enable is high \rightarrow \rightarrow definition of an observation window
- if at least one pixel of the MP is hit, both the columns of the MP will be read and a DataValid (DV) bit is associated to the bytes read from the matrix

readout architecture (2)



then get out of the submatrix

tests in lab

 GOAL → test the readout architecture performances, characterize the analog cell, understand the trend of the most important features along the matrix

• noise scan \rightarrow noise parameters

• injection scan \rightarrow gain curve

first look

- a little was bug discovered: data out lines are not set to 0 after the readout of the pixels but the sparsifier logic does not take into account this feature;
- the bug is completely understood;
- all the tests of the matrix are still possible: fake hits are eliminated;
- the test procedure is a little bit slower and therefore we have characterized the matrix patchy.

Noise Scans

- GOAL → extract the baseline and the noise parameters (no sensor connected)
- SAMPLE \rightarrow 3 chips, 3 macrocolumns (MC) for each submatrix

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• MC = 6, MC = 20, MC = 30
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Х

y



Noise Scan example

Larger pixels

Virtuoso® Layout Editing: A

I Terminal

📄 icfb – Log: /home/morsani/ 🔣 Library Manager: WorkArea 📄 LSV

Noise Scan results

СНІР	MC	baseline - μ (mV)	μ threshold noise - dispersion (mV)	
1	6	$\textbf{205.9} \pm \textbf{0.3}$	1 .6 %	0.460 ± 0.007
	20	$\textbf{205.3} \pm \textbf{0.3}$	1.8%	$\textbf{0.448} \pm \textbf{0.006}$
	30	$\textbf{205.6} \pm \textbf{0.3}$	1.5%	$\textbf{0.460} \pm \textbf{0.007}$
2	6	$\textbf{212.0}\pm\textbf{0.3}$	1.5%	0.35 ± 0.01
	20	211.1 ± 0.3	1.4%	$\textbf{0.37} \pm \textbf{0.01}$
	30	$\textbf{210.5} \pm \textbf{0.3}$	1.7%	0.41 ± 0.01
3	6	$\textbf{208.8} \pm \textbf{0.3}$	1.4%	0.323 ± 0.005
	20	$\textbf{209.3} \pm \textbf{0.2}$	1.2%	0.362 ± 0.007
	30	$\textbf{208.0} \pm \textbf{0.3}$	1.4%	0.355 ± 0.008

Injection Scans

- GOAL \rightarrow extract the gain (mV/fC)
- SAMPLE \rightarrow 3 chips, 3 macrocolumns (MC) for each submatrix

Injection Scan sequence*

Injection Scan example

estimator of the height of impulse out of the preamplifier

gain extraction - chip2

Inject Scan results

CHIP	MC	gain (mV/fC)	gain dispersion	offset (mV)
1	6	41.4 ± 0.2	5.6%	174.9 ± 0.3
	20	41.9 ± 0.2	5.0%	174.7 ± 0.4
	30	41.4 ± 0.2	5.3%	175.0 ± 0.3
2	6	40.3 ± 0.2	6.0%	176.0 ± 0.4
	20	40.1 ± 0.2	5.2%	175.5 ± 0.3
	30	40.7 ± 0.2	5.4%	176.1 ± 0.4
3	6	39.1 ± 0.2	5.4%	173.6 ± 0.3
	20	39.1 ± 0.2	5.9 %	172.8 ± 0.2
	30	39.7 ± 0.2	5.5%	172.6 ± 0.3

Characterization of FE chips

	post layout simul.	CHIP1	CHIP2	CHIP3
baseline (mV)	180	205.6 ± 0.5	211.2 ± 0.5	208.7 ± 0.5
threshold dispersion (e-)	350	490 ± 50	500 ± 50	450 ± 50
ENC (e-)	120	69 ± 2	59 ± 3	55 ± 2
gain (mV/fC)	45	41.6 ± 0.3	40.4 ± 0.3	39.3 ± 0.3

conclusions and plans

- a bug has been recognized, understood and tamed;
- Section 3 FE chips have been characterized with positive results and a reasonable agreement with the expected performances;
- at the end of summer we expect to receive some chips inteconnected by bump-bonding to the sensors and we should start their characterization in lab beginning on september.

Bug & consequences (1)...

 the outenable is not set to 0 after the readout of an odd column if there is at least a hit (☆) in the odd column of the MP → fake hits (★)

UNLUCKY CASE

LUCKY CASE

...and countermeasure

 the outenable is not set to 0 after the readout of an odd column if there is at least a hit (☆) in the odd column of the MP → fake hits (☆)

Bug & consequences (2)...

 the outenable is not set to 0 after the readout of an odd column if there is at least a hit (☆) in the odd column of the MP → fake hits (★)

...and countermeasure

 the outenable is not set to 0 after the readout of an odd column if there is at least a hit (☆) in the odd column of the MP → fake hits (☆)

