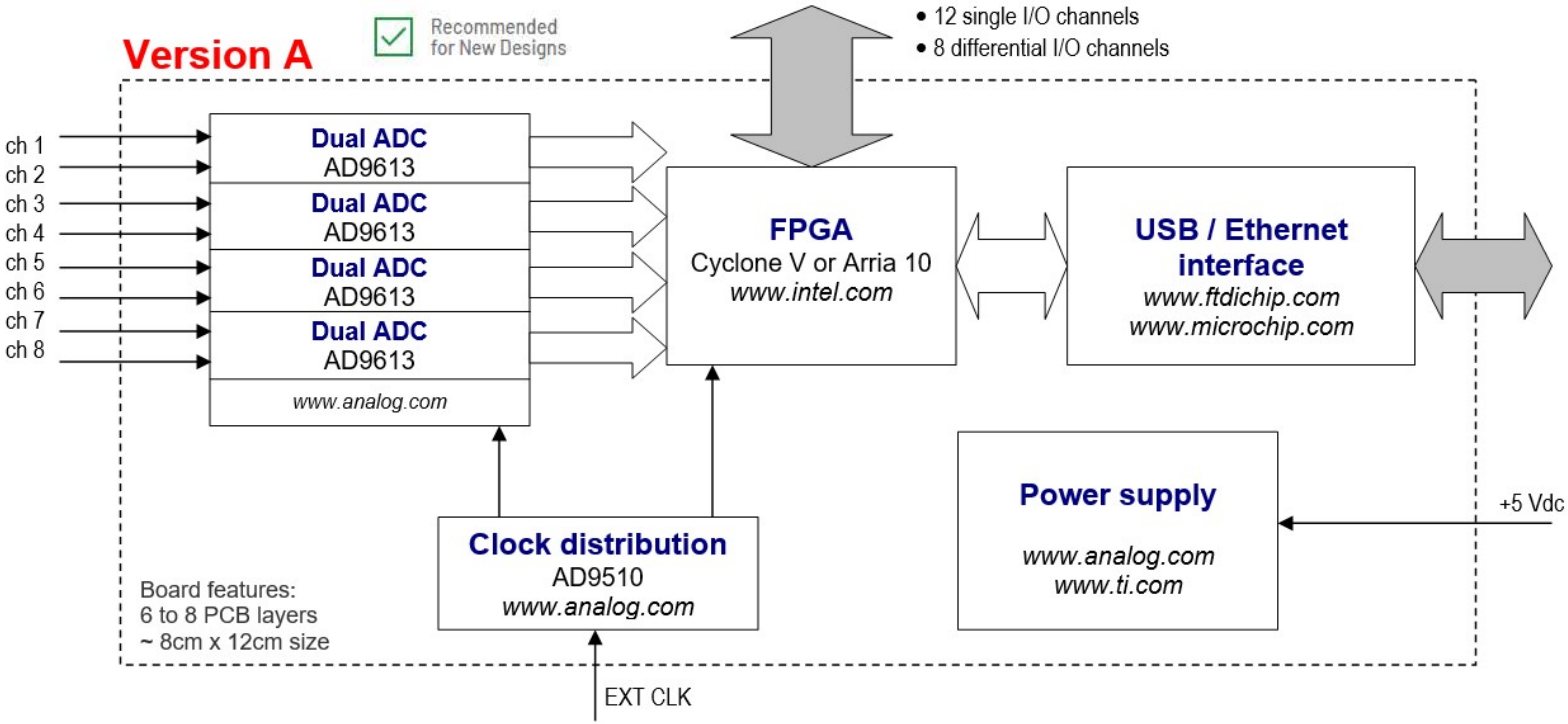
SiPM-DAQ module overview for CYGNO



Main features:

- programmable logic
- 8 digitizers 12bit@250MSPS
- 20 I/O channels
- USB/Wifi/Eth interface
- single +5V supply operation

Connectors and Devices:

- connectors : 8 coaxial LEMO, 30 pairs header type, 1 USB B type, 1 power
- 2 ADCs (*10mm x 10mm*)
- 1 clock distribution (*10mm x 10mm*)
- 1 FPGA
- 1 Serial Configuration Device (ex: EPCS64)
- 1 multichannel power device (ex: TPS75003)
- 1 USB interface (ex: FT2232H)

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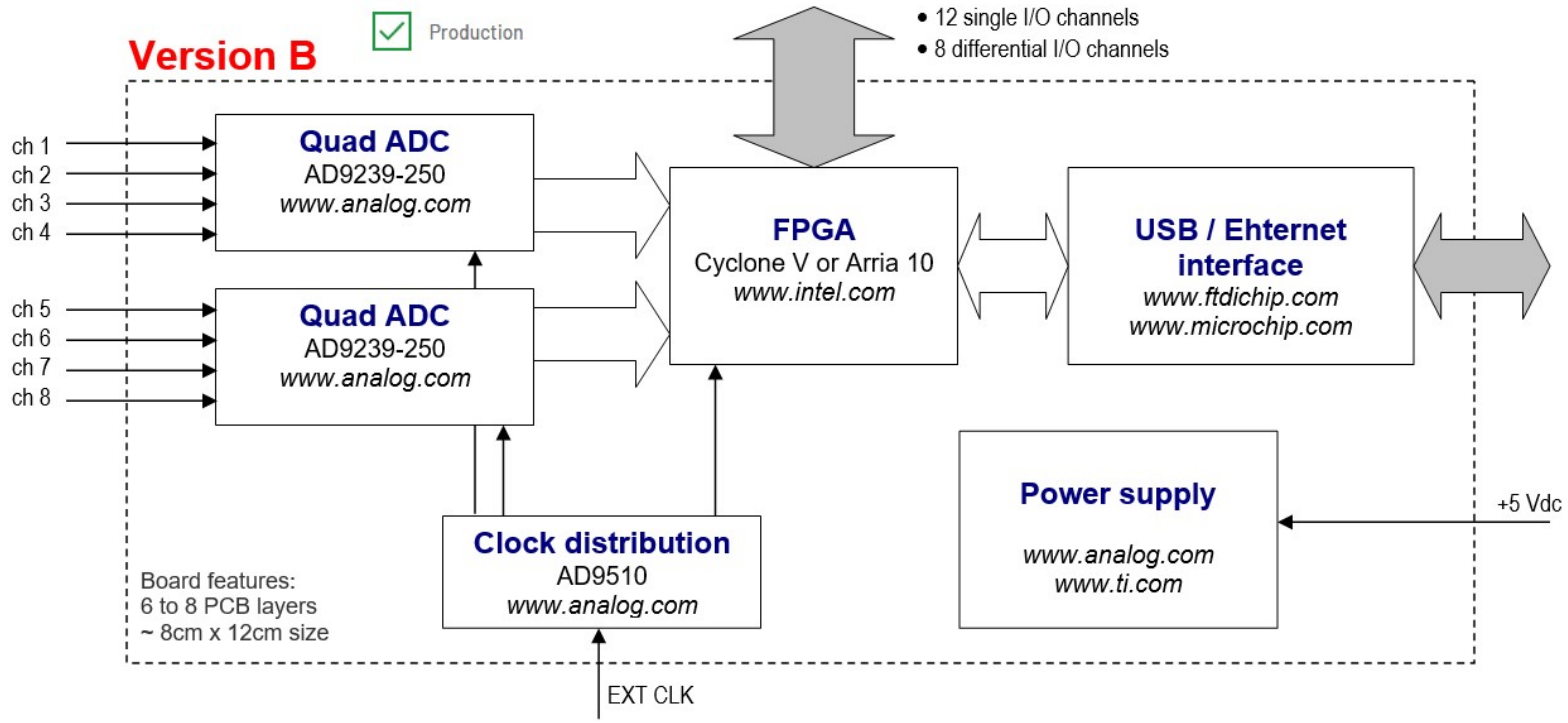

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Cost per module

(ADCs and FPGA with true cost (from Invoices) to Brasil. Items 3 to 5 are conservative estimates)

CYGNO SiPM Digitizer **DUAL-ADC – Version A**						
ITEM	Description	Part Number	Manufacturer	Unit Price (US$)	Units / module	Total (US$)
1	Dual 12-bit ADC, 250MSPS	AD9613BCPZRL7-250	Analog Devices	120,28	4	481,12
2	Arria 10 GX FPGA	10AX016C4U19E3SG	Intel	400,00	1	400,00
3	other components			300,00	1	300,00
4	PCB manufacturing cost (1)		Griffus	160,00	1	160,00
5	PCB mounting cost			100,00	1	100,00
					TOTAL	1.441,12

CYGNO SiPM Digitizer **QUAD-ADC – Version B**						
ITEM	Description	Part Number	Manufacturer	Unit Price (US$)	Units / module	Total (US$)
1	Quad 12-bit ADC, 250MSPS	AD9239BCPZ-250	Analog Devices	284,95	2	569,90
2	Arria 10 GX FPGA	10AX016C4U19E3SG	Intel	400,00	1	400,00
3	other components			300,00	1	300,00
4	PCB manufacturing cost		Griffus	160,00	1	160,00
5	PCB mounting cost			100,00	1	100,00
					TOTAL	1.529,90

Some initial questions to guide the ADC-FPGA selection for a SiPM-DAQ in CYGNO

TOPIC -- QUESTION

1. ADC -- How many ADC channels per module?
2. ADC -- 12 bits or 14 bits ADC vertical resolution?
3. ADC -- 250 MSPS (4 ns sampling) or 500 MSPS (2 ns sampling) ADC sampling rate?
4. ADC -- Is the ADC dynamic range very critical?
5. GENERAL -- What is the expected event rate from the SiPM?
6. GENERAL -- What is the bandwidth required between module and computer for data readout?
7. GENERAL -- What is the most adequate communication interface between module and computer (USB, Ethernet, other serial standard, VME)?
8. FPGA -- Is it interesting a powerful FPGA in order to do some high-speed DSP or not?
9. FPGA -- Is it interesting to have a built-in processor in the FPGA?

Some initial questions to guide the ADC-FPGA selection for the SiPM-DAQ in CYGNO

TOPIC -- QUESTION

1. ADC -- How many ADC channels per module? 8 channels
2. ADC -- 12 bits or 14 bits ADC vertical resolution? 12 bits
3. ADC -- 250 MSPS (4 ns sampling) or 500 MSPS (2 ns sampling) ADC sampling rate? 250 MSPS
4. ADC -- Is the ADC dynamic range very critical? NO
5. GENERAL -- What is the expected event rate from the SiPM? ???
6. GENERAL -- What is the bandwidth required between module and computer for data readout? ???
7. GENERAL -- What is the most adequate communication interface between module and computer (USB, Ethernet, other serial standard, VME)? USB or Ethernet.
8. FPGA -- Is it interesting a powerful FPGA in order to do some high-speed DSP or not? YES
9. FPGA -- Is it interesting to have a built-in processor in the FPGA? YES