ATLAS ITk Pixel Demonstrators

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on behalf of the ITk Pixel Collaboration

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Abstract

The ATLAS tracking system will be replaced by an all-silicon detector for the HL-LHC upgrade around 2025. The innermost five layers of the detector system will be pixel detector layers which will be most challenging in terms of radiation hardness, data rate and readout speed. A serial power scheme will be used for the pixel layers to reduce the radiation length and power consumption in cables. New elements are required to operate and monitor a serially powered detector including a detector control system, constant current sources and front-end electronics with shunt regulators. Prototypes for all subsystems are built to verify the concept and operate multiple serial power chains as a system test. The evaluation of both the readout of multi-modules and mechanical integration are further aims of the prototyping campaign. In the contribution, results will be presented of this prototyping effort. Moreover, details and features of serial powering for full detector systems will be given.

ITk Pixel layout and sub systems

The ITk will comprise both silicon pixel and silicon strip sub systems aiming to provide tracking coverage[a] up to $|\eta| < 4$. In total, there will be >10m^2 of pixels and 165m^2 of strips.

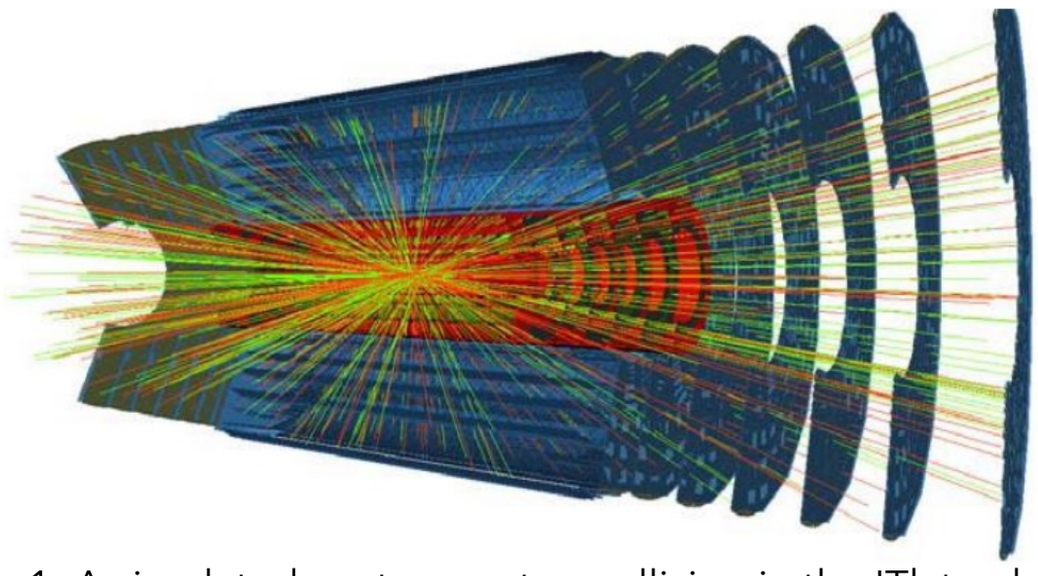


Fig. 1: A simulated proton-proton collision in the ITk tracker. A pile-up[b], μ~200 is expected at typical HL-LHC luminosities.

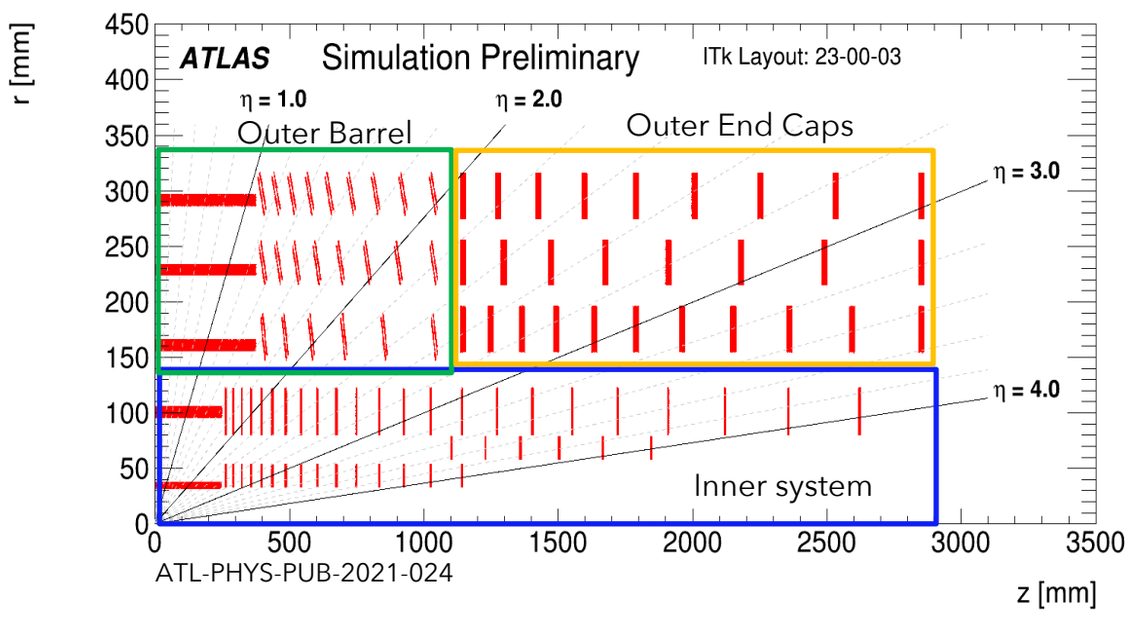


Fig. 2: A layout quadrant for the ITk Pixel detector showing the relative positions of the Inner and Outer pixel Systems.

Serial powering

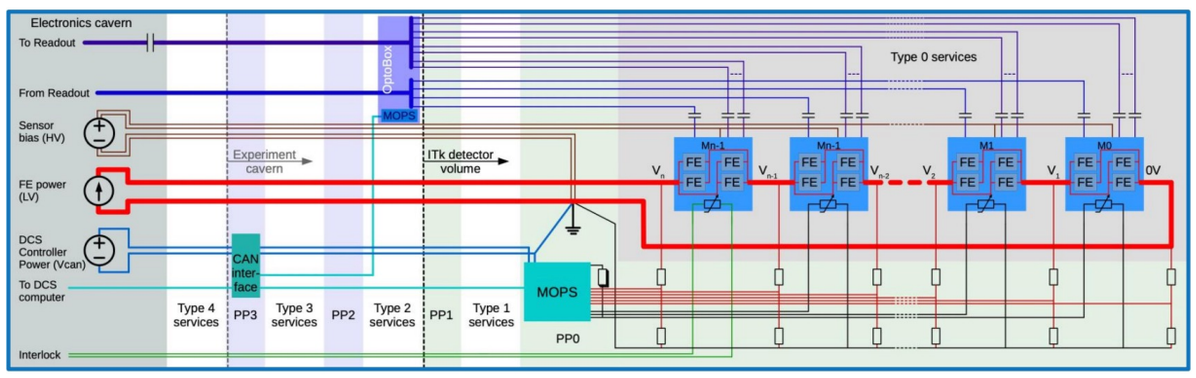


Fig. 3: Serial powering and services scheme for ITk Pixel quad modules. Front-end ASICs within a quad module are powered in parallel and serial powering chains of quad modules are constructed with up to 13 modules

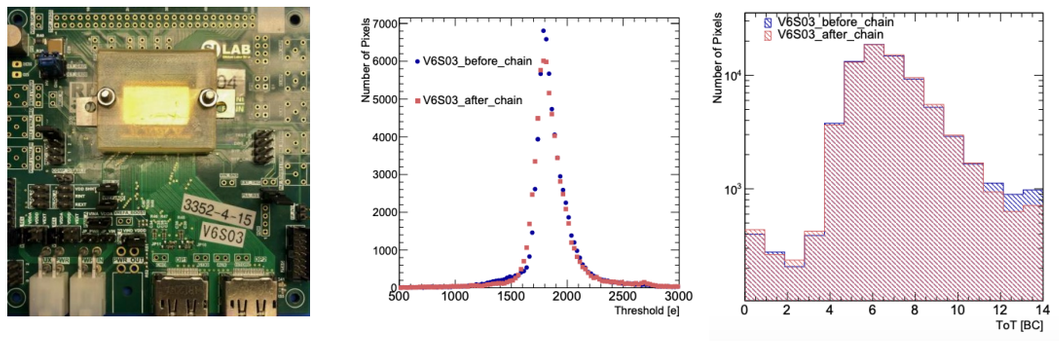
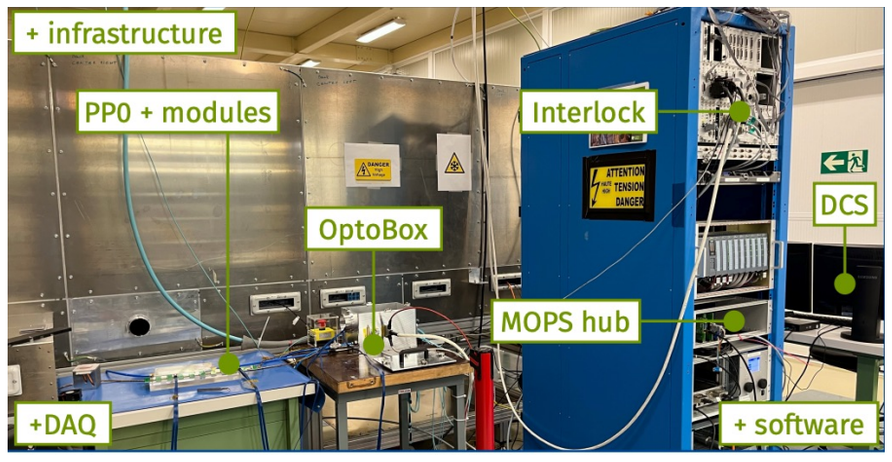


Fig. 4: (Centre, right) Results from a serial powering chain constructed using 16 irradiated single chip (left) RD53A[c] modules. No discernable difference between serial and non-serial powered modules is observed[d]

Pixel demonstrators and infrastructure for testing



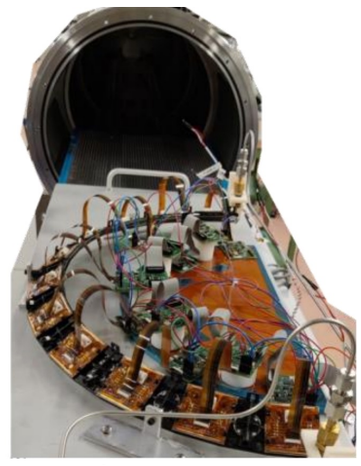


Fig. 5: (Left) The outer barrel demonstrator test stand at SR1 in CERN. (Right) An inclined ring loaded with heater modules and services for thermal tests.

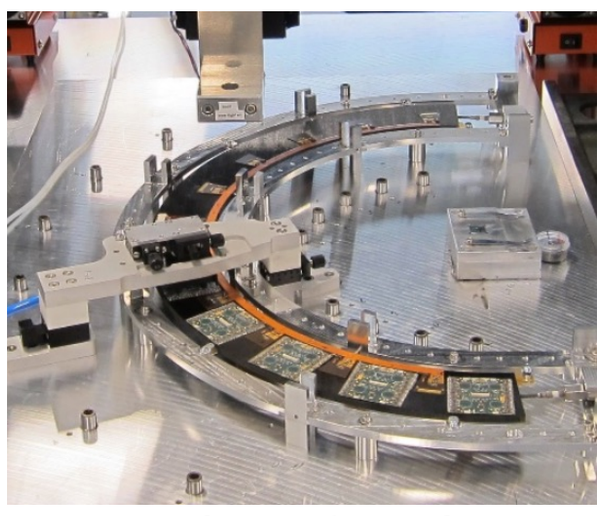
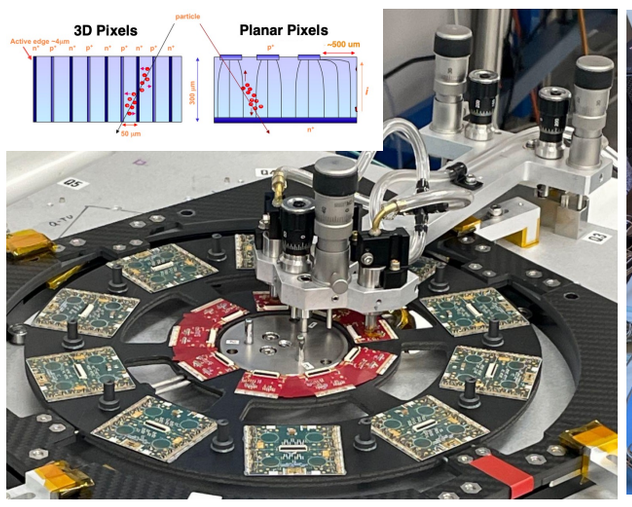


Fig. 6: (Left) Loading of RD53A pixel quad modules onto an end cap 'half ring' local support at RAL (UK). (Right) The outer endcap test stand with Lukasz CO2 cooling plant in Liverpool (UK).



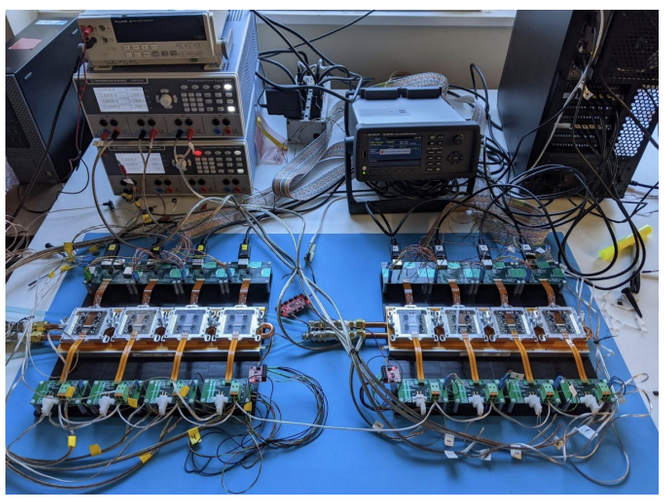
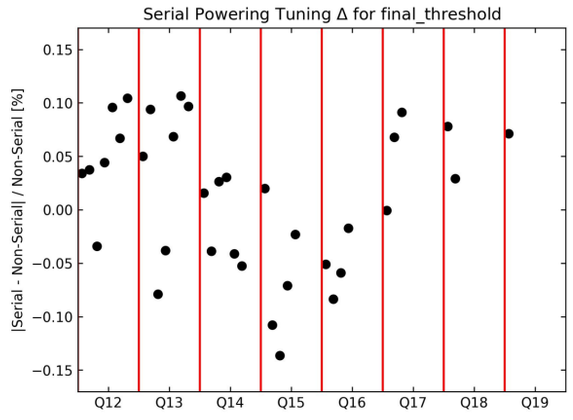


Fig. 7: (Left) Loading of RD53A pixel quad modules and RD53A triplet modules with 3D sensors (red PCB) onto a 'coupled ring' local support structure for the Inner System at SLAC (USA). (Right) 8 ITkPix[e] v1.1 quad modules in a serial powering test stand at Berkeley (USA).

Fig. 8: Readout of the 8 ITkPix v1.1 quad modules (Fig. 7) is carried out using YARR[f] with / without serial powering. No significant difference is observed at the minimum tuned threshold of 1000e-



Bibliography and acknowledgements

[a] Pseudorapidity (η) describes the angle of a particle relative to the beam axis
[b] Pile-up (μ) is the average number of particle interactions per bunch crossing
[c] RD53A readout chip manual: https://cds.cern.ch/record/2287593
[d] Further results here: https://cds.cern.ch/record/2808444
[e] RD53B (ITkPix) readout chip manual: https://cds.cern.ch/record/2665301
[f] Yet Another Rapid Readout: https://yarr.web.cern.ch/yarr/

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