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Data Pre-Processing with High-Level-Syntehsis and Dataflow Programming using HLS C++ Dataflow Template Library

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The readout of detectors with FPGAs is a common practice. Traditionally, this is done using a hardware description language such as VHDL, Verilog, or System Verilog. Data is preprocessed, filtered, and passed to high-performance computing clusters for the next processing steps. Many experiments require a continuous, trigger-less data stream, which significantly increases the algorithmic requirements.
In this work we show how to implement the increasingly complex algorithms using methods of dataflow programming and methods of Modern HLS C++ Template Programming. The focus is also on resource consumption, which must remain below an acceptable limit compared to a pure VHDL implementation. Additional design goals are fast and shorter development time, easy maintenance, the ability to adapt algorithms to changing needs, and high throughput to handle continuous data streams. We present the concept of a dataflow template library that can be used to realize the above design goals. The template library allows an algorithm to be represented as a data flow graph. It is designed in such a way that the maximum possible data throughput can be implemented with an initiation interval of 1. The locality of the algorithm is instantiated by local streaming buffers. It is shown how these buffers are implemented in such a way that a nearly balanced graph is obtained.

Collaboration

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