The DAQ and clock distribution system of CMS MIP Timing Detector

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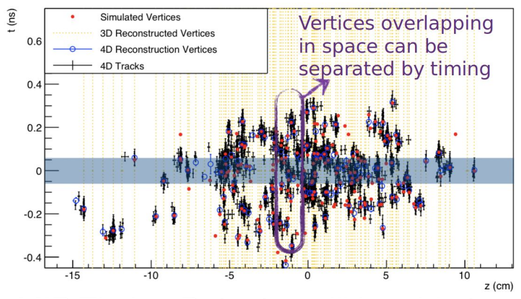
MIP Timing Detector

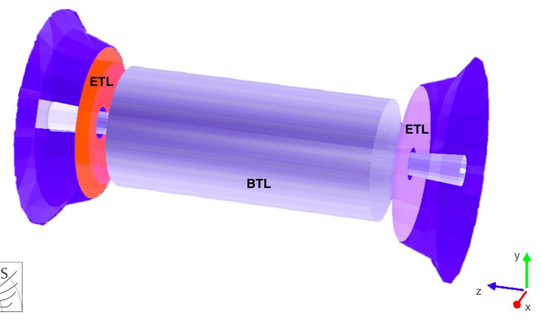


With increasing luminosity, **pileup** *(unwanted extra collisions)* and noise levels will grow as well.

Pileup early run2: ~30, **HL-LHC: ~140-200**.

BTL: LYSO crystals and SiPM

ETL: LGAD sensors



➔ MIP Timing Detector will be able to measure precisely the **production time** of minimum ionizing particles (MIP) ⇒ adding a **new dimension** for disentangling pileup.

➔ Significant addition to the HL-LHC program:

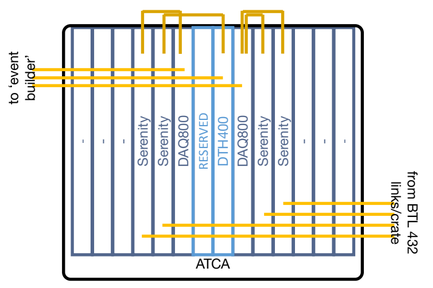
- Recover Run-2 vertex purity with 4D tracking
- Unique potential for Long Lived Particle searches
- Unique flavour physics in Heavy Ion collisions through particle ID

➔ The detector consists of **two parts**: barrel (BTL), thin cylindrical layer between tracker and ECAL, and endcap (ETL), two-disk system between tracker and HGCAL.

➔ MIP sensitivity with **about 30 ps time resolution at HL-LHC start and about 60 ps at 3000 fb-1.**

Infrastructure

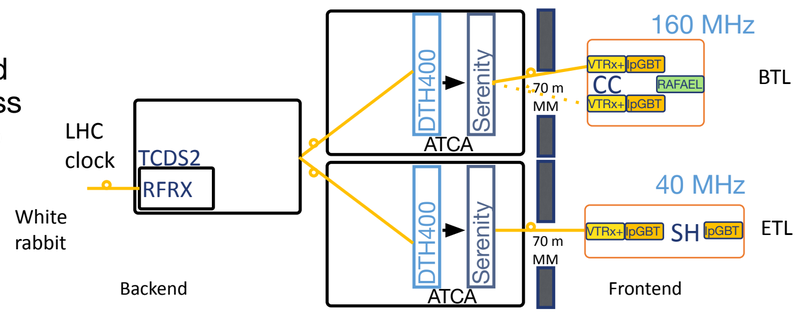
A common data acquisition (DAQ) system will collect data from readout chips, reconstruct timing information, and send data to the event builder.



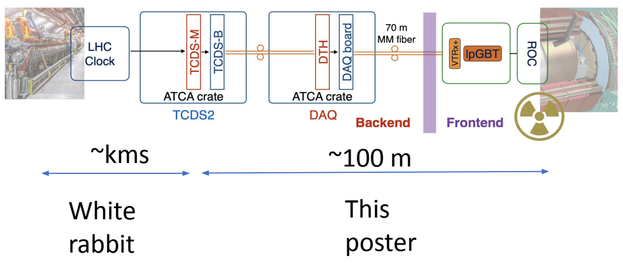
The MTD DAQ system is built around the state-of-the-art ATCA-form-factor Serenity board with two high speed FPGAs.

The **clock distribution** should provide a stable clock with less than **15ps RMS jitter** (1 Hz to sampling frequency).

Bidirectional DAQ links are used to distribute the embedded clock.

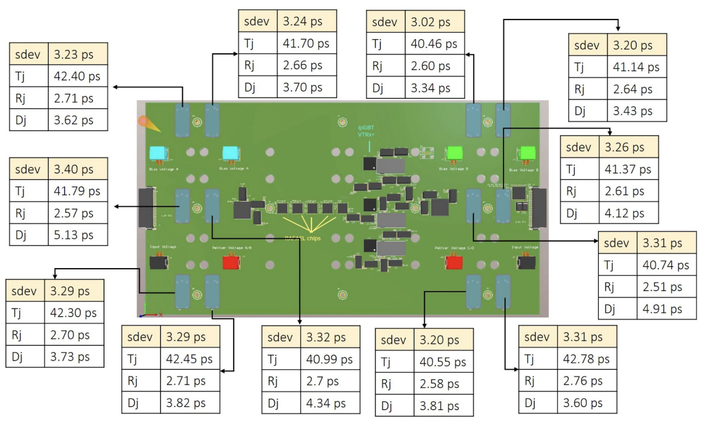


Clock Distribution



The precision clock is synchronized to the LHC bunch frequency (40MHz) and is received by the subsystem and transmitted to the detector via high-speed data links.

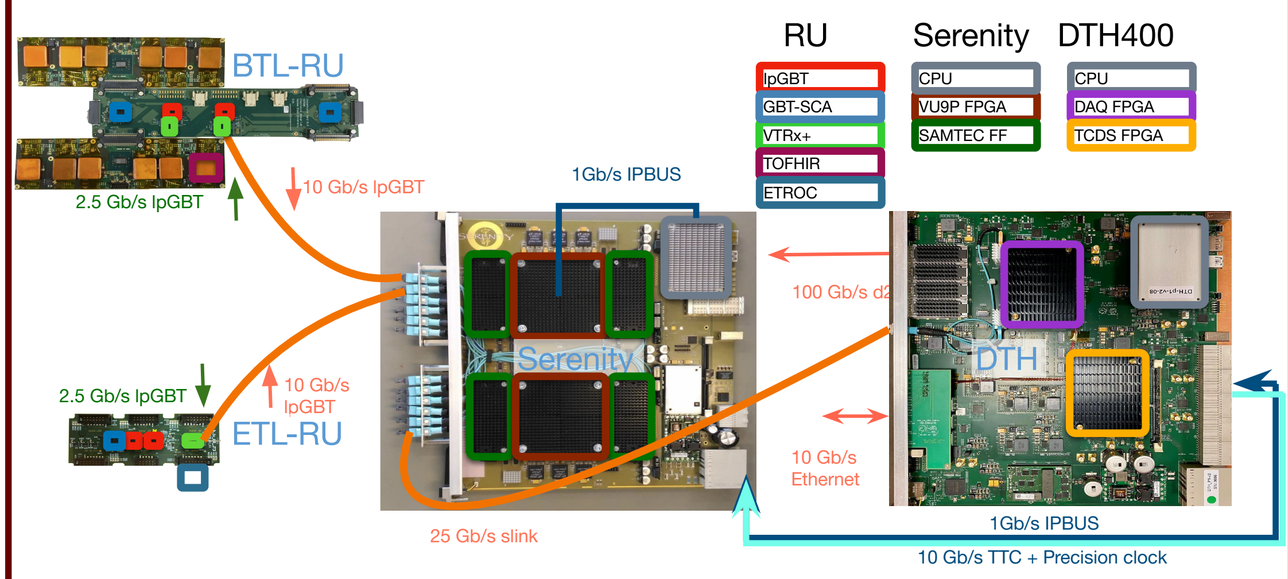
3.2 ps RMS jitter achieved with for clock distribution measurements (BTL)



Clock distribution measurements for different FEB (Front End Boards) with BTL Concentrator Card

Components of the DAQ chain

In the final system the Serenity board will hold 2 high speed, high capacity Xilinx VU9P FPGAs enabling real time reconstruction of the timing information.
BTL Readout Unit (RU) includes Concentrator Card.

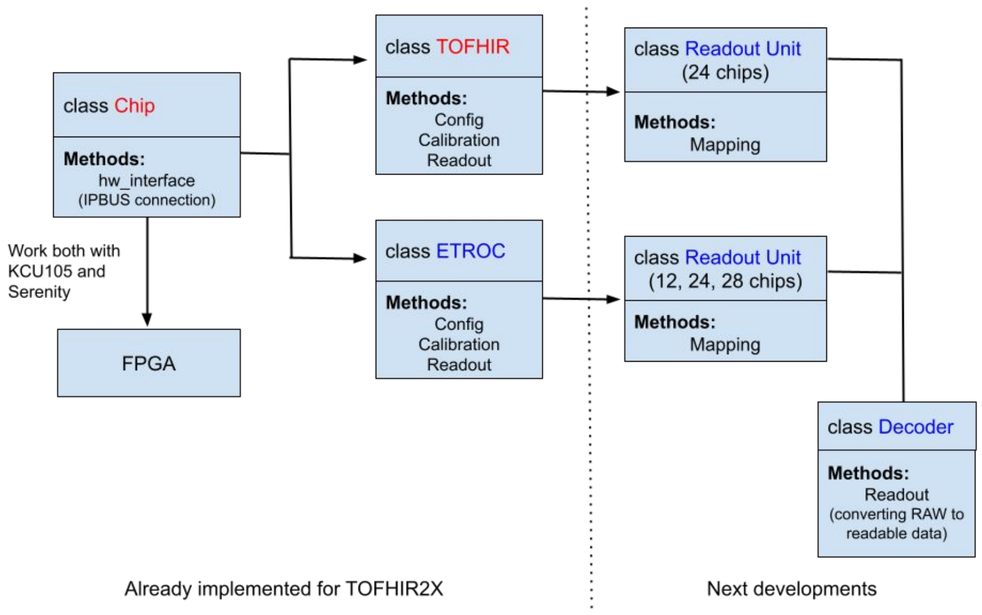


Software Developments

➔ Versatile framework for MTD DAQ is being developed (can be used both for BTL and ETL).

➔ The initialization, configuration and readout chain has been implemented and tested with the test stand using TOFHIR readout ASIC (BTL).

➔ On top of this framework a web based GUI is developed to be used with the local DAQ.



System Tests

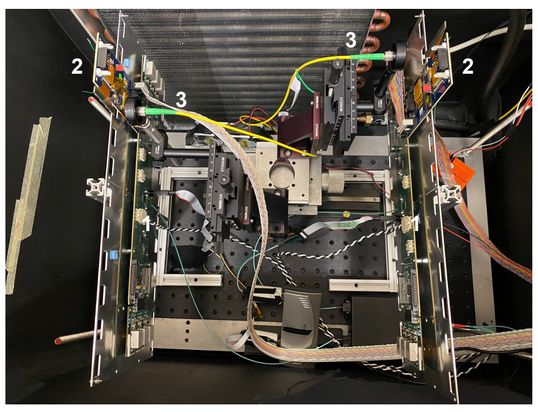
Test setup consists of:

DAQ system

1 - Concentrator Card v1

2 - FE board with 2 TOFHIR ASICs

3 - Lasers



➔ The laser is shined on the naked SiPMs or crystals delayed by a constant phase difference (10 ps RMS) wrt to the TDC reference clock.

➔ The optical fibers are split into two to provide a synchronized signals for two channels.

➔ An example of a GUI window with reconstructed timing resolution achieved during one of the system tests with TOFHIR ASIC.

➔ Results are well within the expectations - no degradation in timing due to embedded clock distribution is observed.

➔ Larger scale tests will be performed with a slice of detector.