Front End, Trigger and Data Management
Poster Review

Martin Grossmann (PSI, Switzerland), Lodovico Ratti (UniPV and INFN, Italy)

15th Pisa Meeting on Advanced Detectors
La Biodola, Isola d'Elba, May 22-28, 2022

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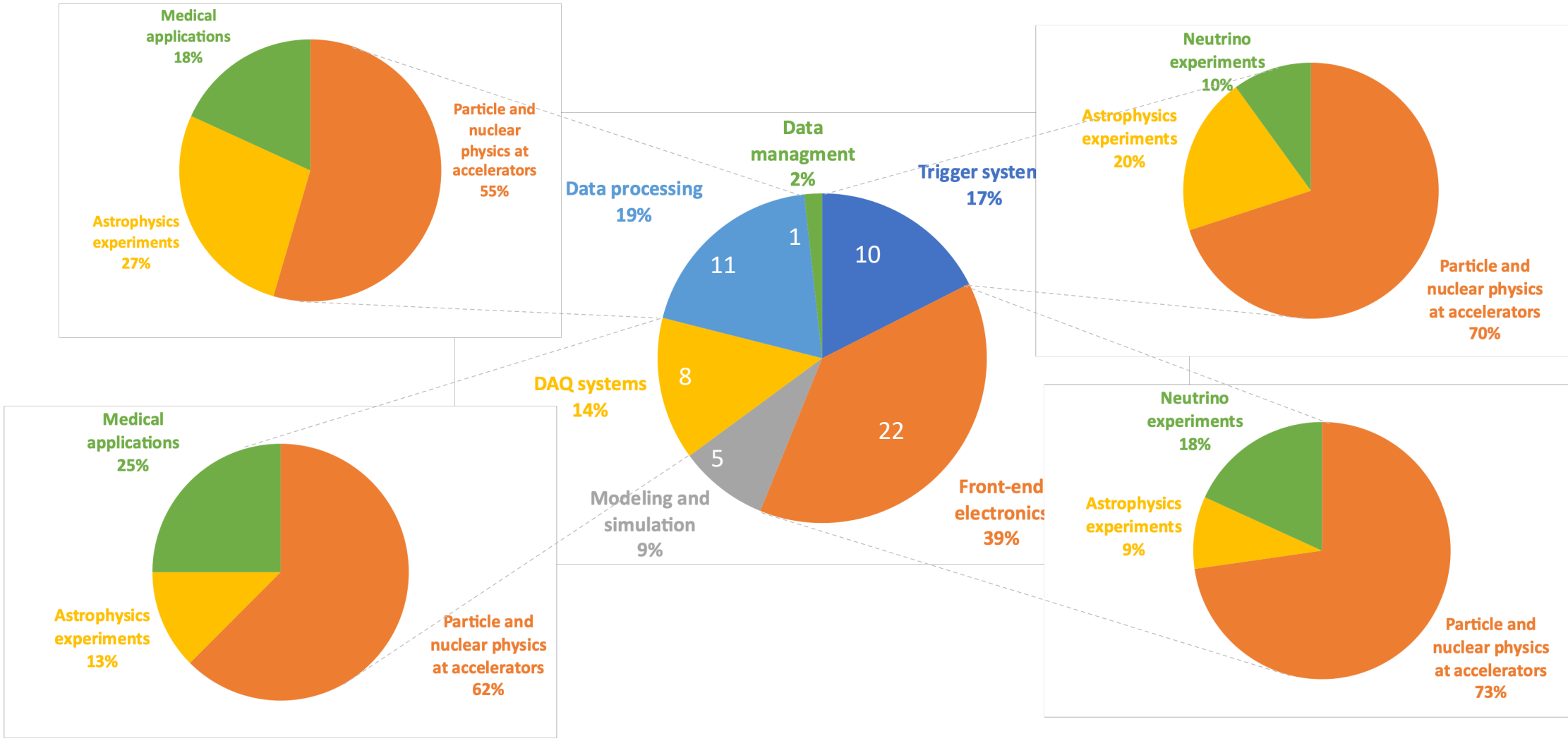

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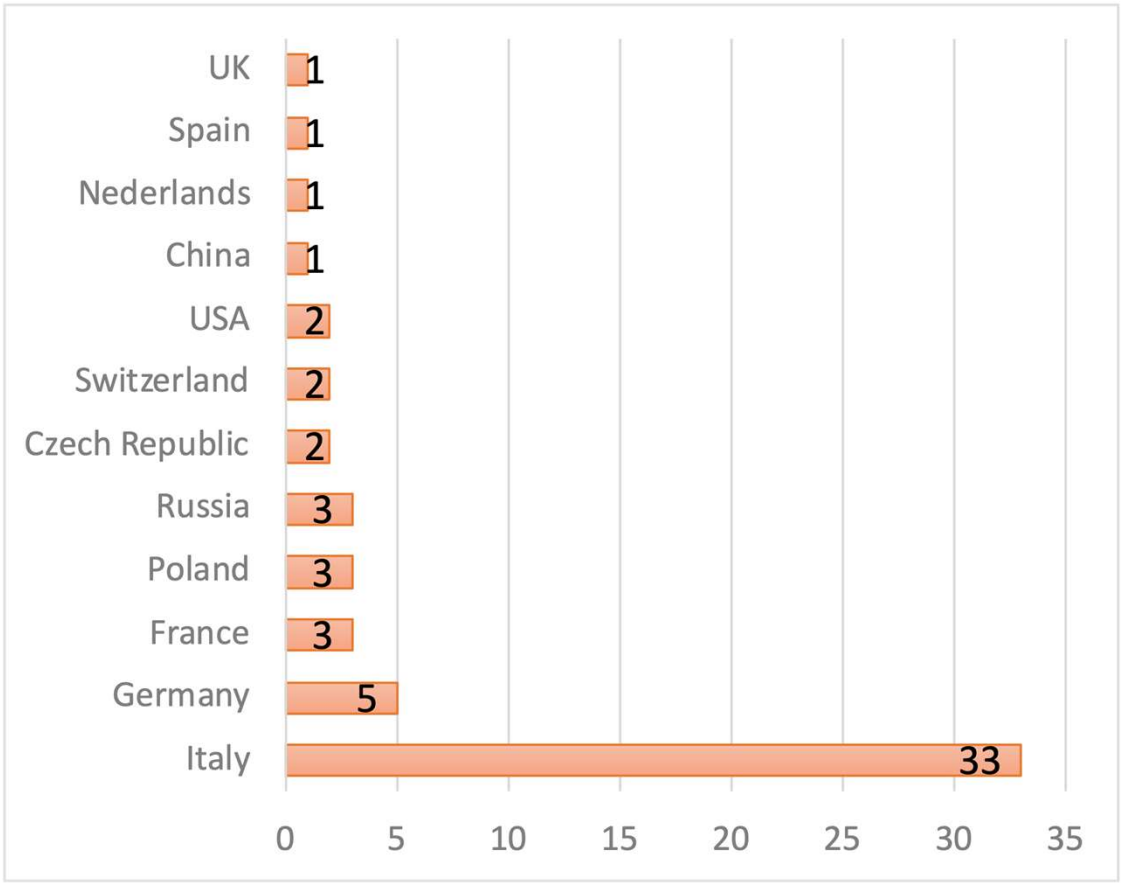

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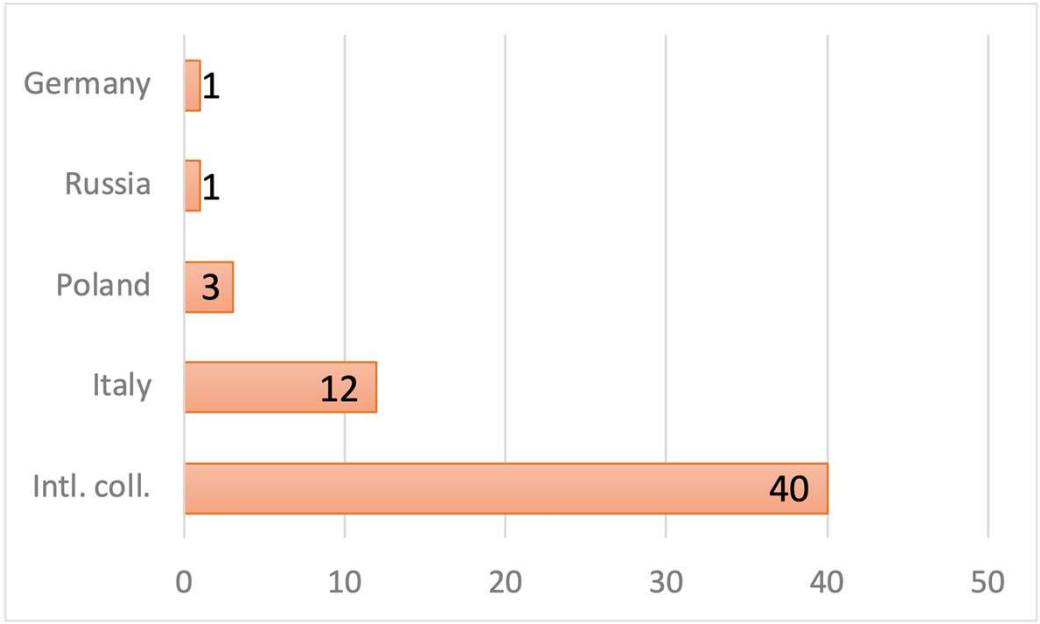


15th Pisa Meeting on Advanced Detectors

Front End Electronics Module Design for the Schwarzschild-Couder Telescope (SCT) Camera

C. Aramo, E. Bissaldi, M. Bitossi[1], L. Di Venere, F. Giordano, F. Licciulli, S. Incardona, S. Loporchio, G. Marsella, F. R. Pantaleo, R. Paoletti and G. Tripodo on behalf the SCT collaboration

1National Institute for Nuclear Physics (INFN Pisa Section) – Italy; email: massimiliano.bitossi@pi.infn.it

FEEM summary

Architecture

Distributed over two submodules: Primary (PRIM) and Auxiliary (AUX) Modules due to:

- Isolate Digital/power areas from analogue part
- Long path for analogue trace => isolated from possible sources of noise
- Encased into a metal casing for protection and for attaching to the SIPMs

Very compact form factor due to SCT Camera requirements: 274 mm x 46 mm for each submodule

Highly complex PCB: 14 layers, blind and buried vias
64 analogue channels (32+32 CHs)

T5TEA chip for triggering task

TARGET-C chip :1 GSa/s, 10 bits effective

Handles preamplifier (SMART chip) for SiPM

Prototype main goals:

- Demonstrate the performances of new FEEM: noise, distortion, reliability etc.
- Preparing the next production of the FEEMs

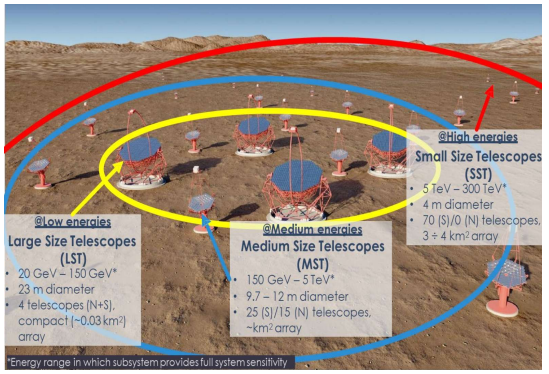
Conclusion

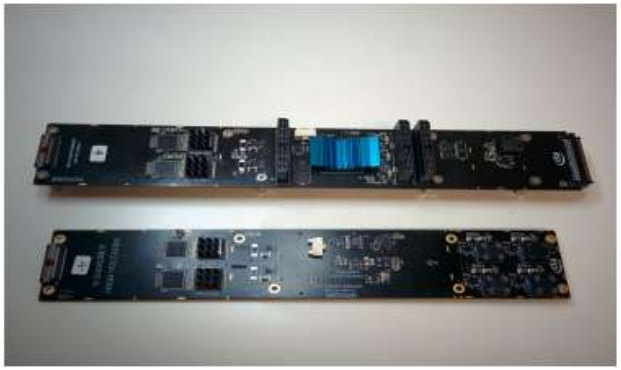
First prototypes available and their will be test in summer 2022

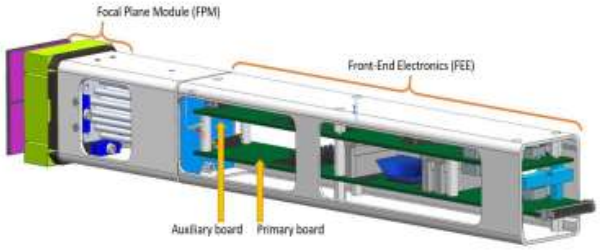
At the end of august 2022 result on the prototype will be issued

Beginning of autumn 2022 first bunch of FEEMS

End of 2022 full production (200 FEEMs)will be expected to be delivered

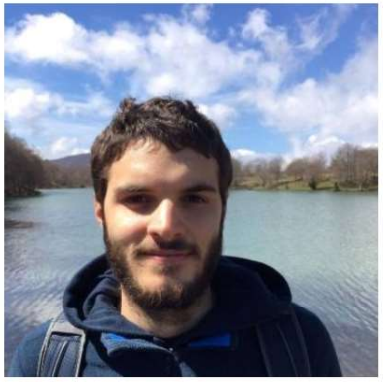






Quality control tests on the new front-end electronics for the Schwarzschild-Couder Telescope

C.Aramo(1), E.Bissaldi(2,3), M.Bitossi(4), Mario Buscemi (5,6), L.Di Venere(2,3), F.Giordano(2,3), S.Incardona (5,6), F.Licciulli(2), S.Loporchio(2), G.Marsella(5,6), F.R.Pantaleo(2,3), R.Paoletti(7,8), **G.Tripodo**(5,6).



An experimental setup has been devised to test about 750 SMART, which will be used to equip the full camera of the prototype SCT. Each SMART was tested for proper operation in response to a laser pulse. In this contribution we present a detailed scheme of the test bench and the first results obtained on the quality control measurements.

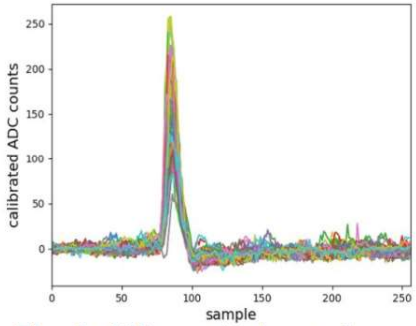


Fig. 1: *100 acquired waveforms.*

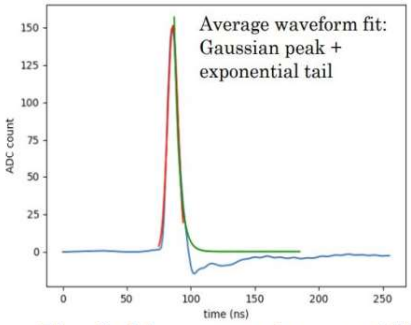


Fig. 2: *Mean waveform and fits.*

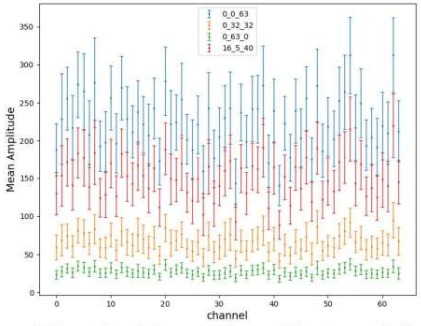


Fig. 3: *Mean Amplitude of the mean waveform for 4 different configurations.*

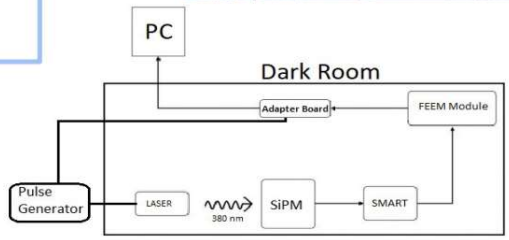


Fig. 4: *Test bench used for the tests.*

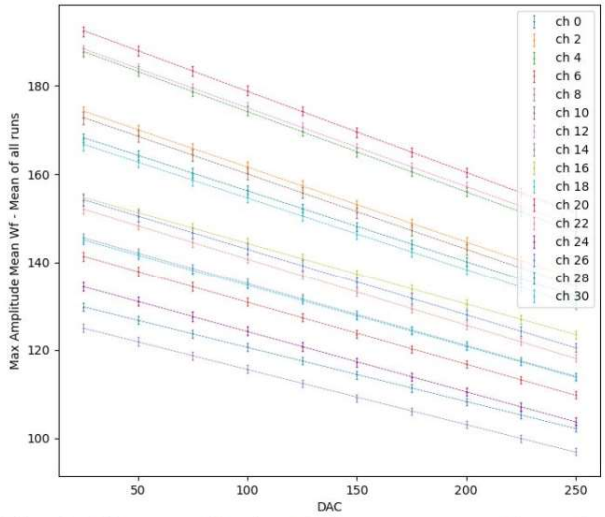


Fig. 5: *Max amplitude of the mean waveform for different SiPM bias (DAC).*

Summary:

- **SMART:** SiPM Multichannel ASIC for high Resolutions cherenkov Telescope.
- Test bench for SMART;
- Quality control test;
- Results analysis.

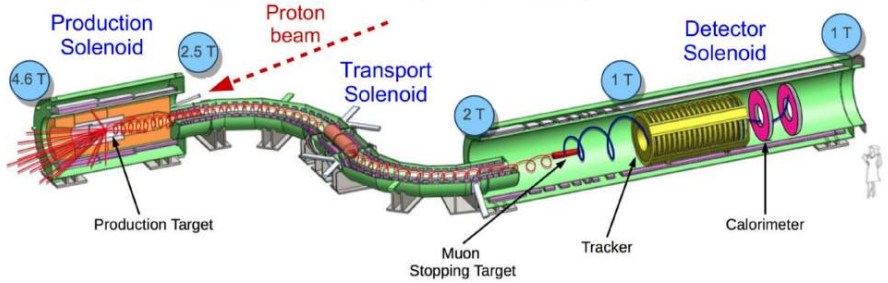
Status of the TDAQ and slow control systems of the Mu2e experiment at Fermilab - Summary

A.Gioiosa - INFN

The Mu2e experiment at Fermilab

$$R_{\mu e} = \frac{\mu^- + A(Z,N) \rightarrow e^- + A(Z,N)}{\mu^- + A(Z,N) \rightarrow \nu_\mu + A(Z-1,N)}$$

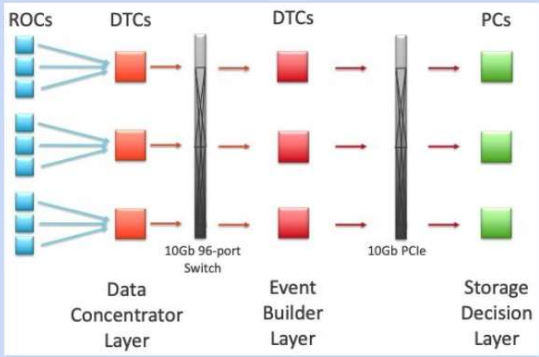
The signal we are looking for is a delayed monoenergetic electron with an energy of just under 105 MeV (muon mass)



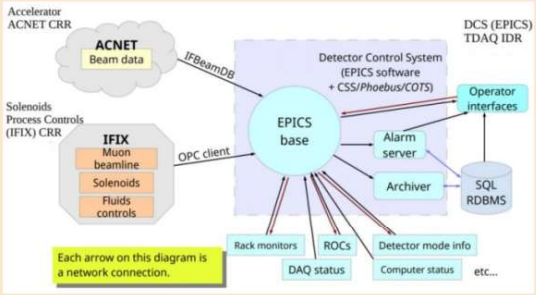
The Mu2e's Trigger and Data Acquisition System (TDAQ)

The TDAQ uses *otsdaq* as solution https://otsdaq.fnal.gov

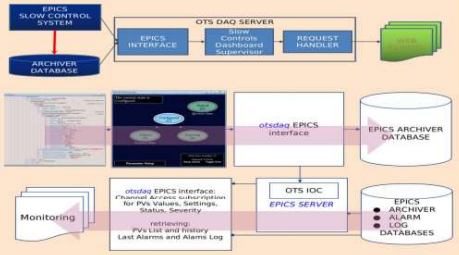
- 396 Read-Out Controllers (ROCs)
- 69 Data Transfer Controllers (DTCs)
- 800 threads on 40 nodes for HLTrigger → ~5 ms x event
- ~40 GB/s data read out to storage decision layer
- ~280 MB/s written to disk



The Detector Control System (DCS)



Experimental Physics and Industrial Control System (EPICS) has been chosen for DCS implementation



otsdaq allows the user to monitor or interact with their own DAQ hardware and all other devices managed by EPICS

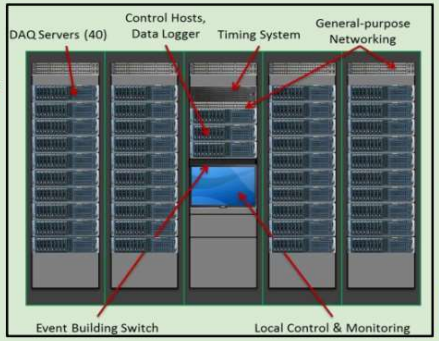
TDAQ and DCS installation in the Mu2e building

Last two year vertical and horizontal slice tests

- Characterization of synchronization and jitter
- Testing of DTC-ROC interface
- Trigger benchmarking

The installation plans

The racks, cabling, networking and controls are installed first, followed by the DAQ servers



What is now ready in the DAQ room

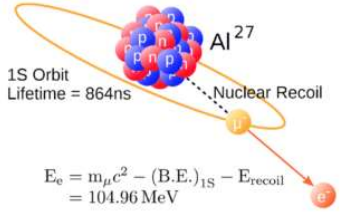
General-Purpose Network; 12 DTCs nodes

Mu2e Event Display Development

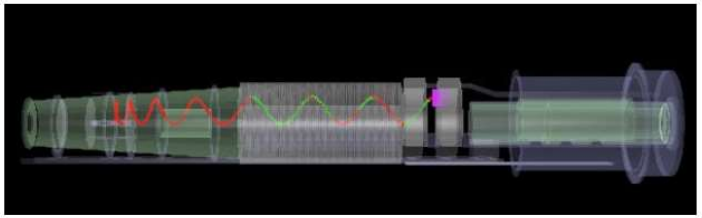
Using TEve and Eve-7

N. Chithirasreemadam, S. Middleton (Caltech), S. Donati
INFN, Pisa and University of Pisa

- The Mu2e experiment will search for the CLFV neutrinoless coherent conversion of muon to electron, in the field of an Al nucleus.
- It will examine ~ 10^{18} stopped muons in 3 years of running with an expected single-event sensitivity of ~ 3×10^{-17}.
- The expected signal is a monochromatic electron with an energy about 105 MeV. If observed, it would be a clear evidence for BSM physics.

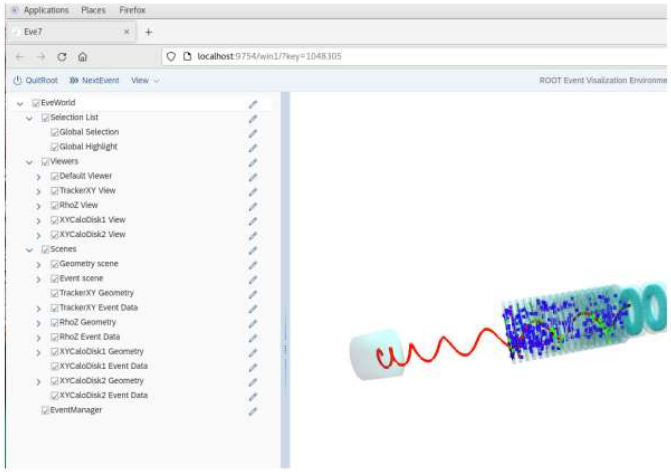


- A custom made display with GUI has been developed specifically for Mu2e using TEve and an online version is being developed using Eve-7, both ROOT based 3-D event visualisation frameworks.
- They are crucial for monitoring and debugging during live data taking, assisting in Offline analysis as well as for public outreach.



Conversion electron 3-D Event Display,
Red : MC truth track, Green : Reconstructed track

- For the 3D visualisation, a GDML file containing the Mu2e geometry is created in Mu2e Offline and directly imported to TEve.
- TEve maintains access to the raw art file making it convenient to go between the raw and reconstructed data within the display browser. It has event selection and navigation tabs.
- Reconstructed data like the tracks, hits and clusters can be displayed within the detector geometries upon GUI request.
- True Monte Carlo trajectory of particles traversing the muon beam line can be displayed in all the solenoid regions of Mu2e giving a complete illustration of the experiment.
- Tracks are coloured according to their particle identification and users get to select which trajectories to be displayed. This is a useful feature to distinguish the conversion electron signal track from the background trajectories.
- Reconstructed tracks are refined using a Kalman filter. The resulting tracks can be displayed alongside truth information, allowing visualisation of the track resolution.
- The user can remove/add data based on energy deposited in a detector or arrival time.
- Most of the above mentioned features have been migrated to the online event display as well, which allows remote access for live data taking and for multiple users to interact with the display simultaneously .



Online display with an event containing the conversion electron and other background hits

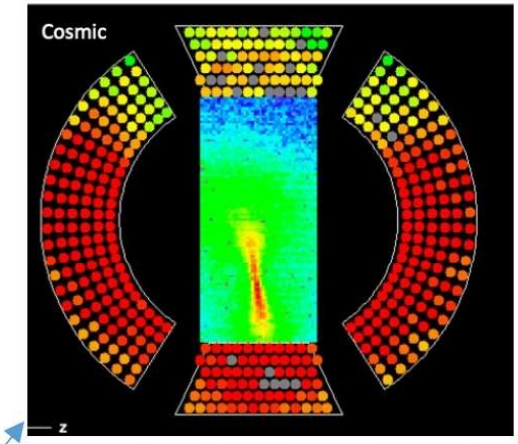
Design of the WaveDAQ System

Stefan Ritt, PSI

- **DAQ system** developed for the **MEG II** experiment
- **Custom crate** system with **Gigabit** readout, shelf management and advanced global **triggering**

#95 Marco Francesconi: "MEG II trigger"

- **9000** Channels **5 GSPS** / 12 bit
- Integrated **high voltage** system for SiPMs
- Successfully deployed in MEG II producing **first data**
- Interesting system for **many applications**

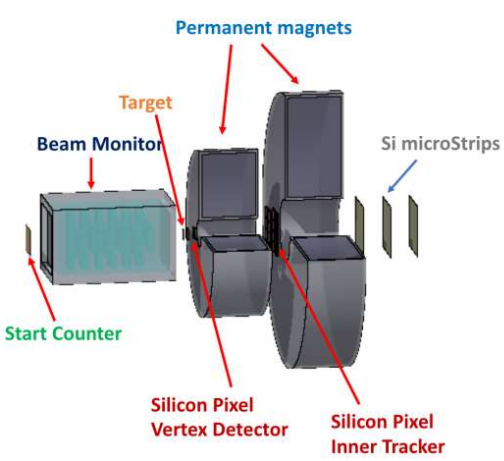


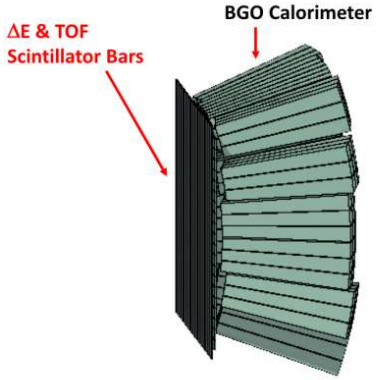
16-channel WaveDREAM board


Custom crate up to 256 channels

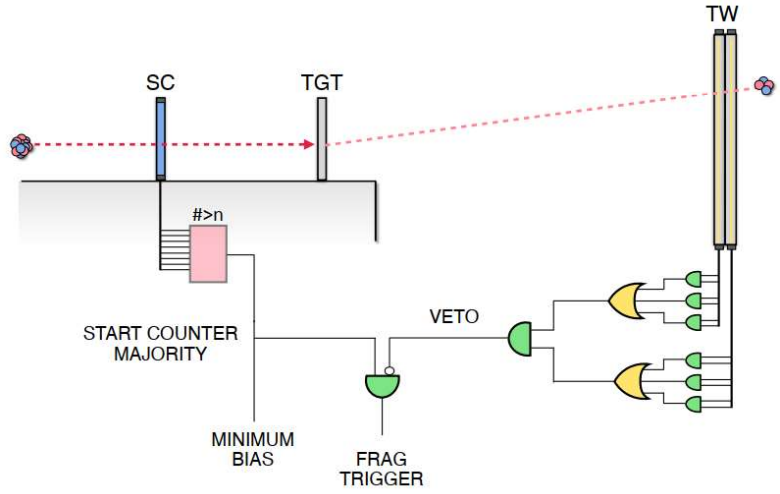

Full MEG II System 9000 channels

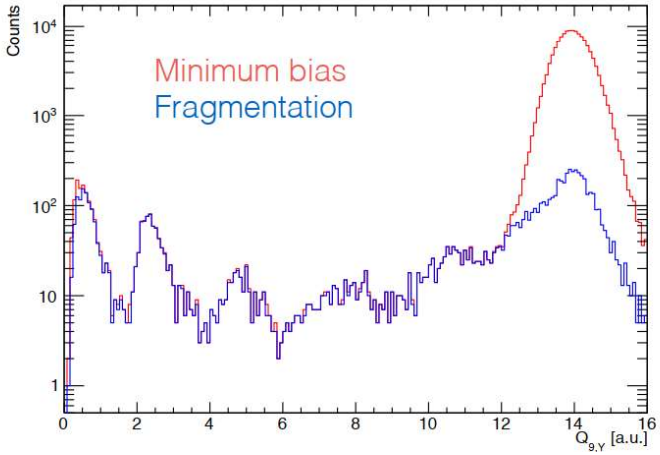
The fragmentation trigger of the FOOT experiment





- Fixed target nuclear fragmentation experiment
- Fragment selection by discriminating energy deposit on scintillation bars
- efficiency close to 100% with sample enriched by factor 6 with fragments





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Frontier Detectors for Frontier Physics
15th Pisa meeting on advanced detectors
La Biodola • Isola d'Elba • Italy
22 - 28 May, 2022

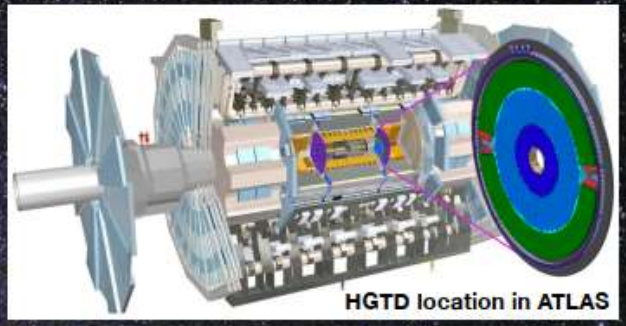
Demonstration System of the HGTD Peripheral Electronics Board (PEB) for ATLAS Phase II Upgrade

Liangliang Han, on behalf of the ATLAS-HGTD Collaboration
Nanjing University

Demonstration System of the HGTD Peripheral Electronics Board (PEB) for ATLAS Phase II Upgrade

In order to mitigate the pileup effects caused by the increasing instantaneous luminosity of proton-proton collisions at HL-LHC, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade.

There will be several types of Peripheral Electronics Boards (PEB), which will be installed in the peripheral regions of the HGTD.

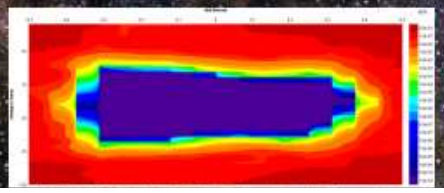

HGTD location in ATLAS

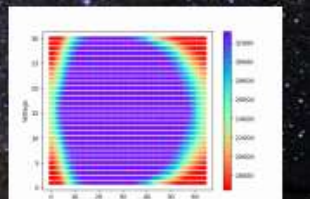

Test system setup

Prior to the PEB prototype, we developed the PEB demonstration system to verify many concerns in advance, such as versatile links, PCB manufacturing techniques, mechanical parameters, key chips, DAQ system, and etc.

The demonstration system consists of :
A set of hardwares, dedicated firmware and lpGBT configuration toolkit

We have tested the system. Basic functions are successfully implemented. And versatile links (uplink @10.24Gbps and downlink@2.56Gbps) are successfully established as well. BERT can be achieved less than 10^-14.





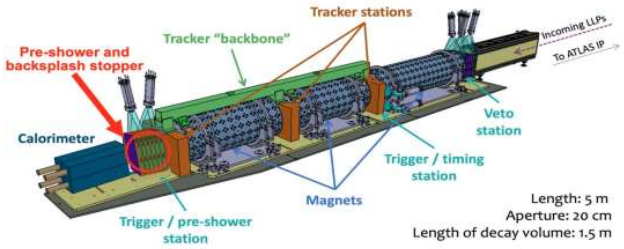
Development and simulation of a new preshower detector for the FASER experiment at the LHC

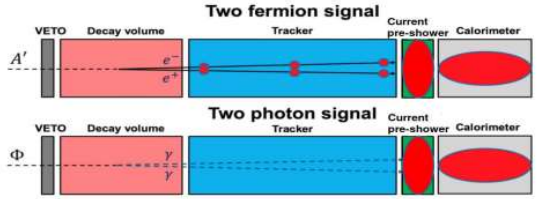
15th Pisa Meeting on Advanced Detectors

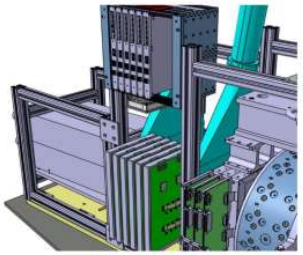
Rafaella Eleni Kotitsa (rafaella.eleni.kotitsa@cern.ch) on behalf of FASER Collaboration

UNIVERSITÉ DE GENÈVE

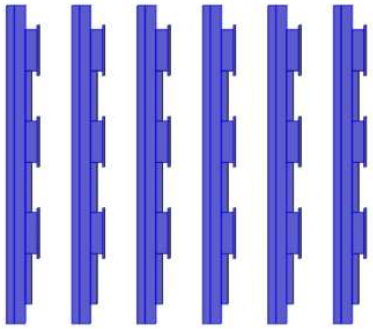
FASER is a new experiment that will operate at Run 3 at the Large Hadron Collider and it is located 480 m away from ATLAS. It is designed to search for Long Lived Particles (LLPs), that will decay at zero angle inside the detector. The new preshower detector of the FASER experiment will enable the detection of long lived particles that decay in two photons. As a result the signal that the new preshower targets to measure, is produced by two photons with energies up to TeV scale and separation 200 μm. For this reason a high granularity preshower detector is needed. This new preshower detector that will do all this, will consists from 6 layers of monolithic silicon pixel detectors attached to six tungsten layers and it will operate during 2024.

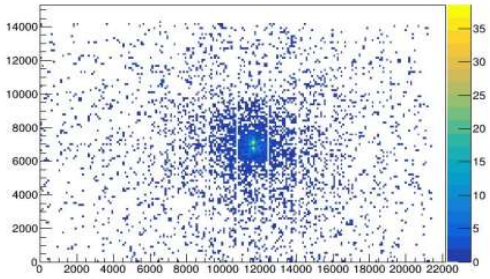


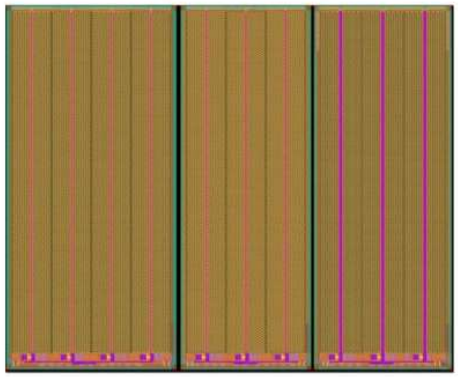


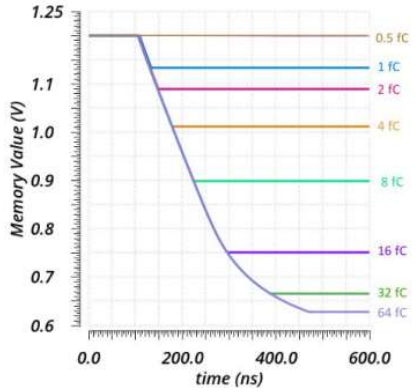


For this new preshower a monolithic ASIC in 130 nm SiGe BiCMOS technology is being developed, in collaboration between CERN, University of Geneva and KIT. The monolithic ASIC will measure the charge by means of analog memories integrated in pixel. Analog multiplexers and flash ADCs are used to read out the entire matrix in few tens of μs, while the fast amplifiers based on SiGe HBTs will provide the time of arrival of the shower core with 200 ps time resolution.
The pre-production run of the ASIC with three alternative layouts of the readout scheme is presently under test.

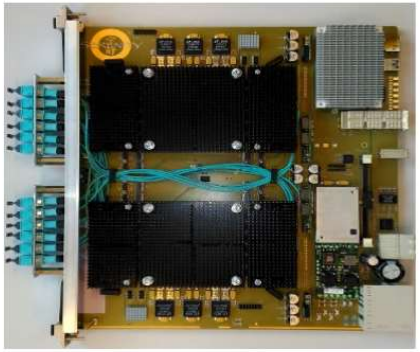






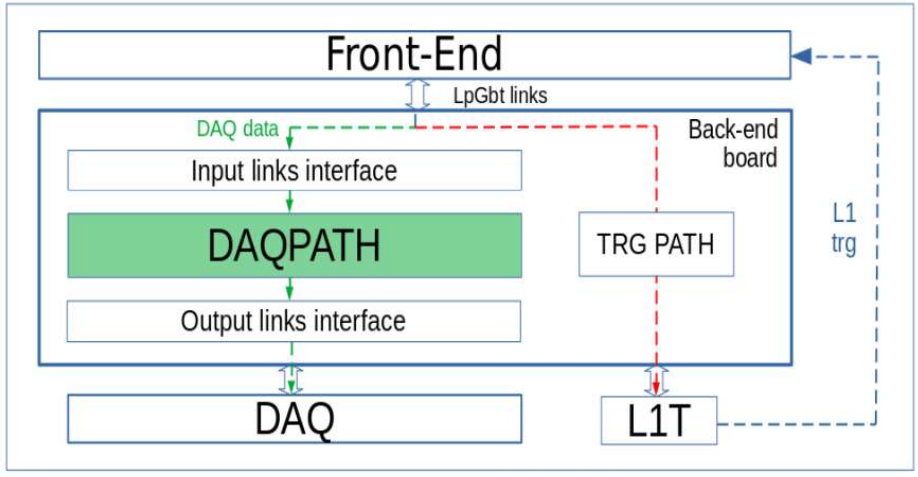


The DAQPATH readout system of the Serenity boards for the CMS Phase-II Upgrade



- Serenity boards are ATCA custom boards used in the readout of the CMS detectors in the High Luminosity LHC upgrade. Each board can handle up to 144 optical input links (up to 25Gb/s each) and supports up to two high-performance FPGAs.
- Detector-facing Serenity board is required to aggregate raw events (FE data) received from the detector on every L1 accept and route this event fragment to the central DAQ system.

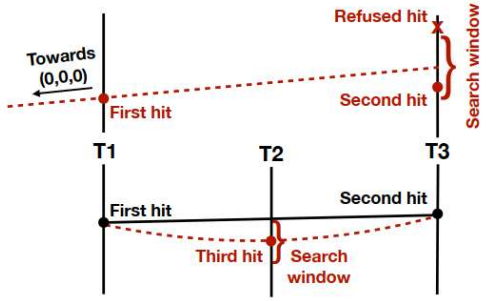
- The DAQPATH firmware goal is to collect and merge DAQ data packets and to manage their transmission to the DAQ system over output optical 25Gb/s links.
- The DAQPATH system has a modular and parametric structure: each DAQPATH module feeds one output link with data from a programmable number of input channels.
- First version (v.1.0) validated with hardware tests on Serenity boards at CERN. This version will be available soon as a tool-kit for users in the EMP official repository.

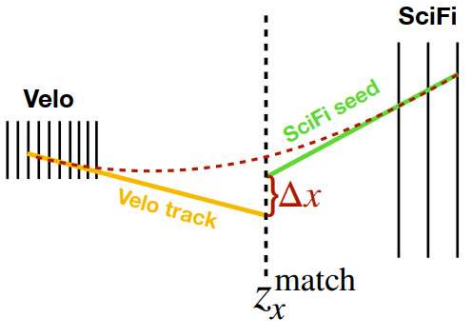


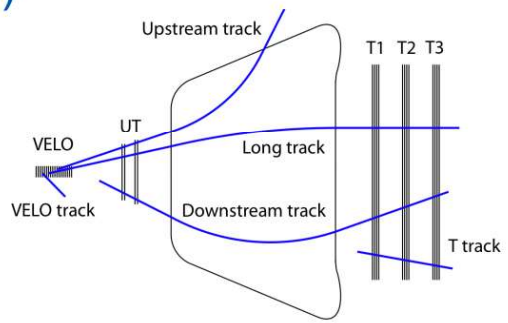
Guido Magazzù, Paolo Prosperi - INFN Sezione di Pisa - 15th Pisa Meeting on Advanced Detectors - Edition 2022

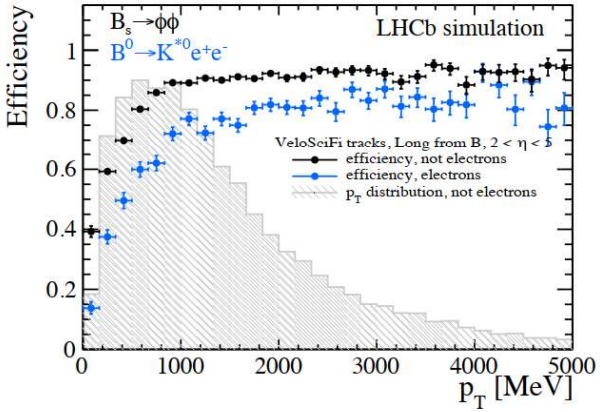
Standalone track-reconstruction on GPUs in LHCb

- New fully software-based LHCb trigger system for Run 3 with HLT1 on GPUs
- Entire new set of tracking detectors (Velo, UT, SciFi) to operate at higher luminosity
- Standalone track-reconstruction for Velo & SciFi followed by a VeloSciFi track matching for long track reconstruction
- Other track types (downstream and T tracks) can be used for extending LHCb's LLP programme
- Total tracking efficiencies for (high-p) long tracks up to 83% (92%) at a ghost rate of 9% (5%)
- Throughput:~170kHz on NVIDIA RTX A5000 card that is used in Run 3 data taking









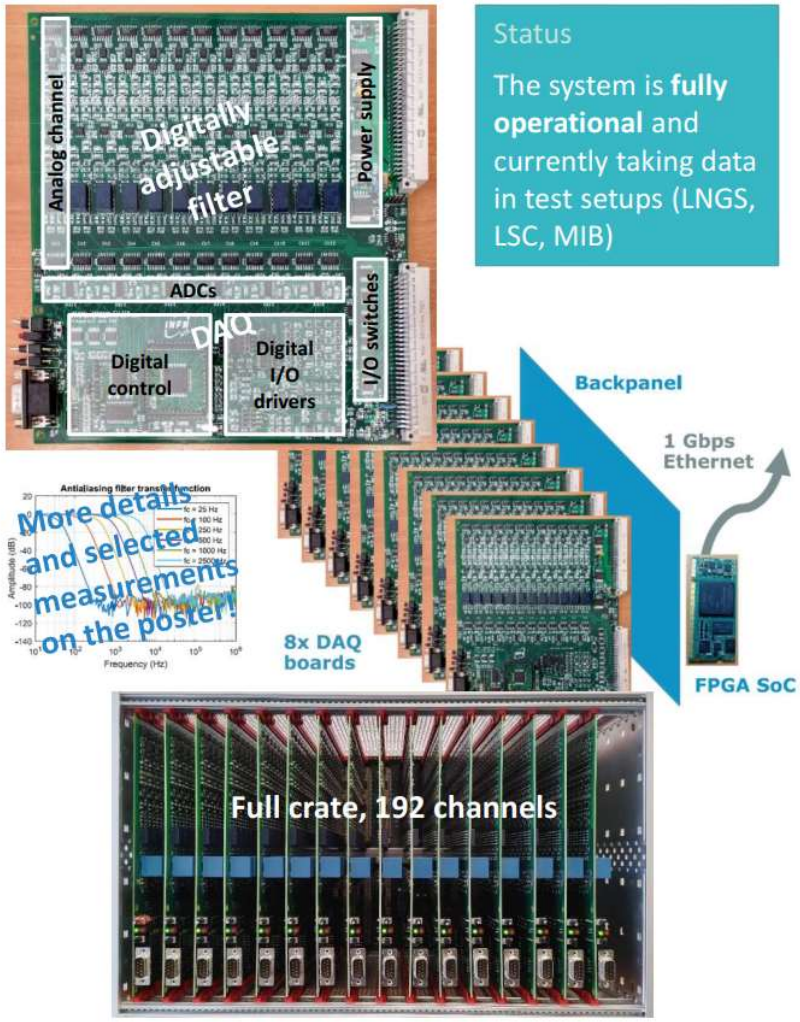
High resolution filtering and digitization system for cryogenic bolometric detectors – P. Carniti, C. Gotti, G. Pessina – Milano Bicocca

Physics case

- Experiments adopting arrays of bolometric cryogenic detectors for the search of 0νββ (like CUORE) will be upgraded with **particle identification** capabilities to reduce background sources and increase their sensitivity
- α vs β/γ discrimination can be performed using **scintillating crystals** due to the lower light yield of α particles
- Light-to-phonon detectors are much **faster** than macro-bolometers (>100 Hz vs 10 Hz) and require lower noise and higher bandwidth readout

The new high-resolution digitizer

- 12 channels, 6-pole Bessel-Thompson low pass filter
- Adjustable cut-off frequency (10-bit, 24-2500 Hz range)
- Low power consumption (250 mW/channel, full system)
- Integrated high-resolution sigma-delta 24-bit ADCs
- Sampling rate up to 25 ksps (250 ksps with 6 channels)
- Twofold operation: fully-integrated digitizer (internal ADCs) or just analog filter (with external commercial DAQ)
- Continuous data stream with FPGA SoC on the backplane through 1 Gbps Ethernet (RTP protocol over UDP)
- Slow control with Python-based ZeroMQ server



Status

The system is **fully operational** and currently taking data in test setups (LNGS, LSC, MIB)

Studies of the CBC3.1 readout ASIC for CMS 2S-modules

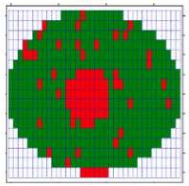
- CBC is ASIC to be used for CMS tracker upgrade 2s modules and it is currently in the production phase and wafer probing is on going.
- The performance has been proven in modules with chips from engineering run in beams and with TID and SEU tests.

Wafer probing summary

- Engineering run (2018) – 13 wafers in Lot1
  - Average Yield > 80 %, yield patterns are observed in all the wafers
- Pre-production run (2019) – 24 wafers per lot, Lot2 & Lot3
  - Average Yield > 80%, yield patterns are observed in some of the wafers
  - Memory errors and I2C register corruption were identified at **low temperature test at -30 °C**
- Production run (2021-) – 270 wafers in Lot4 – Lot19, total 500 wafers are expected
  - low T issues were studied in detail and wafer probing continues at room temperature
  - **Yields from most lots (sampled) > 75 %** with additional tests to identify low T issues, strong lot dependence in the yield and patterns

The impact of the issues found at low T test on occupancy is estimated to be < 10^{-4} compared to an expected occupancy of 1-2%.

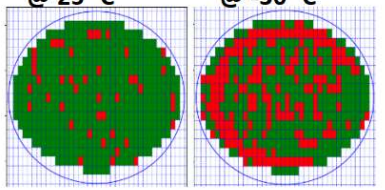
wafer (a) in Lot1



developed on a wafer probing station to study yield and performance in operation conditions of the CMS experiment. *Not for wafer probing for production wafers due to the technical difficulty.*

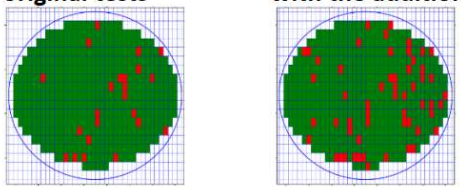
wafer (b) in Lot3

@ 25 °C **@ -30 °C**



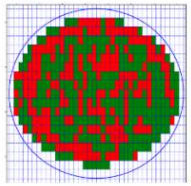
wafer (c) in Lot9 @ 25 °C

original tests **with the additional tests**



wafer (b) in Lot3

@ 25 °C with the additional tests



Wafer-level testing of the readout chip of the CMS Inner Tracker for HL-LHC

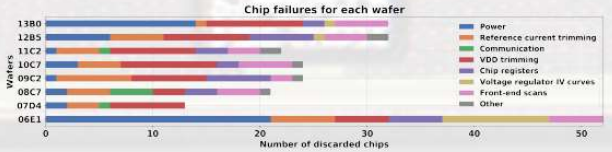
Nazar Bartosik[2] Lino Demaria[2] Michael Grippo[1,2] Fabio Luongo[1,2]

[1]University of Turin [2]INFN Turin

- The **CMS Inner Tracker**, in the **High-Luminosity LHC** (HL-LHC) phase, will be instrumented with more than 10^4 **CMS Readout Chips (CROCs)**
  - 65 nm readout chips developed by the joint ATLAS-CMS RD53 collaboration
  - Very complex chips with several design novelties (e.g., serial powering)
- A batch of 20 wafers of prototype CROC chips (CROCv1) has been produced
  - 8 of these wafers have recently been tested by the Turin INFN section for hybridisation
- **Wafer-level testing setup** developed at INFN Turin
  - Semi-automated probe station (Cascade Microtech CM300xi)
  - Custom electronics, such as the probe card and an auxiliary card for PC control
  - Python wafer-level testing software (**gitlab.cern.ch/croc_testing/croc_wlt**)
- **Wafer-level testing results**
  - Average yield of the 8 tested wafers is **73 %**
  - Rejected chips: 220 out of 1104 (20 %) marked red and discarded. Most rejections due to **power anomalies** or **failed/marginal chip trimming**
  - Obtained important **calibration** and **characterisation** data for hundreds of chips
- **Discussion**
  - Commissioned wafer-level testing setup at INFN Turn to test wafers from the first batch of CROC prototypes
  - Collected calibration and characterisation data useful for prototype modules production and testing

***Left figure**: wafer-level testing hardware; **right figure**: CROCv1 wafer (300 mm ⌀)*

Wafer maps examples



Discarded chips with non-finalised wafer-level testing cuts

Contact: michael.grippo@cern.ch

Implementation of the Cluster Counting and Timing technique on FPGA for the reduction of transferred data and stored information.

G. Chiarello[c], F. Cuna[a], A. Corvaglia[a]G.,G.Cocciolo, B. D'Anzi [d,e], M. De Liso, N. De Filippis[d,e], W. Elmetenawee[d,e], E. Gorini[a,b], F. Grancagnolo[a], A. Miccoli[a], M. Panareo[a,b], M. Primavera[a] ,G.F. Tassielli[d.e] and A. Ventura[a,b]

Abstract

Ultra-low mass and high granularity Drift Chambers fulfill the requirements of tracking systems for modern High Energy Physics experiments at future high luminosity accelerators (FCC or CEPC). The application of the Cluster Counting technique adds a valuable PID capabilities with resolutions outperforming the usual dE/dx technique. Moreover, by measuring the arrival times of each individual ionization cluster to the sense wire (Cluster Timing) and by using suitable statistical tools, it is possible to perform a bias free estimate of the impact parameter in drift chambers operated with a Helium based gas mixtures. The Cluster Counting/Timing techniques consist in isolating pulses due to different ionization clusters, therefore it is necessary to have a read-out interface capable of processing such high speed signals and to manage the low amplitude signals from the sense wires. An electronic board including a fast ADC and an FPGA for real-time processing is presented. Additionally, various algorithm implementations for peaks finding are compared.

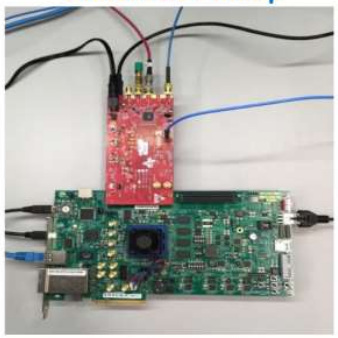
Cluster counting/timing operation

In a conventional drift chamber, only the time of the first cluster is used to estimate the track impact parameter, thus providing a biased systematic overestimate. Cluster timing technique uses statistical tools to reduce the biased estimate by exploiting the information of all clusters detected with a cluster counting/timing algorithm implemented on a FPGA. The algorithm (in VHDL/Verilg languages) identifies, in the digitized signals, in real time, the peaks due to the single ionization electrons, records their times and amplitudes and sends the data stored to an external device when a specific trigger signals occurs.Initially, to evaluate the performance of the algorithm, simulated signals through an AWG have been used and the obtained results on the number of real and false peaks found have been compared to assess whether eventual errors were due to the algorithm itself or to approximations in the VHDL implementation and successively its efficiency calculated the percentage of fake peaks versus the number of real peaks.

Solution

The solution consists in transferring, for each hit drift cell, instead of the full spectrum of the signal, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e. the amplitude and the arrival time of each peak associated with each individual ionization electron.

Hardware Setup



KIT EVAL ULTRASCALE FPGA KCU105

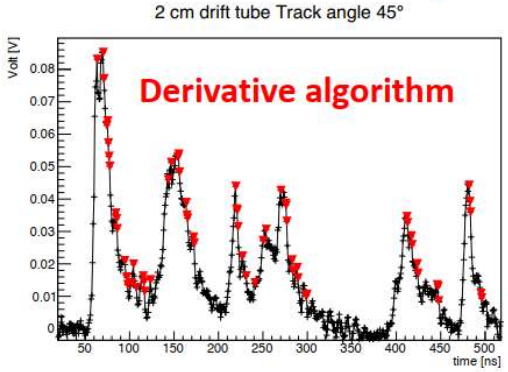
- UltraScale™ XCKU040-2FFVA1156E
- Transceiver 20 GTH
- 2 moduli SFP+ da 10Gbps

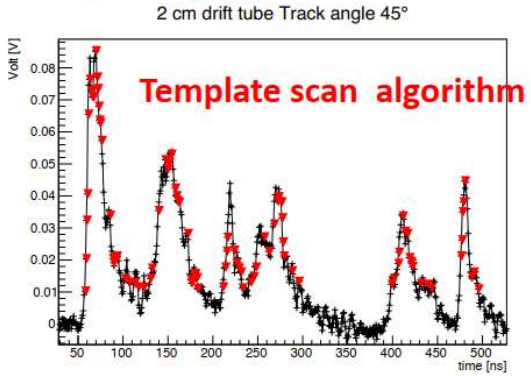
ADC32RF45EVM

- 14-bit
- Dual channel
- 3GSPS

Cluster Finder Approach

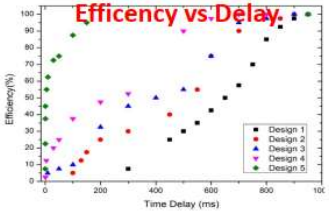
Test on several possible algorithms. A simple peak finder algorithm, based on the first and second. The red arrows indicate the peaks identified by the algorithm





Implementation of the algorithm

The CluTim algorithm (implemented on a FPGA, interfaced with a ADC), identifies in real-time the peaks corresponding to the different ionization cluster, stores each peak amplitude and time in an internal memory and sends the stored data to an external device when a specific trigger signal occurs. Such a quasi-on-line procedure results in data reduction factors of almost two orders of magnitude with respect to the raw digitized data.



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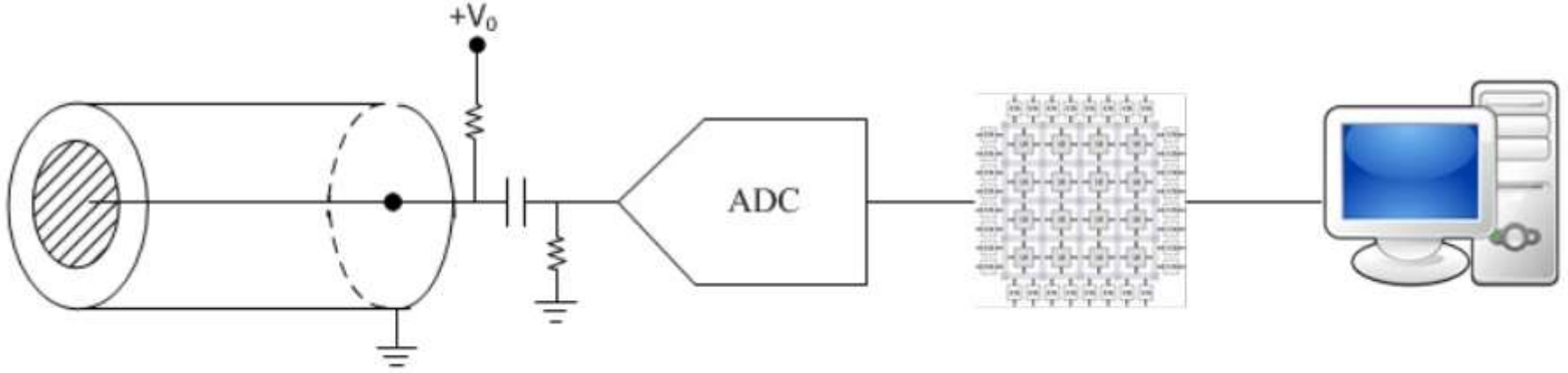

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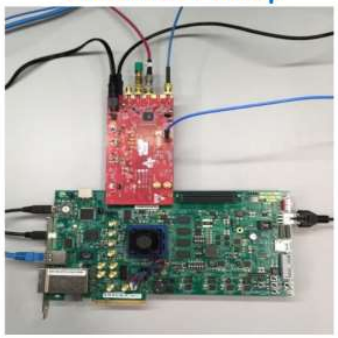

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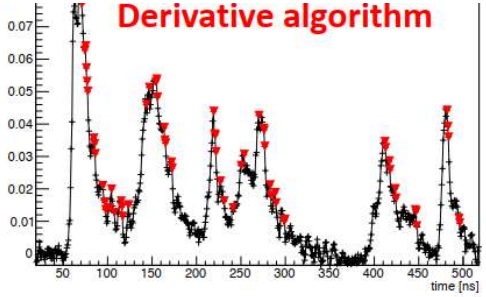

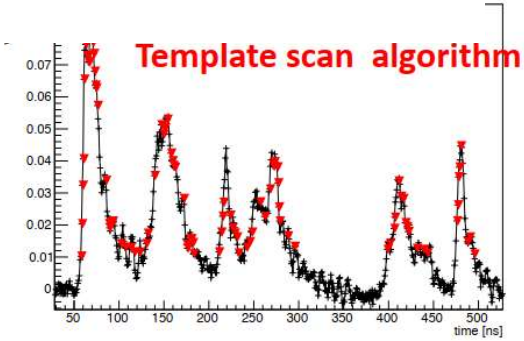

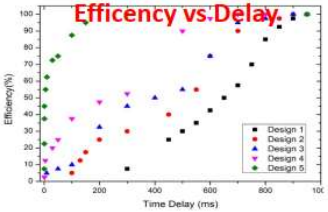

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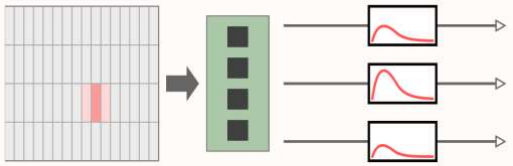
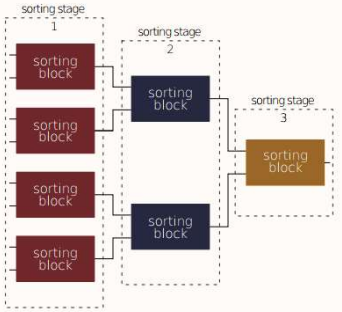
Developing a Cluster-Finding Algorithm with Vitis HLS for the CBM-TRD

David Schledt, Christoph Blume and Udo Kebschull
Goethe-Universität Frankfurt am Main

- The poster describes the implementation of the CBM-TRD data preprocessing firmware.
- The CBM experiment will have interaction rates of up to 10 MHz
  - The goal is to measure rare probes of the QCD phase diagram with unprecedented statistics
  - Raw data rates of up to 2 TB/s
  - Online event selection with 4D track reconstruction inevitable
- The CBM-TRD is one of the biggest data producers of the experiment.
  - A great candidate to reduce the raw data load in the FPGA layer to accelerate the online event selection
- The data processing is written in C++ and is implemented with Xilinx Vitis HLS.
  - HLS allows for a much quicker design cycles.
  - Functional validation can be done completely in software.
- The implemented design is fully pipelined for maximum throughput and achieves a average data reduction of 80.6%.



Schematic depiction of a detector trigger, where the center pad fulfilled the SPADIC trigger logic and the neighboring pads are read out as forced neighbor triggers.



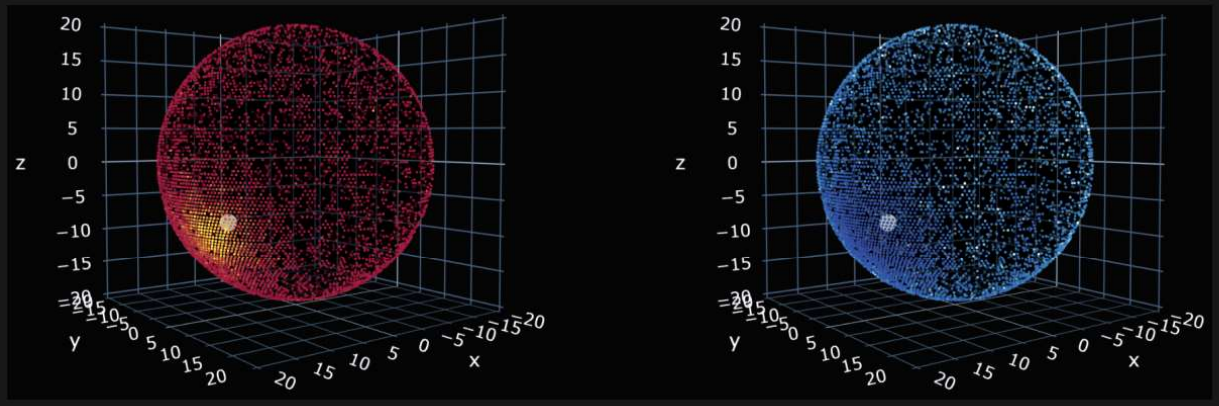
Inside the **FPGA**, the data needs to be prepared for further processing. The entire processing

Machine Learning Techniques for Energy Reconstruction in JUNO experiment

Arsenii Gavrikov, Fedor Ratnikov on behalf of the JUNO collaboration

JUNO is a multipurpose experiment located in China with a broad physical program. The primary aims of JUNO are to determine the mass ordering of neutrino and to precisely measure of three oscillation parameters.

In this work, we present machine learning methods for neutrino energy reconstruction in JUNO. We consider following methods: Boosted Decision Trees (BDT) and Fully Connected Deep Neural Network (FCDNN), trained on aggregated features, calculated using information from the whole array of large PMTs.

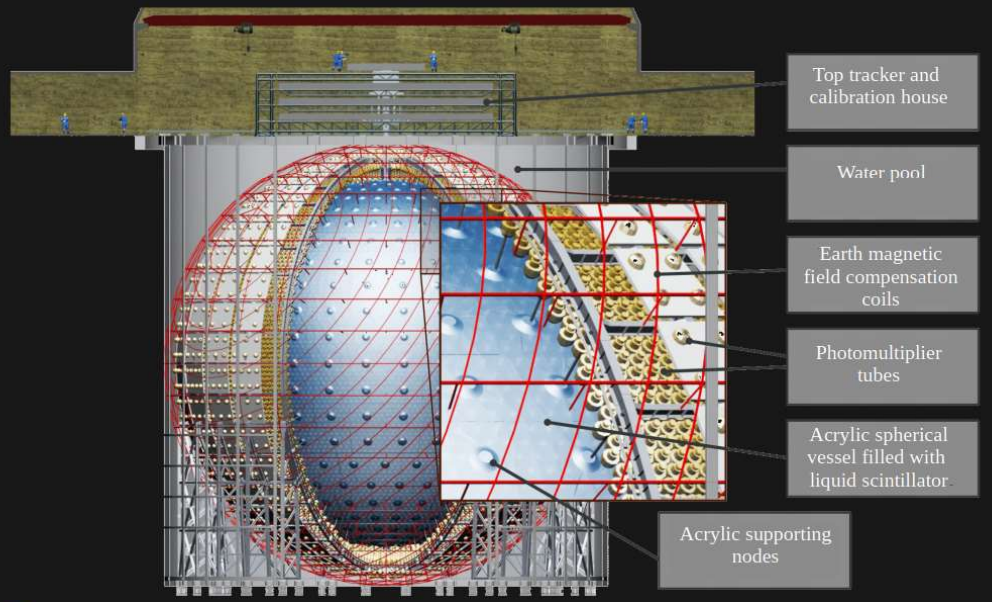


Avaliable information:

- Charge at each PMT;
- First Hit Time (FHT) at each PMT;
- PMT position.

We want to provide:

- Deposited energy Edep with a high energy resolution: 3% @ 1 MeV.



Summary:

- Designed a large set of aggregated features;
- Investigated their informational importance;
- Selected a subsets providing the same performance as the full set;
- Achieved required for the physics goals effective resolution: ã < 3%
- The models have great computation speed;
- In addition, we considered three calibration sources for the future evaluation of the models on the real data.

Francesco Gonnella (University of Birmingham) - francesco.gonnella@cern.ch

Hog (HDL on git): an easy system to handle HDL on a git-based repository

Pisa Meeting - 22-29 May 2022

RATIONALE

Coordinating firmware development among many international collaborators is becoming a very widespread problem.

Guaranteeing **firmware synthesis with Place and Route reproducibility** and assuring **traceability of binary files** is paramount.

Hog tackles these issues by exploiting advanced git features and integrating itself with HDL IDEs: Xilinx **Vivado**, Xilinx **ISE** (planAhead) or Intel **Quartus**.

The integration with these tools intends to **reduce** as much as possible **useless overhead work** for the developers.

WHAT IS HOG?

Hog is a set of **Tcl and Shell scripts** plus a suitable **methodology** to handle HDL designs in a GitLab repository.

Hog is included as **a submodule** in the HDL repository and allows developers to create the Vivado/PlanAhead/Quartus project(s) locally and synthesise/implement it or start working.

HOG ON YOUR MACHINE

- a **simple** and **effective** way to maintain HDL code on git
- **automatically integrated** into Xilinx/Intel project without additional effort
- ensure the code was **not modified** before building binary files
- ensure **traceability** of binary files (even if produced locally)
- multi-platform compatibility, working both with **Windows** and **Linux**
- compatibility and support for **IPBus**
- automatic creation of **Sigasi** project

HOG CONTINUOUS INTEGRATION ON GITLAB

- **YAML files** to run continuous integration in your **GitLab** repository
- Automatic **tag creation** for versioning
- Automatic **GitLab release** creation with and **binary files**
  - including timing
  - utilisation reports
- **Automatic changelog** in the release note **parsed from commit messages**
- Possibility to store the output binary files on EOS

A Modular Data Acquisition System for Reconstruction of Radiation Dose Spatial Distribution in Radiotherapy Treatment Planning

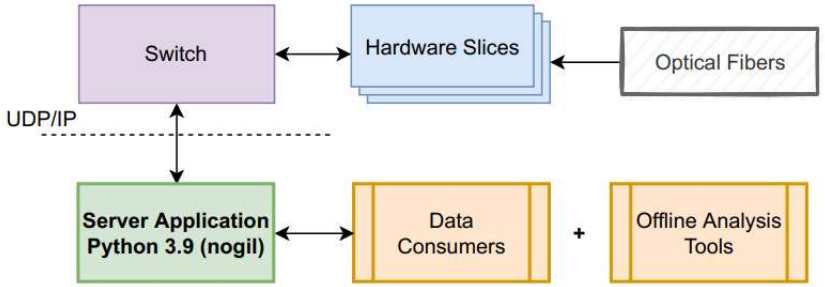
Paweł Jurgielewicz[1], Marcin Filipek[1], Tomasz Fiutowski[1], Damian Kabat[2], Kamila Kalecińska[1], Łukasz Kapłon[2], Maciej Kopeć[1], Stefan Koperny[1], Dagmara Kulig[2], Jakub Moroń[1], Gabriel Moskal[2], Antoni Ruciński[3], Piotr Wiącek[1], Tomasz Szumlak[1], and Bartosz Mindur[1]

[1]AGH University of Science and Technology, Faculty of Physics and Applied Computer Science, Krakow, Poland
[2]Department of Medical Physics, Maria Sklodowska-Curie National Research Institute of Oncology Krakow Branch, Krakow, Poland
[3]Institute of Nuclear Physics Polish Academy of Sciences, Krakow, Poland

European Funds Smart Growth
Republic of Poland
FNP Foundation for Polish Science
European Union European Regional Development Fund

Poster Summary

We present a comprehensive Data Acquisition (DAQ) system for future 3-dimensional radiation dose deposition detector dedicated for improvement of cancer-diagnosed patients' treatment planning



- The hardware is based on fine-grained scintillator cells and extendable signal processing units (64-channel each) providing simultaneous and synchronous information about number of photons and their energy
- The DAQ framework eases communication between hardware and software layers and exposes UDP/IP protocol while software manages acquistion process and broadcasts data to consumer widgets
- We show preliminary results indicating possibility of reliable energy estimation and counting photons with the presented system

dose3d.fis.agh.edu.pl
pawel.jurgielewicz@agh.edu.pl

Medical Imaging Data Analysis Using 3D Deep Learning Models Towards Improving the Individual Treatment Plans

Kamila Kalecińska[1], Tomasz Fiutowski[1], Paweł Jurgielewicz[1], Damian Kabat[2], Maciej Kopeć[1], Łukasz Kapłon[2], Stefan Koperny[1], Dagmara Kulig[2], Jakub Moroń[1], Gabriel Moskal[2], Antoni Ruciński[3], Piotr Wiącek[1], Bartosz Mindur,[1] and Tomasz Szumlak[1]

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European Funds Smart Growth
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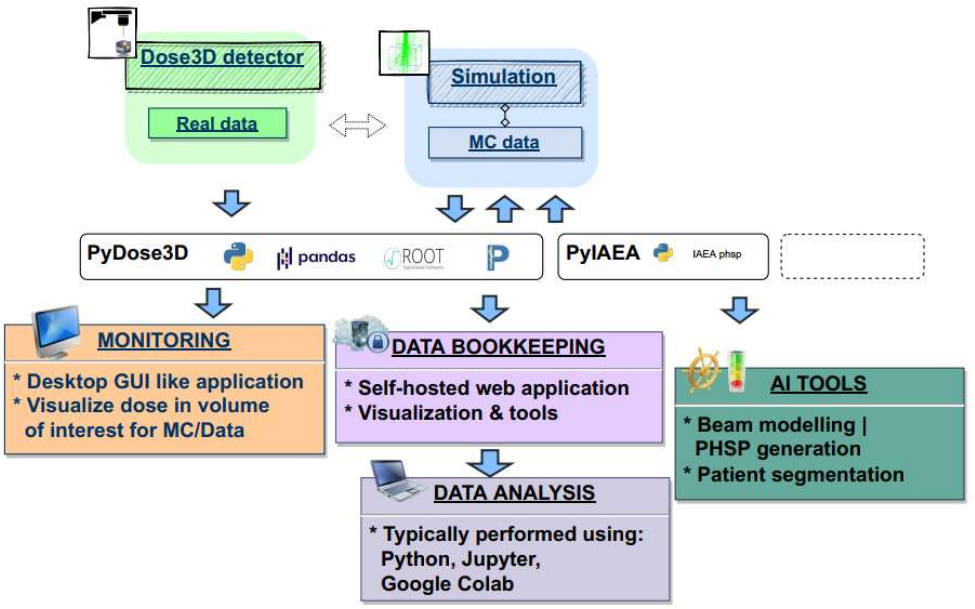
Poster Summary

- TEAM NET Dose3D Project is being supported by Machine Learning (ML) techniques in the process of building the tool for geometry delivery for 3D detector.
- Geometry for detector is in the form of a 3D Computed Tomography (CT) scan of the human body with highly precise delineation of affected area and surrounding organs.
- The process of extracting the desired object from a medical image (segmentation) is performed by automatic tool based on deep learning model.
- We presented a preliminary results of training Generative Adversarial Networks (GANs) model for data augmentation purposes
- Medical data preprocessing and model training is supported by using the most advanced technologies for healthcare: NVIDIA Clara and MONAI.



dose3d.fis.agh.edu.pl
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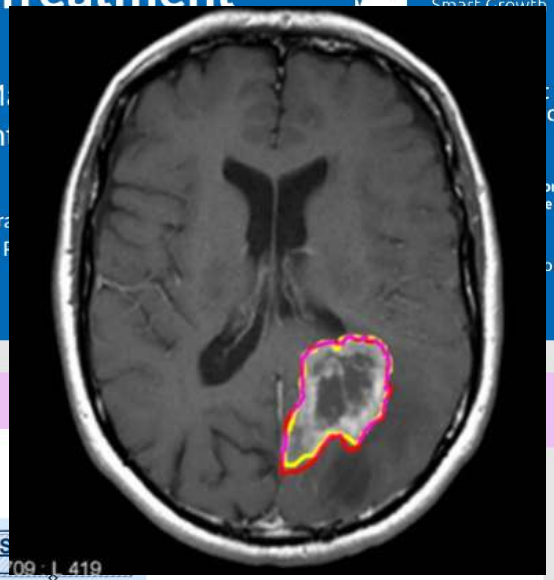
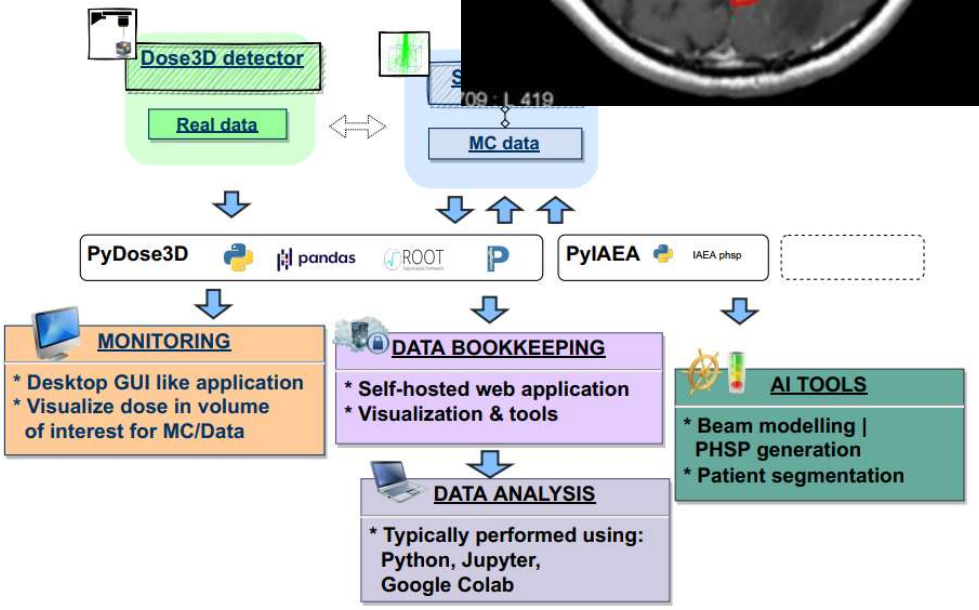
[2]Maria Sklodowska-Curie National Research Institute of Oncology Krakow Branch, Department of Medical P
[3]Polish Academy of Sciences, Institute of Nuclear Physics, Krakow, Poland



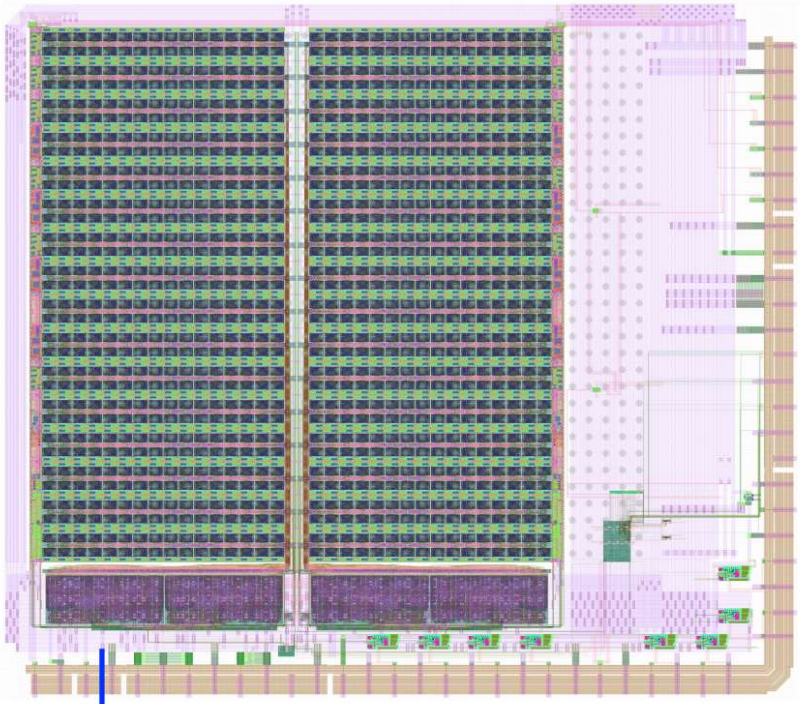
Poster Summary

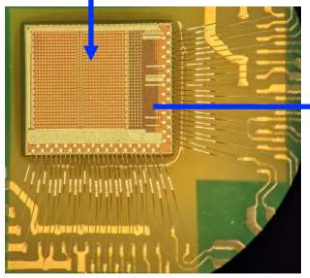
- TEAM NET Dose3D Project is being supported by Machine Learning (ML) techniques in the process of building the tool for geometry delivery for 3D detector.
- Geometry for detector is in the form of a 3D Computed Tomography (CT) scan of the human body with highly precise delineation of affected area and surrounding organs.
- The process of extracting the desired object from a medical image (segmentation) is performed by automatic tool based on deep learning model.
- We presented a preliminary results of training Generative Adversarial Networks (GANs) model for data augmentation purposes
- Medical data preprocessing and model training is supported by using the most advanced technologies for healthcare: NVIDIA Clara and MONAI.



dose3d.fis.agh.edu.pl
kamila.kalecinska@agh.edu.pl

Timespot1: an ASIC for high-resolution timing and high rates in 28-nm CMOS technology





Bonded Timespot1 ASIC

TS1-PCB 120x80 mm²

Reduced size (32x32 = 1024 pixels, total area 6 mm²),
Complete set of functionalities for pixel readout with timing
Max sustainable rate 3 MHz/pixel (1 TDC per pixel)
(1.8 x 1.8) mm² sensitive area. 50 µm pixel pitch (in y direction)
3-side abuttable matrix (xy pitch on sensor side is 55 µm)

- **640 MHz master clock**
- **Digital row: 16x2 TDC each** + Controls, Conf. registers, I²C I/F
- **Analog row (16x2 AFE each)**
- **Analog (service) column. Each contains:** 1 Band-Gap circuit, 5x Σ–Δ DACs (producing analog levels used by pixels), Programmable bias cell (for power consumption), bias replicas with source followers.
- **8x LVDS driver** (each @1.28 Gbps)

Results on timing performace (time resolution σ_{TA})

- **TDC: $\sigma_{TA} \approx 20$ ps, in average**, with a relatively wide dispersion across the channels of the ASIC (around 5 ps rms)
- TDC simulated $\sigma_{TA} < 10$ ps. Worsened timing performance and dispersion due to the master clock jitter inside the pixel matrix. More accurate clock distribution is needed.
- **AFE: $\sigma_{TA} \approx 40$ ps, in average.** However, this value is limited by the performance of the TDC, which bias the estimate of the AFE resolution towards higher values.
- Identified bug on the Offset Compensation mechanism, which prevent the setting of the discriminator threshold towards nominal low values. The intrinsic AFE performance appears below 20 ps. The bug is easily recoverable by design.
- The next version of the ASIC is in preparation

GWitchHunters

Machine Learning and citizen science to improve the performance of Gravitational Wave detectors

Massimiliano Razzano[1,2] , Francesco Di Renzo[1,2], Francesco Fidecaro[1,2], Gary Hemming[3], Stavros Katsanevas[3]

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On behalf of the REINFORCE Consortium

- Focused on **GW, Machine Learning and Citizen Science**
- **Glitch classification and characterization** in Advanced Virgo
- Auxiliary channels
- Tasks also available for Desktop and mobile devices
- Coupled to dedicated **Virgo Glitch Database** and monitoring system

- Launched @ Nov 2021,
- **>2500 registered users**
- Products input for **Machine Learning CNN pipeline**