

Contribution ID: 449

Type: Poster

The ITk interlock hardware protection system

Tuesday, 24 May 2022 09:16 (1 minute)

For the upgrade of the Large Hadron Collider (LHC) to the High-Luminosity Large Hadron Collider (HL-LHC) the ATLAS detector will install a new Inner Tracker (ITk), which consists completely of silicon detectors. Although different technologies were chosen for the inner and outer part, the major risk for all silicon detectors are heat-ups, which can cause irreparable damages. As, once the detector is installed, detector elements are not accessible for several years or even for the lifetime of the detector, such damages must be avoided by all means.

The ITk interlock system is a hardwired safety system, it acts as last line of defense and is designed to protect the sensitive detector elements against upcoming risks. Core of the interlock system is an FPGA, which houses an interlock matrix. It collects signals from interlock protected devices and distributed signals onto interlock controlled units (e.g. power supplies). Additionally, signals from external systems can be integrated. To keep the number of detector elements, which are out of operation, at a minimum, the power supplies are controlled with a high granularity. The resulting large number of channels also explains why no commercial solution was selected.

We explain the concept in detail, report about the realization of the interlock system and future plans.

Collaboration

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Session Classification: Solid State Detectors - Poster session