The ITk interlock hardware protection system
from concept to realization

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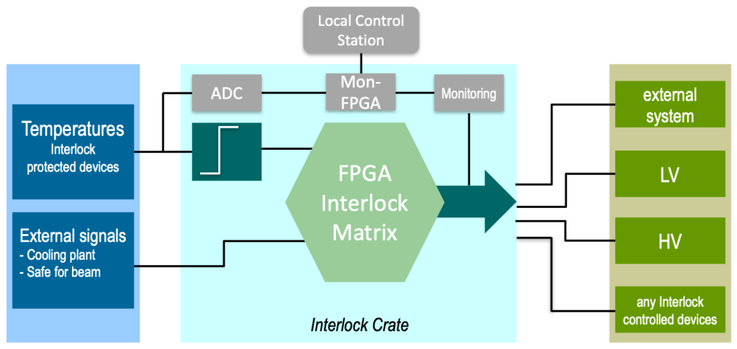
For the upgrade of the Large Hadron Collider (LHC) to the High-Luminosity Large Hadron Collider (HL-LHC) the ATLAS detector will install a new Inner Tracker (ITk), which consists completely of silicon detectors. Although different technologies were chosen for the inner and outer part, the major risk for all silicon detectors are heat-ups, which can cause irreparable damages. As, once the detector is installed, detector elements are not accessible for several years or even for the lifetime of the detector, such damages must be avoided by all means.
The ITk interlock system is a hardwired safety system, it acts as last line of defense and is designed to protect the sensitive detector elements against upcoming risks. The core of the interlock system consists of distributed FPGAs, housing the interlock matrix decision tables. They collect signals from interlock protected devices and distribute signals onto interlock controlled units (e.g. power supplies). Additionally, signals from external systems can be integrated. To keep the number of detector elements, which are out of operation, at a minimum, the power supplies are controlled with a high granularity. The resulting large number of channels also explains why no commercial solution was selected.

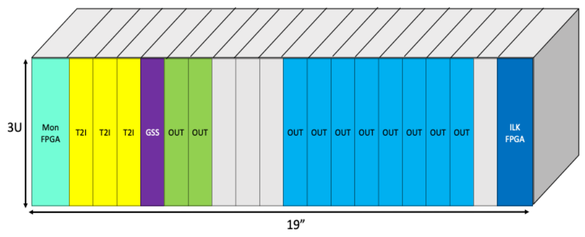
Concept



- The interlock system is a hardware based safety system
- It acts between
  - devices to be protected
  - units which can be a risk to the device
- FPGAs house the interlock matrix decision tables

- Keep number of detector units – out of operation – low!
  - high segmentation for a safety system
  - large number of channels (13000 channels)
  - custom made solution

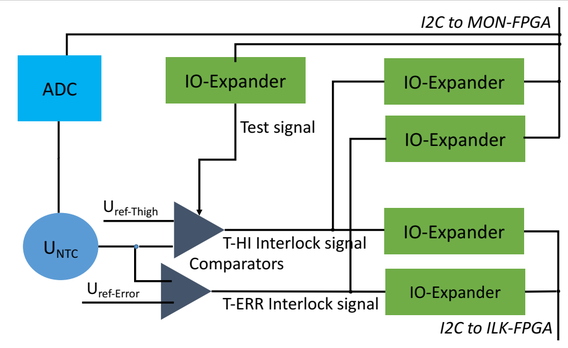
LISSY



- The **L**ocal **I**nterlock **S**afety **SY**stem is a 3U 19” crate
- Fulfill requirements of ITk strip and pixel detector
  ➔ modular system
- Sub-detectors combine modules according to their needs
- T2I module (temperature to interlock module)
- OUT module maps signals to the interlock controlled devices
- General Safety Signal module receipts signals from external

- Up to 576 interlock signals can be handled by one LISSY
- Signals are connected to the ILK FPGA via IO-expander
- 3 hardwired interlock signals
- Fail safe logic: unplugged cable = interlock

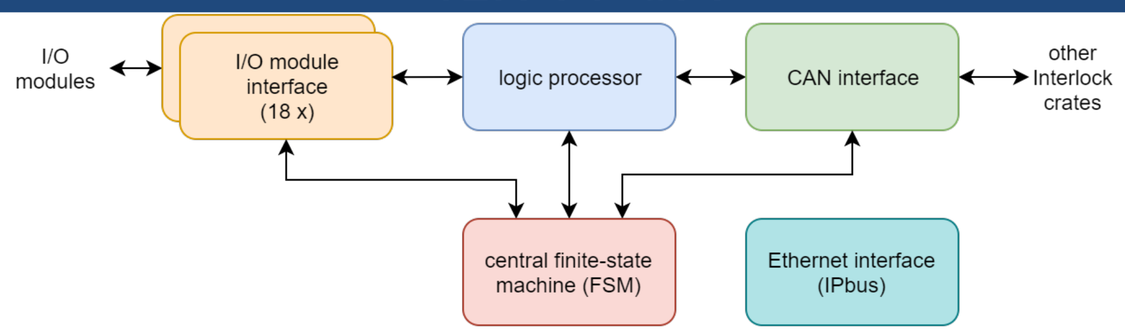
T2I module



- Main risk for all silicon detectors are heat ups
- The T2I module transfers analogues signals from a temperature sensor (NTC) into a binary interlock signal
- Discriminator to create binary interlock signal T-HI
- 2nd discriminator to detect broken cable: T-ERR
- T-HI and T-ERR are propagated to ILK-FPGA
- Threshold defined by plug-in

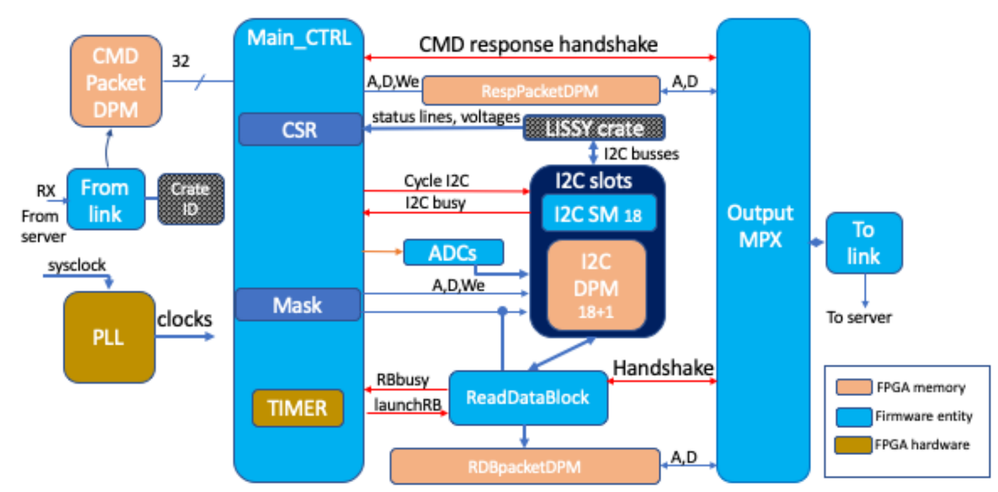
- T-HI and T-ERR are separately propagated to Mon-FPGA
- ADC for monitoring
- Test signals can be sent by Mon-FPGA

ILK-FPGA



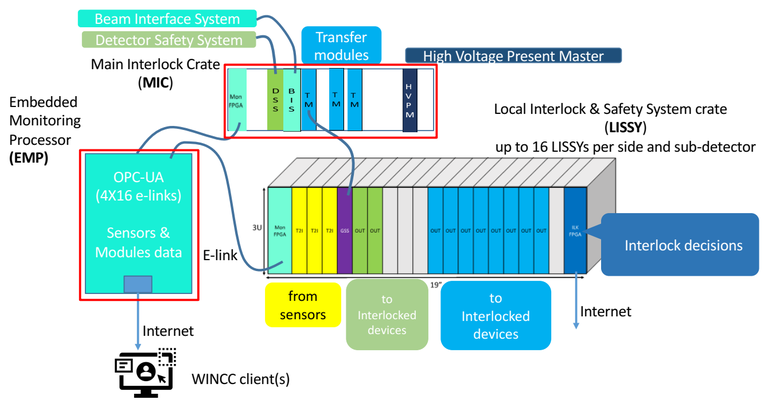
- ILK-FPGA (Xilinx Artix-7 200T) is the central decision unit in the interlock system
- Can handle up to 576 local inputs and outputs + 120 inputs from remote crates
  - I2C interface to the I/O modules at 400 kHz, CAN interface at 500 kBit/s
- Typically 10-100 Hz update rate
- User logic is separated from the FPGA firmware:
  - Same firmware running on all interlock crates
  - Interlock user logic can be updated separately during operation of the crate
  - User logic is the program running inside the logic processor
- 10/100 Mbit/s Ethernet interface for user access using IPbus interface
- Software tools:
  - Low-level tools for debugging, firmware update
  - Interlock compiler: generating user logic program from boolean equations

Mon-FPGA



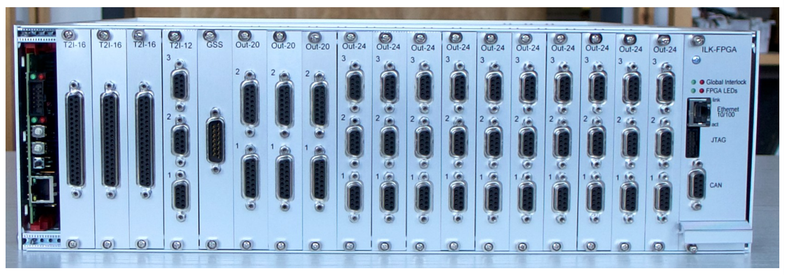
- Reads 18 LISSY modules over 18 private I2C busses
- Concurrent operation of the I2C busses
- Automatically selects the I2C readout sequence according to the module type
- Transfers the LISSY module readout data to a backend device over private LVDS link
- Non solicited mode (periodic transmission) is default
- Responds to commands from the back-end
- OPC-UA service in the back-end devices, Win-CC clients

Overall System



- Up to 16 LISSYs per sub-detector
- One Main Interlock Crate to distribute signals from external
  Beam Interface System
  Detector Safety System (cooling plants, smoke etc.)
- One EMP (embedded monitoring processor)
  collects data from Mon-FPGAs
  standard ATLAS DCS component
  OPC-UA server & integration into WinCC

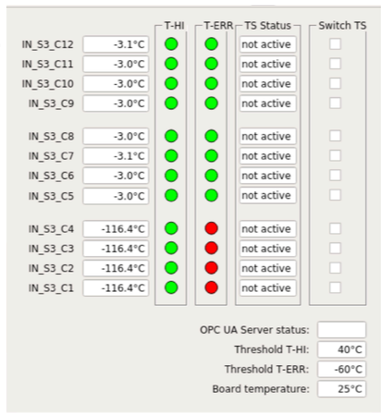
Realization



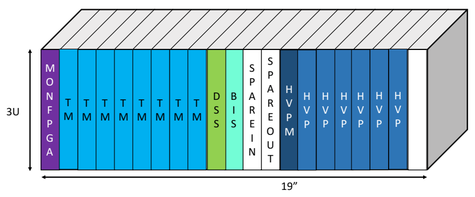
Current status:

- Pre-production of 10 crates is ongoing
- First LISSYs crates delivered to the sub-detectors
- Problem with IC delivery of Mon-FPGA
- New design available

- OPC-UA server available
- Integration into WinCC started



Outlook



Main **I**nterlock **C**rate
- Hardwired distribution of interlock signals
- Receives signals from external systems
  Beam **I**nterface **S**ystem
  ATLAS wide **D**etector **S**afety **S**ystem
- **T**ransfer **M**odule provides signals to individual LISSYs
- High Voltage Present module collects status signals of HV crates

- Before production, ensure that all needs by the sub-detectors are covered
- The ATLAS HGTD[1] has shown interest in LISSY
- Design of EMP crate, adapted to the ITK needs
- Detailed design of Main Interlock Crate

[1] High Granularity Timing Detector