

# Photodetection Module Technologies for Particle Physics and Medical Imaging

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15th Pisa Meeting on Advanced Detectors

May 22<sup>nd</sup> 2022



# Motivation for Photodetection Module Technologies R&D

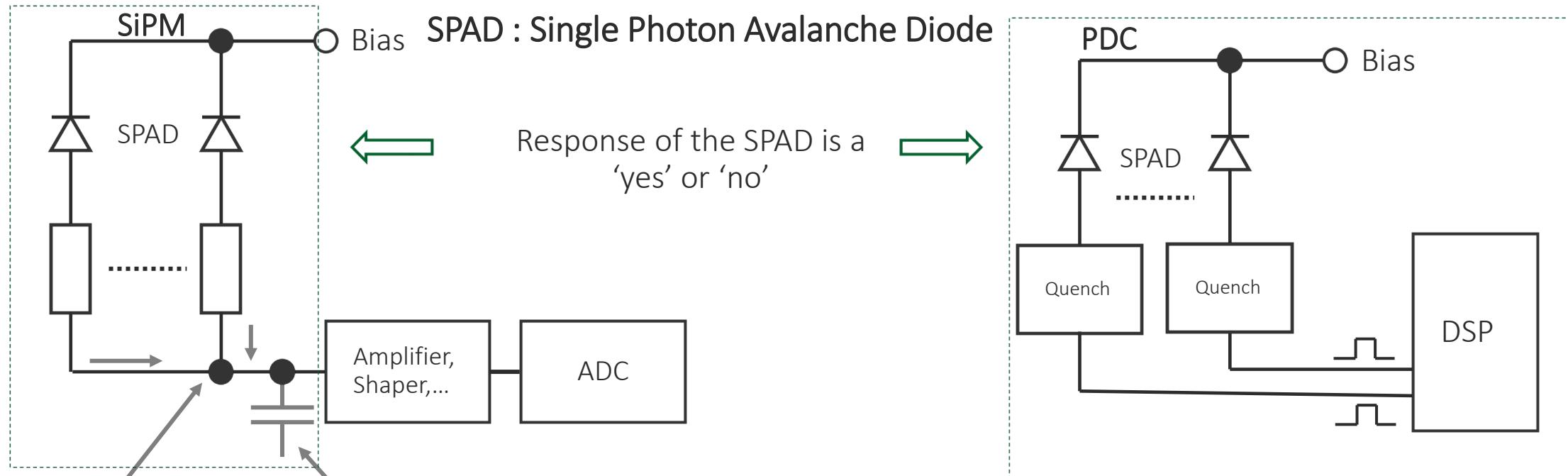
- PMTs have been the sensor of choice for decades and will remain for many systems
- Noble liquid (Xe, Ar) experiments need improved sensitivity for discovery potential
  - PMTs are x1000 more radioactive than silicon sensors, such as “analog” SiPM
- In recent experiments photosensors and electronics are located near or within the noble liquid to maximize photodetection efficiency
  - Constraint on coefficient of thermal expansion: assembly and tests at room temp while operation at cryogenic temperature
  - Radioactive background must be kept low to achieve high sensitivity
  - Minimal power consumption to avoid convection or boiling of the noble liquid

# Motivation for Photodetection Module Technologies R&D

- “Analog” SiPMs are the new trend for neutrino, dark matter and neutron imaging experiments
- The next generation of sensor that will replace “analog” SiPMs with significant advantages are “digital” SiPM, a.k.a:

## Photon-to-Digital Converters

# Analog SiPM VS Photon-to-Digital Converter (PDC)



Analog current sum

SiPM capacitance (=electronic noise)

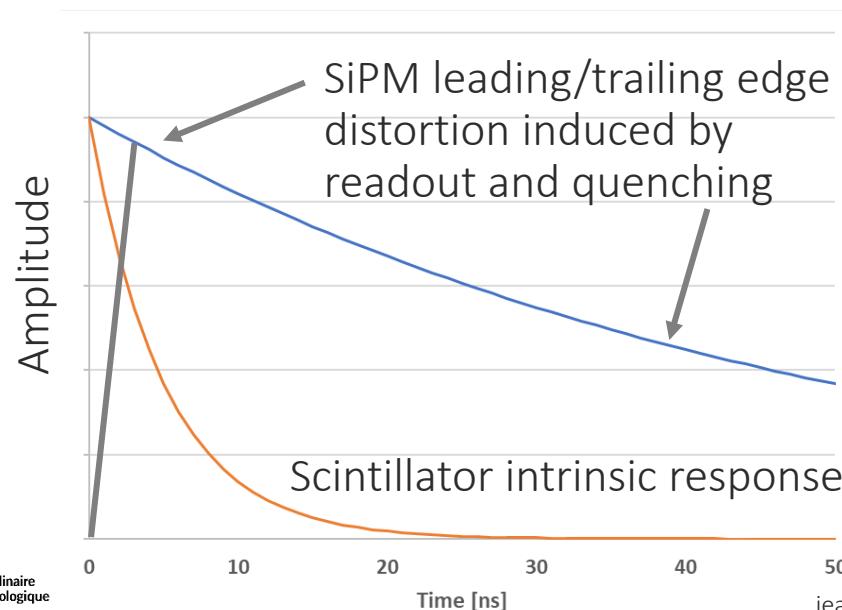
The amplifier transforms charge into voltage and then BACK to digital.

Individual SPAD readout  
No D/A+A/D conversion. Everything stays digital.

# SiPM VS PDC: To Cover Large Photosensitive Area

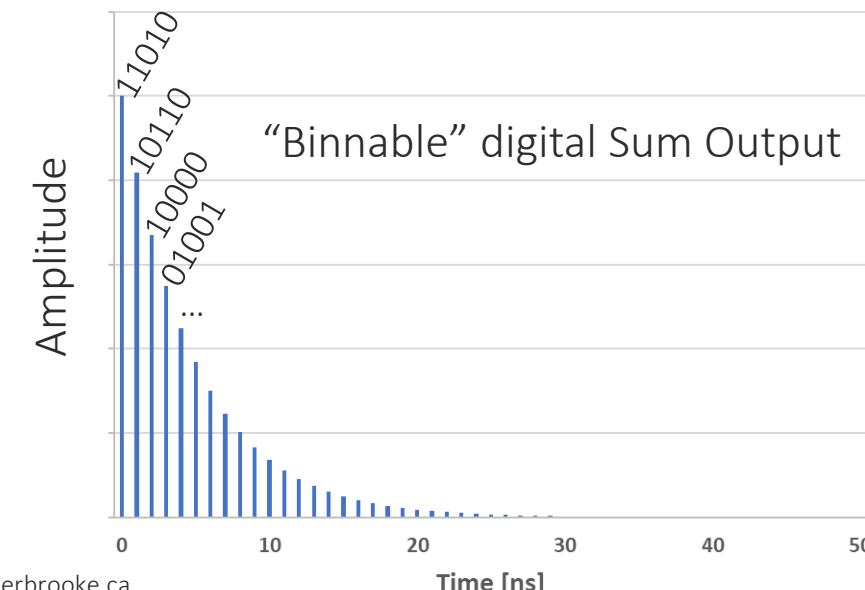
## Analog SiPM

- Need series/parallel combination to minimize the number of readout channels
  - Large input capacitance
  - Noise  $\propto$  capacitance
  - Power required to achieve single-photon resolution
  - Limited bandwidth create signal distortion



## PDC

- As one-to-one SPAD-to-CMOS readout: capacitance is not relevant
- Photon counting and binning
  - Pulse shape discrimination enabled
  - Single photon resolution over the entire dynamic range



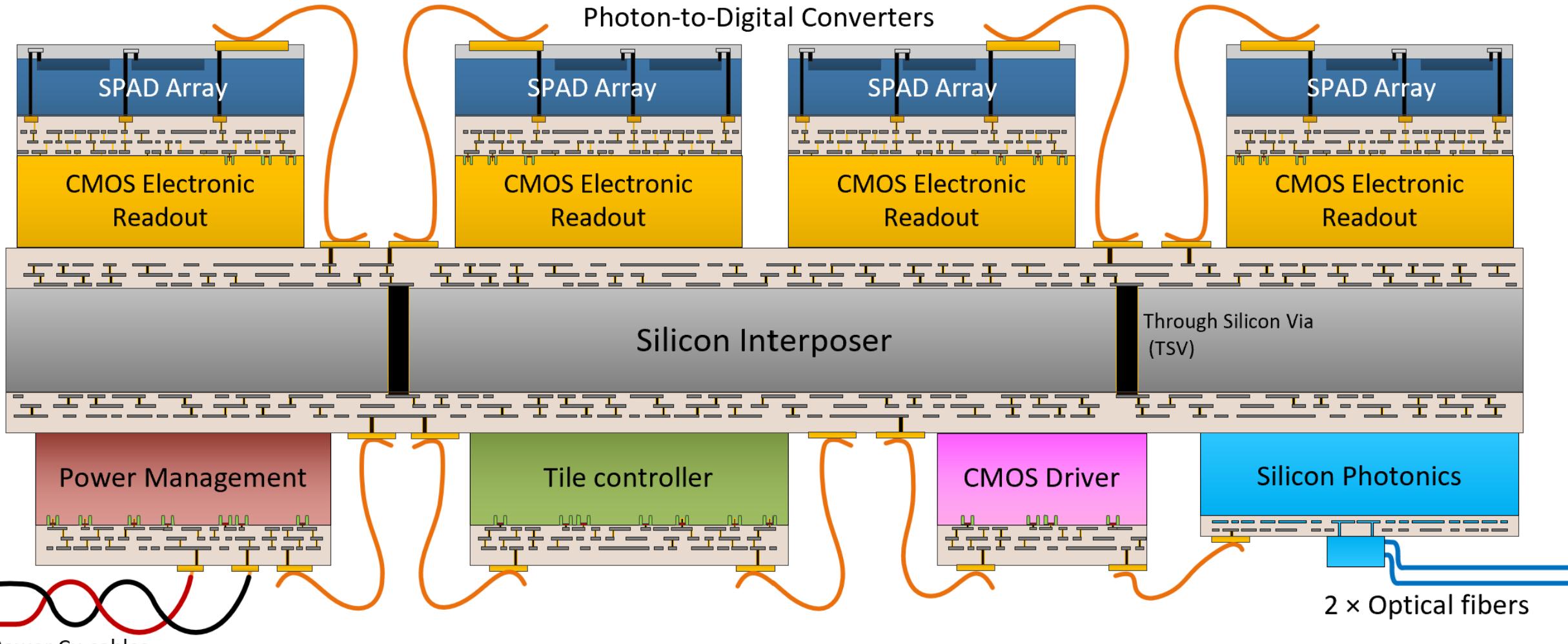
jean-francois.pratte@usherbrooke.ca

# SiPM VS PDC: Dark Count and Afterpulsing (Correlated) Noise

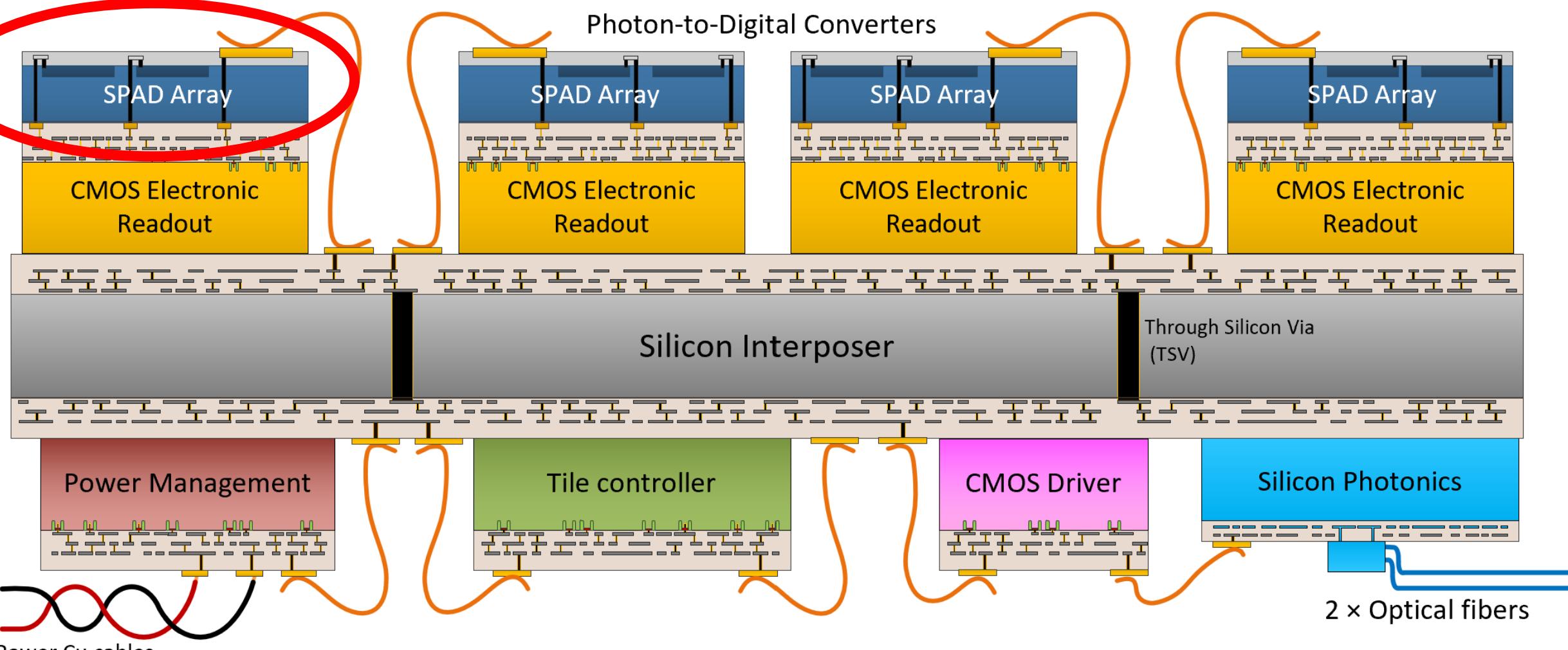
- ~90 % of dark counts are due to top ~10% noisier single photon avalanche diode (SPAD) of an array (analog SiPM or PDC)
  - Impact on single photon resolution and power consumption
  - Analog SiPM: no control
  - PDC: shut the SPADs off, hence **drastically lowering the noise**
- Cryogenic operation: Afterpulsing increase with lower temperature
  - Analog SiPM: No control (but ok, there have improved a lot on this recently)
  - PDC: Adjustable time to keep the SPAD OFF → increase effective photodetection efficiency

Vachon, Frédéric, et al. "Measuring count rates free from correlated noise in digital silicon photomultipliers." *Measurement Science and Technology* 32.2 (2020): 025105.

# Photodetection Module Technologies

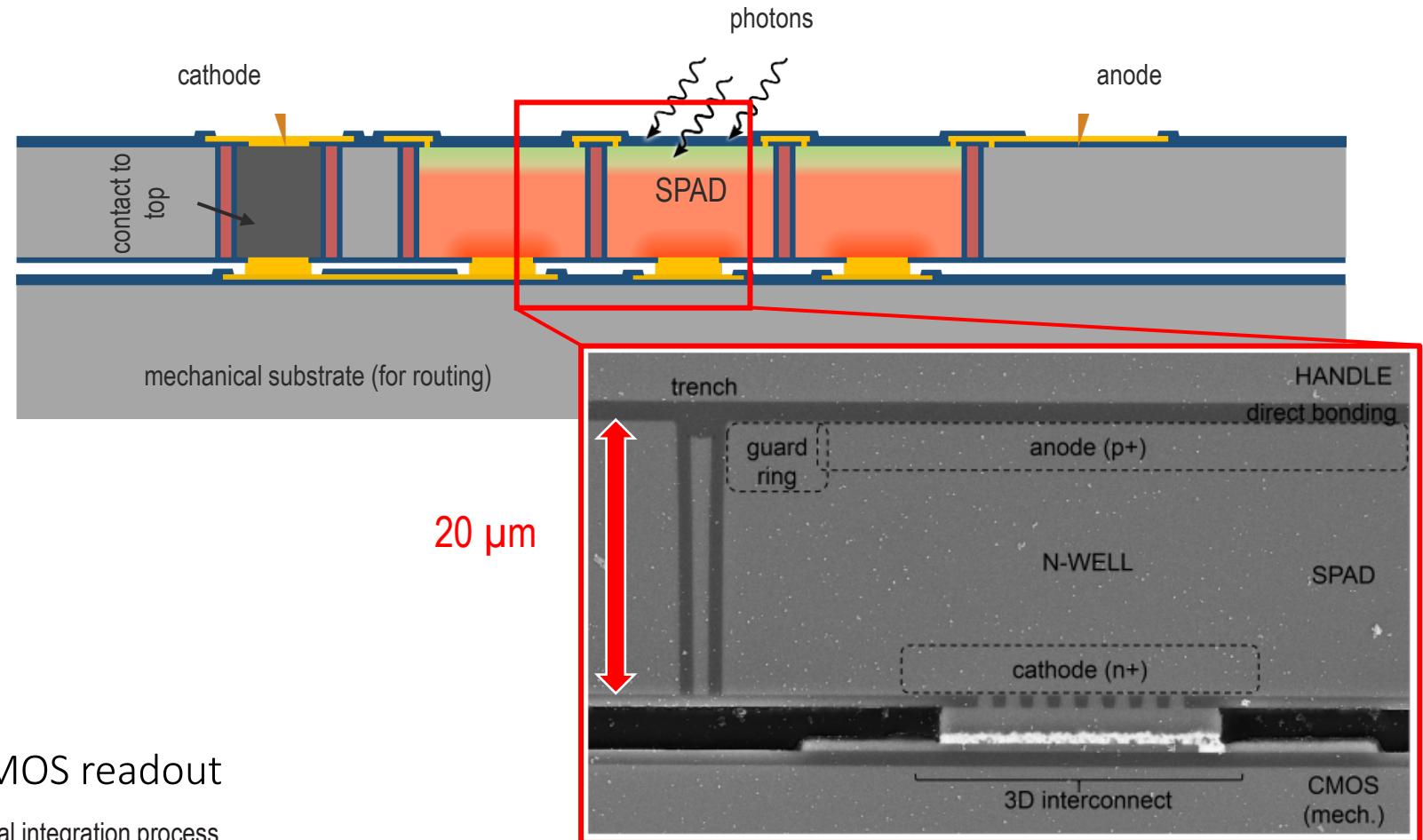


# Photodetection Module Technologies – SPAD Array



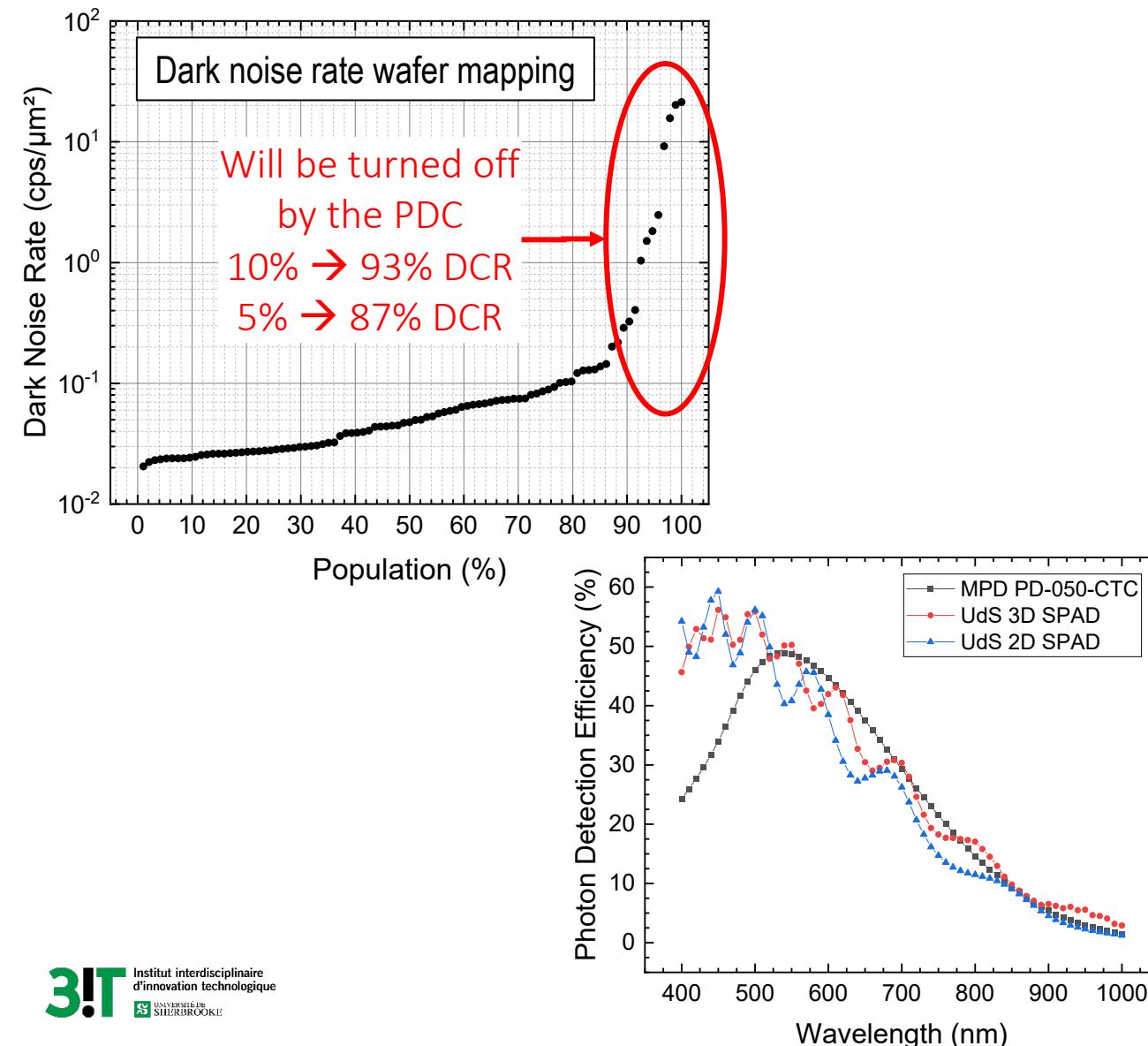
# Vertically-Integrated Frontside-Illuminated TSV-less p<sup>+</sup>n SPAD Array

- 2D SPAD and 3D integration process developed previously [1]
- Full-thickness trenches
  - optical and electrical isolation
  - TSV-less architecture
- Al-Ge eutectic bonding
- 78 µm pitch
- 64 × 64 SPAD Array
- 1<sup>st</sup> phase:
  - 3D SPAD over mechanical substrate with signal routing
- Underway
  - wafer-level 3D integration with CMOS readout



[1] Parent, Samuel, et al. "Single photon avalanche diodes and vertical integration process for a 3D digital SiPM using industrial semiconductor technologies." 2018 IEEE NSS-MIC 2018.

# SPAD Measurements Comparison Between 2D and 3D SPAD

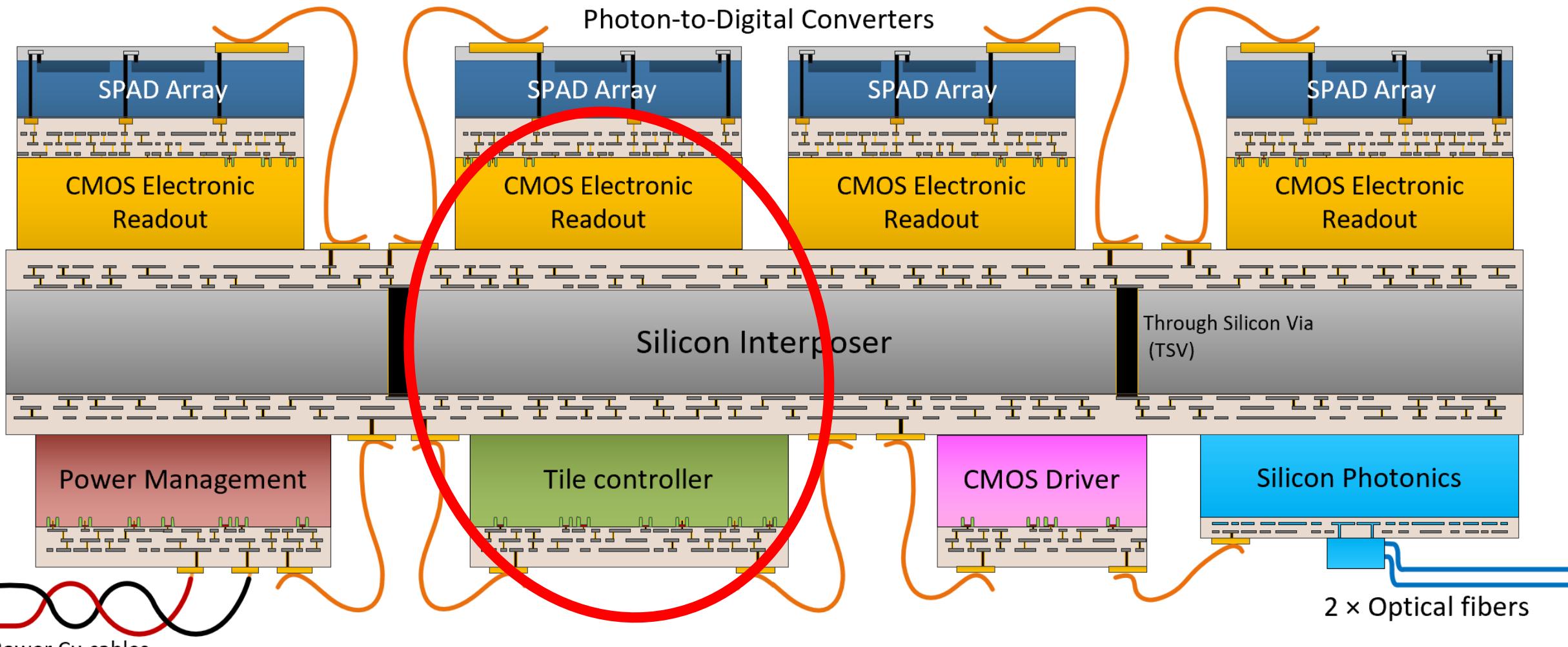


94 single SPADs tested	UdS 2D SPAD	UdS 3D SPAD
Breakdown voltage (V)	typ. 22.1	typ. 24.3
Dark Noise Rate ( $\text{cps}/\mu\text{m}^2$ )	typ. 0.78	typ. 0.05
Afterpulsing (%)	< 5	[10 – 15]
Photon Detection Efficiency peak (% at $\lambda$ )	59 (450 nm)	56 (450 nm)
Photon Detection Efficiency >15%	]400 – 740] nm	]400 – 810] nm
Single-Photon Timing Resolution (ps FWHM at $\lambda$ )	33.8 (410 nm) 21.8 (820 nm)	130.3 (410 nm) 68.6 (820nm)

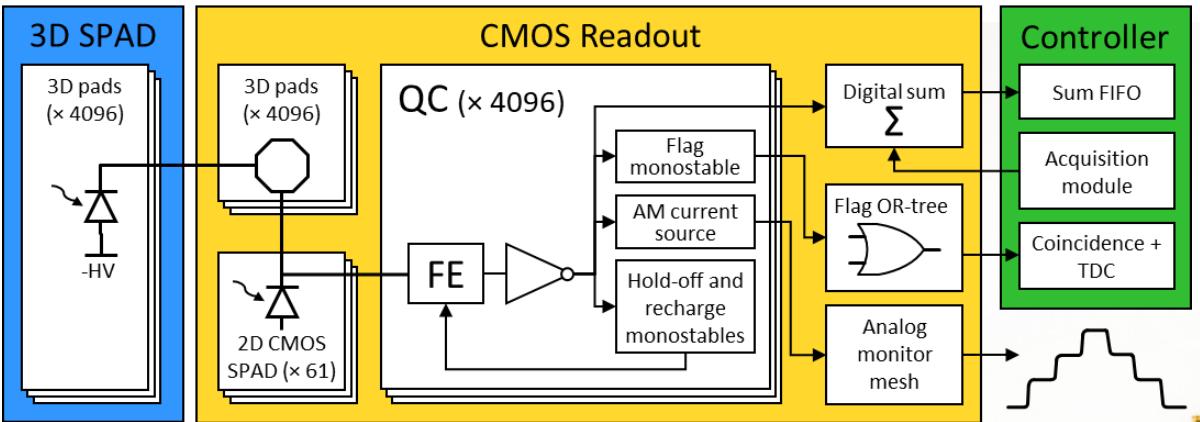
\*all measurements done at 20°C,  $V_{ov} = 25\%$ ,  $t_{ho} = 545$  ns, typical.

Please visit Frédéric Vachon's poster:  
Development of Single-Photon Avalanche Diode Array for Particle Physics and Medical Imaging

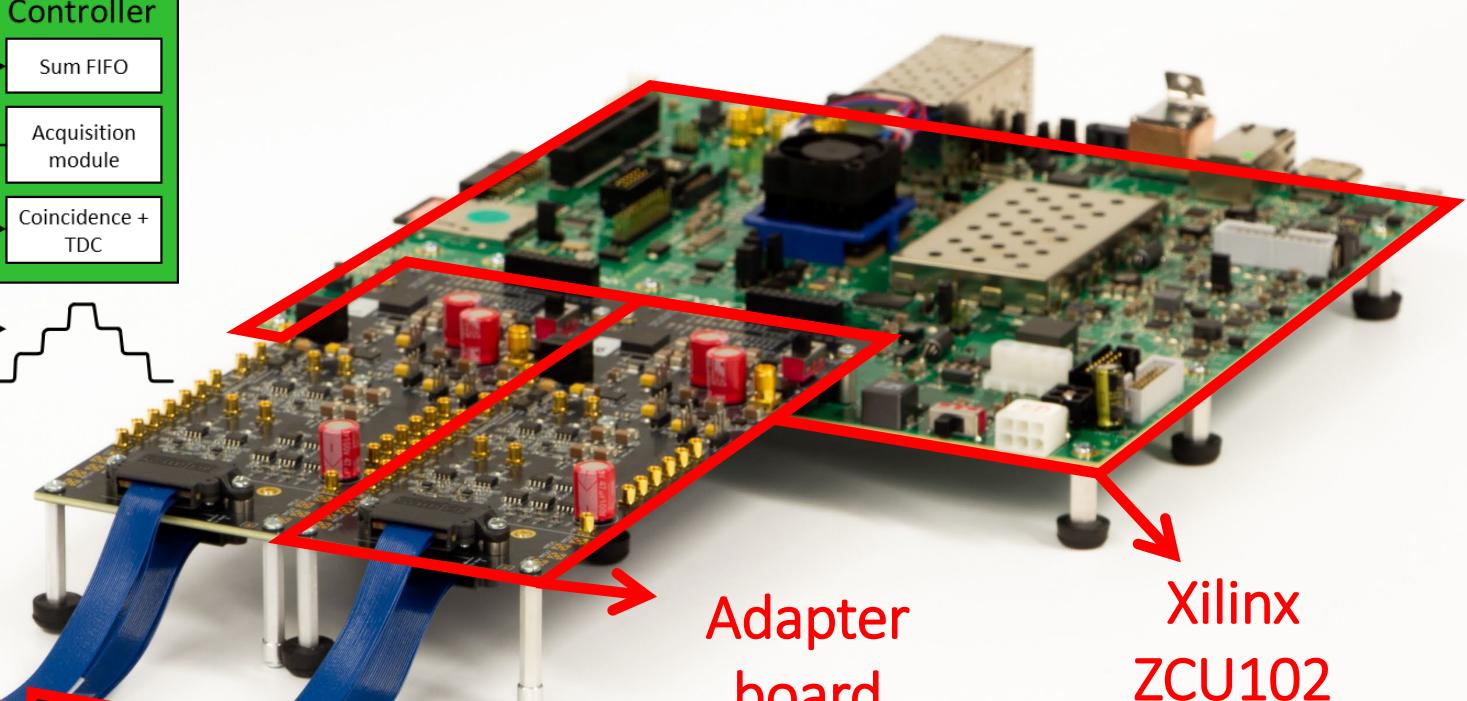
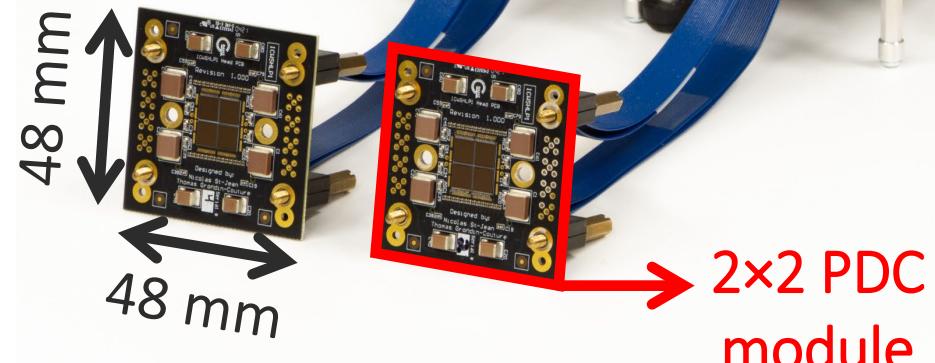
# Photodetection Module Technologies – Photon-to-Digital Converter and Tile Controller



# Photon-to-Digital Converter (PDC) and Tile Controller



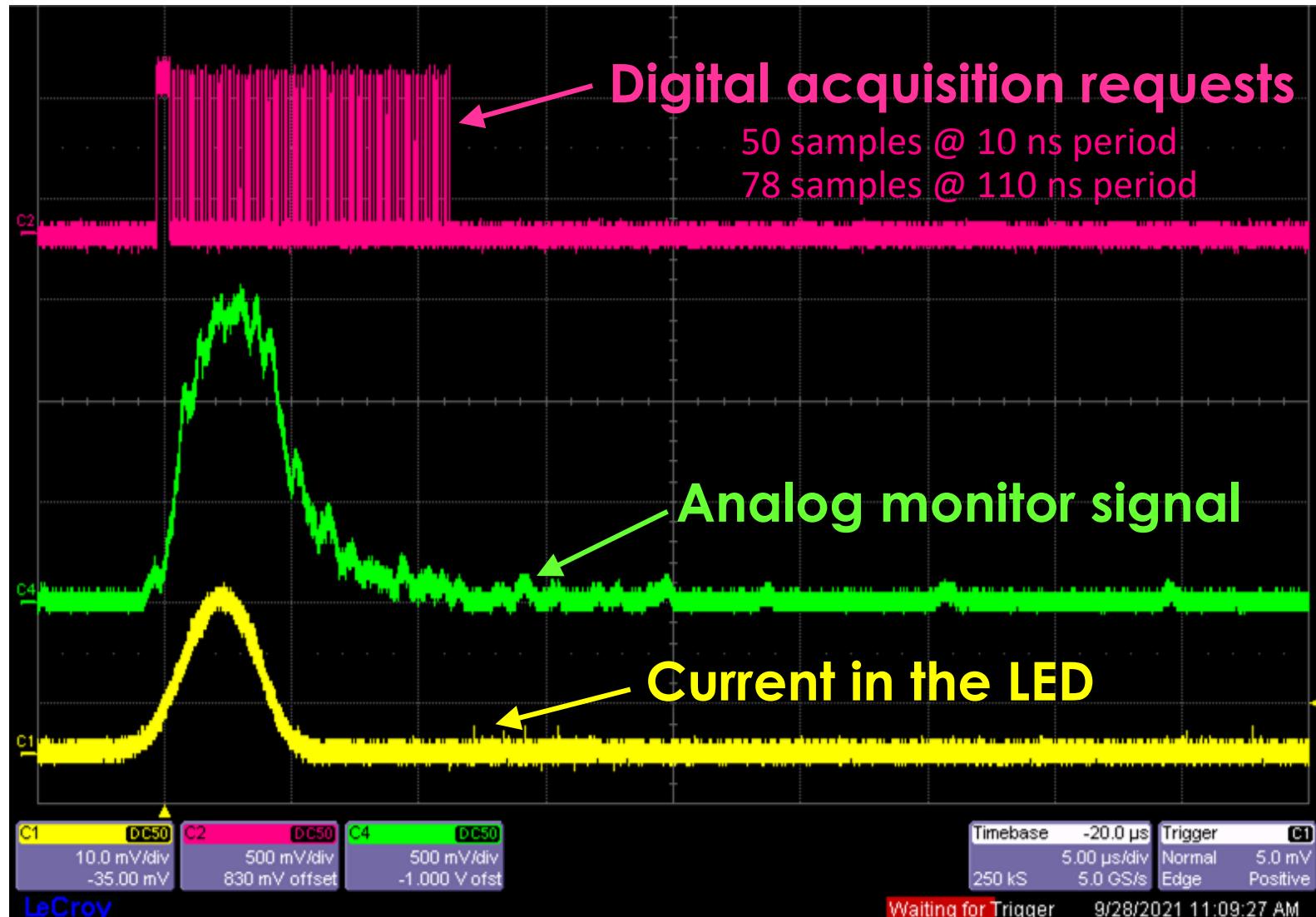
- Wafers of CMOS readout on the way
- Tile controller:
  - 1<sup>st</sup> implementation in FPGA
  - ASIC design started
  - 64 channels
  - <100 ps TDC



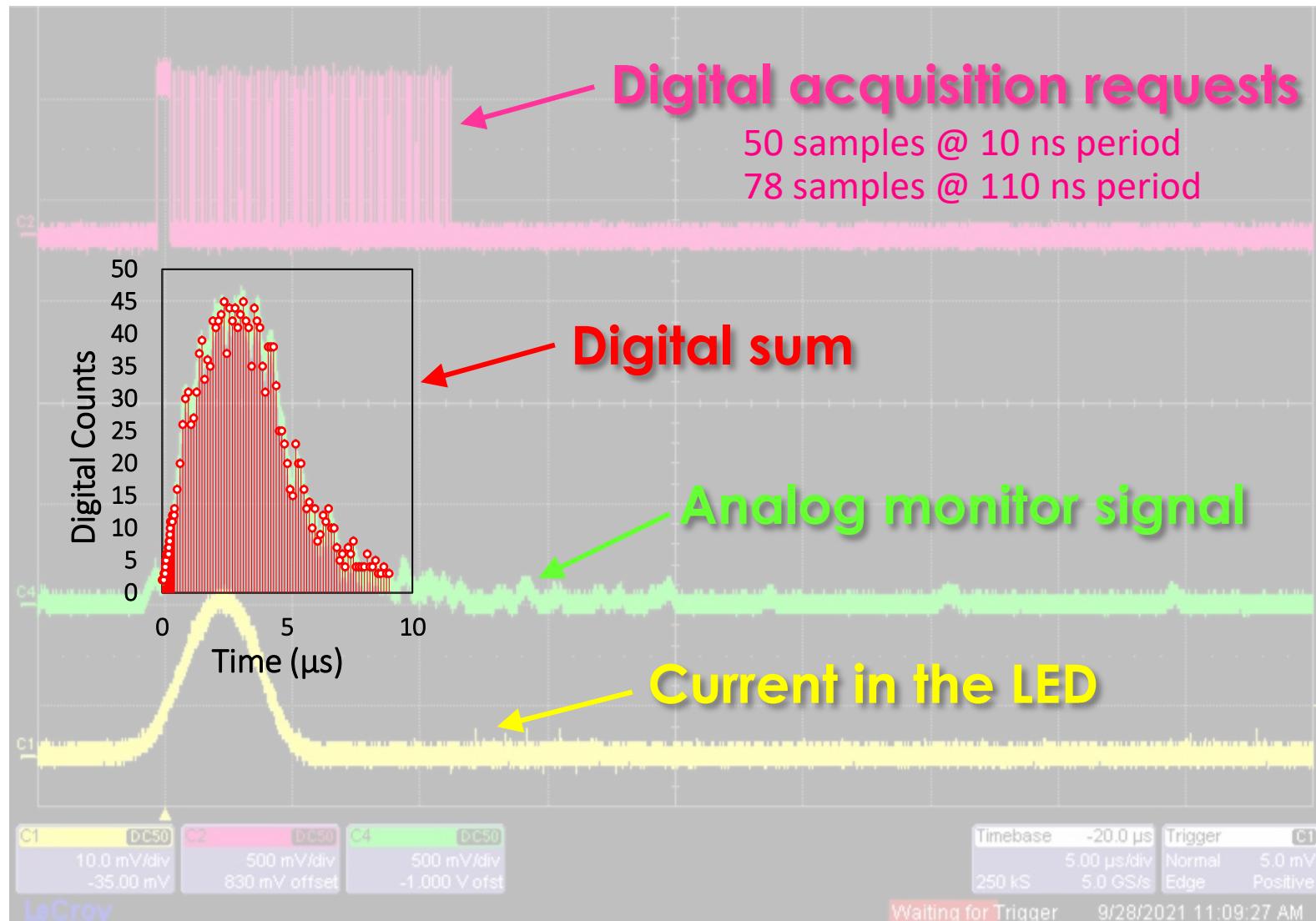
2x2 PDC  
module

Xilinx  
ZCU102  
Zynq FPGA  
platform

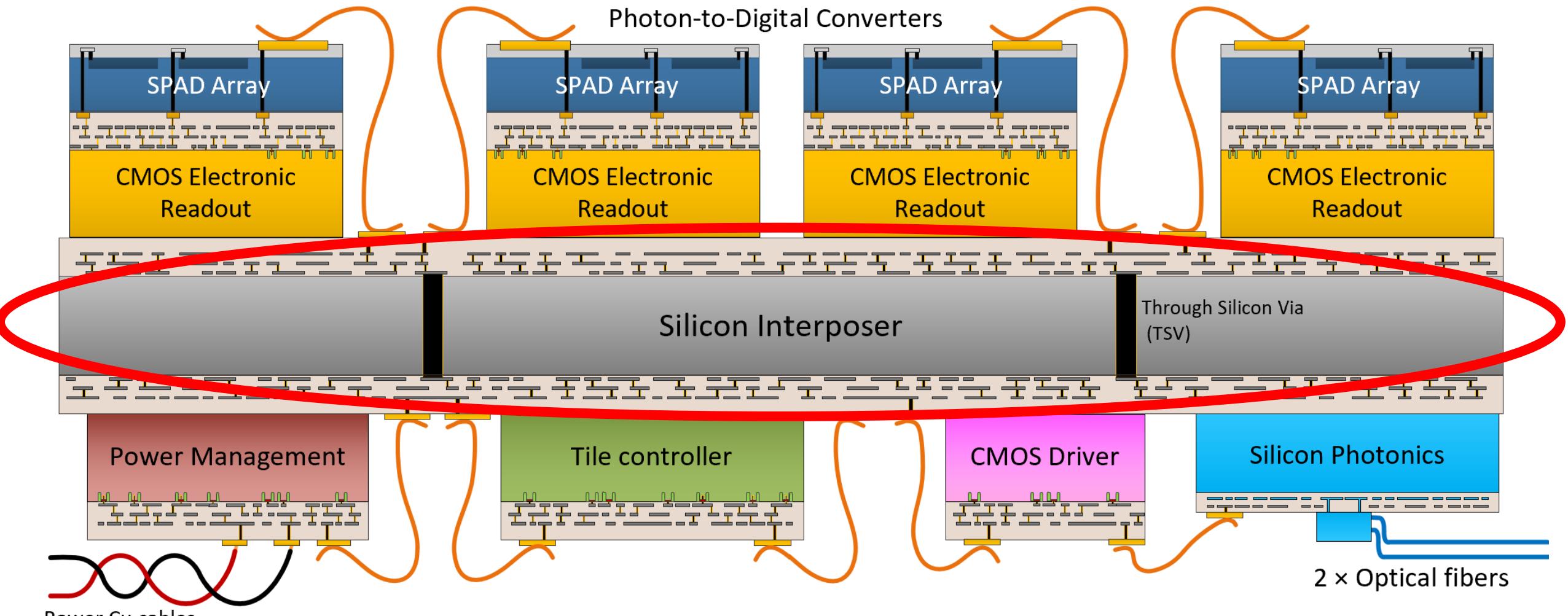
# Photon-to-Digital Converter (PDC) Acquisition with Light Source



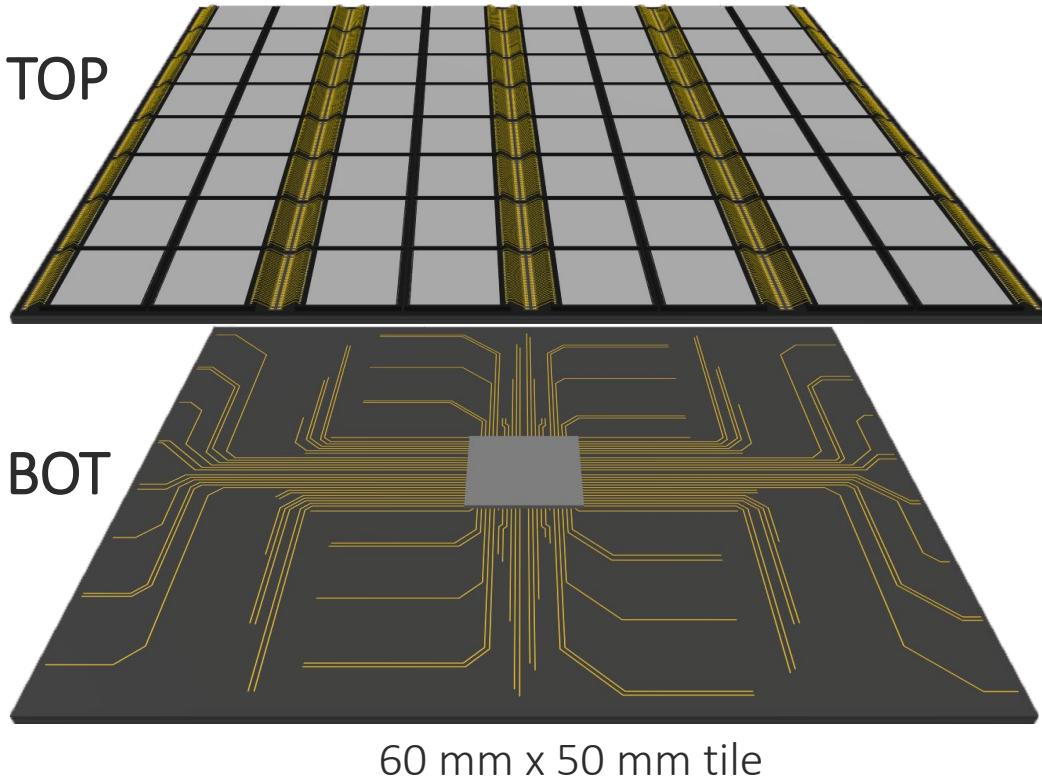
# Photon-to-Digital Converter (PDC) Acquisition with Light Source



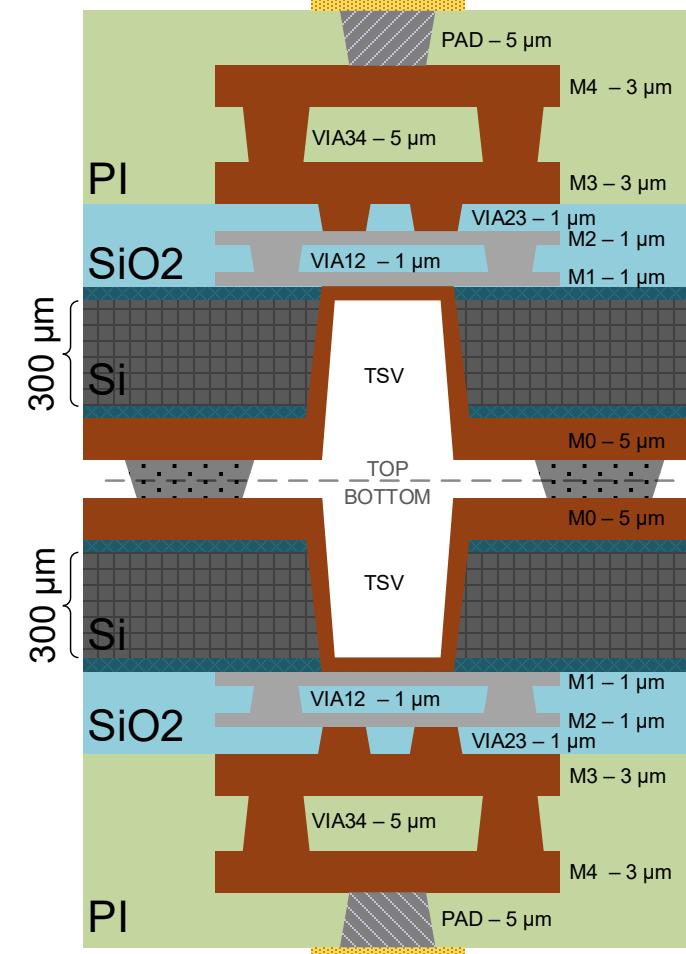
# Photodetection Module Technologies – Silicon Interposer



# $8 \times 8$ Photon-to-Digital Converter (PDC) Tile

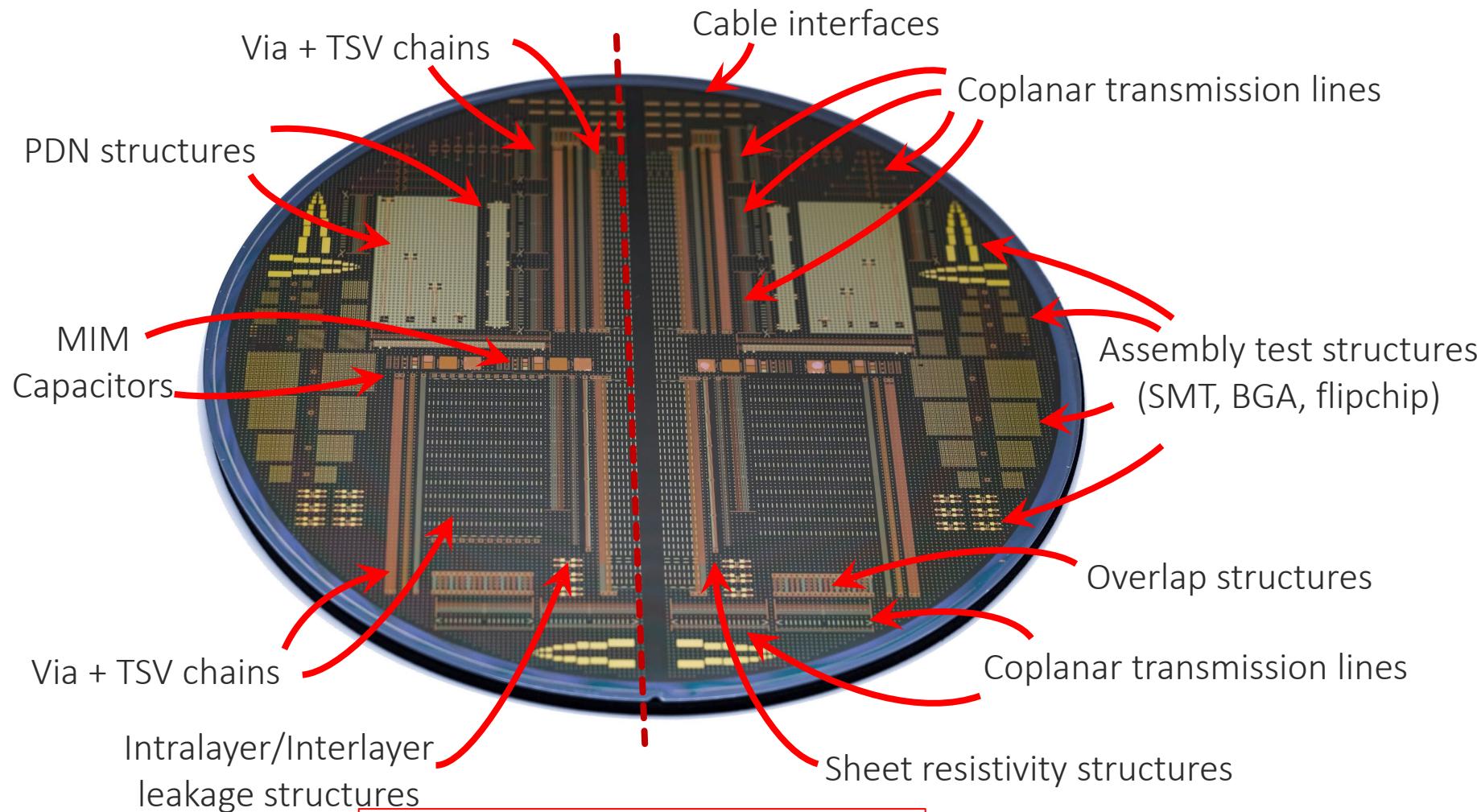


Layer	Layer main usage
M4	Transmission lines + general routing
M3	Transmission lines + general routing
M2	Power Distribution Network (PDN)
M1	PDN + TSV gateway
M0	Low-loss routing + TSV transition



R&D Contract with IZM Fraunhofer

# 200 mm Characterization Wafer and Results



Design kit for:

- Cadence
- Mentor
- Keysight
- See back up slide

# Measurement and Process Qualification

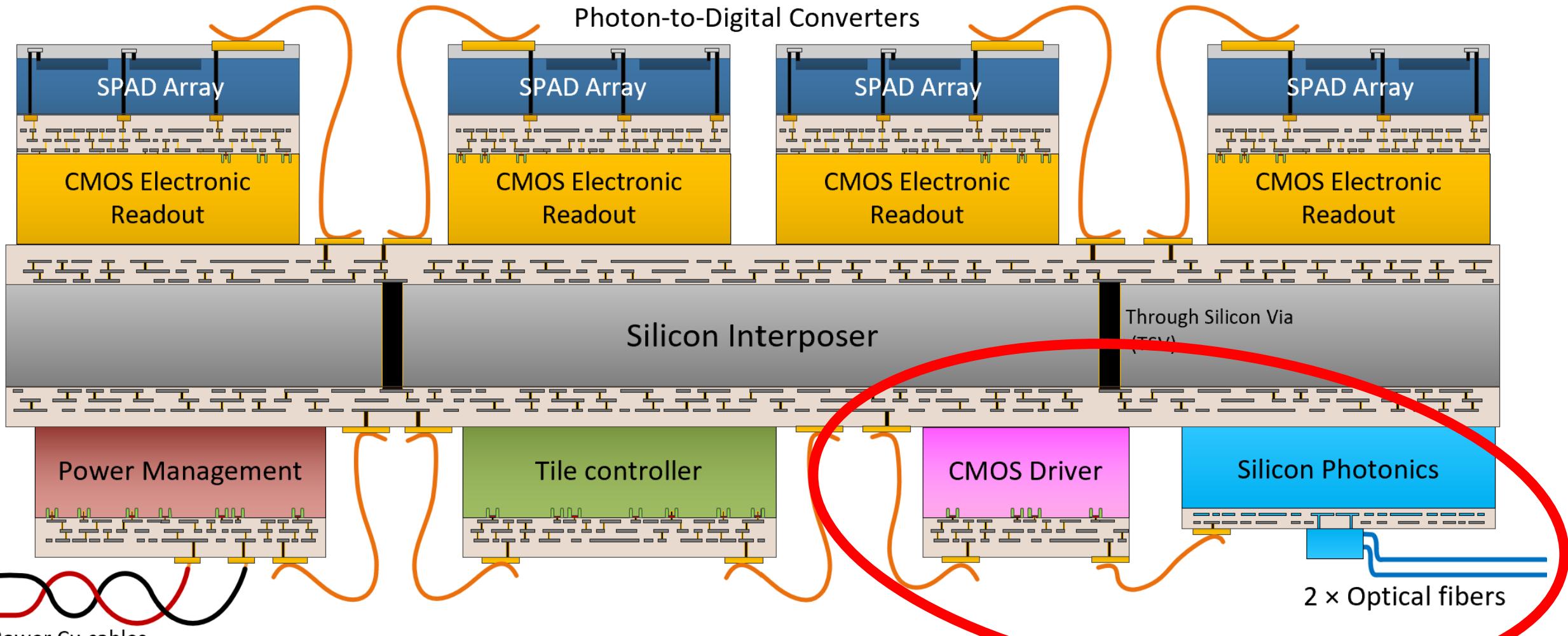
Sheet resistivity		
Layers	Value	N <sub>sq</sub>
M0	2 mΩ/sq	31 834
M1	32 mΩ/sq	56 224
M2	41 mΩ/sq	56 224
M3	5 mΩ/sq	85 660
M4	5.8 mΩ/sq	85 660

Via impedance		
Layers	Value	D.P. <sup>1</sup>
M1M2	76 mΩ N=321E3	< 1E-6
M2M3	16 mΩ N=112E3	< 3E-6
M3M4	10 mΩ N=102E3	< 3.5E-6

Overlap shorts		
Layers	Value	D.P. <sup>1</sup>
M1M2	0/3000	< 11E-3
M2M3	0/2400	< 14E-3
M3M4	0/2400	< 14E-3

<sup>1</sup> D.P = Defect probability (0.95 C.L.)  
$$\text{D.P.} = 1 / \left( -\frac{1}{N} \cdot \log P \right).$$
  
Poisson distribution

# Photodetection Module Technologies – Silicon Photonics Data Acquisition System

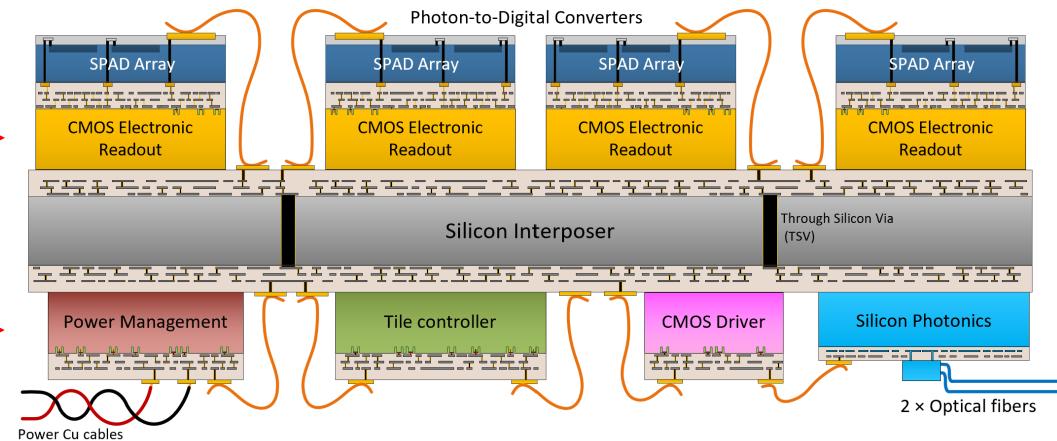


# Conclusion

- Since the last 3 years, all photodetection module technologies are **underway**
  - No roadblock so far
  - SPAD optimization started
  - CMOS wafers ordered
    - First PDC: 2023
  - Interposer:
    - Circuit design to start fall 2022
  - Controller:
    - ASIC design to start fall 2022
  - Silicon Photonic DAQ:
    - Test structures characterization underway
    - System implementation integrated circuit in fab

# Conclusion

- Looking for partners:
  - CMOS readout with TSV in pads (FF ↑↑↑)
  - Power management ASIC for the PDM
  - Mechanical assembly of PDM for larger area
  - Open to ideas and collaborators
- Looking for post-doc and PhD
- Looking for other partners interested in those technologies
- Please visit our poster on SPAD development: discussion welcomed



Frédéric Vachon

# A team's work

## Université de Sherbrooke

- Roger Lecomte
- Nicolas Roy
- Luc Maurais
- Henri Dautet
- Frédéric Nolet
- Maxime Côté
- David Danovitch
- Samuel Parent
- Vincent Philippe Rhéaume
- Caroline Paulin
- Audrey Corbeil Therrien
- Étienne Desaulniers Lamy
- Catherine Pepin
- Benoit-Louis Bérubé
- Alexandre Boisvert
- Étienne Paradis
- Marc-André Tétrault
- Michel Labrecque-Dias
- Étienne Grondin
- Frédéric Vachon
- Pascal Gendron
- Konin Koua
- Tommy Rossignol
- Arnaud Samson
- Simon Carrier
- Gabriel St-Hilaire
- Jonathan Bouchard
- Guillaume Théberge-Dupuis
- Jacob Deschamps
- Frédéric Dubois
- Sean Prentice
- Xavier Bernard
- Marc-Olivier Mercier
- Gabriel Lessard
- Thomas Dequivre
- Frédéric Bourque
- Philippe Arsenault
- William Lemaire
- Keven Deslandes
- Philippe Martel-Dion
- Charles-Frédéric Gauthier
- Artur Turala
- Valérie Gauthier



**CANADA  
FIRST**  
RESEARCH  
EXCELLENCE  
FUND

**APOGÉE  
CANADA**  
FONDS  
D'EXCELLENCE  
EN RECHERCHE



## Collaborators

- Fabrice Retiere (Triumf)
- Lorenzo Fabris (ORNL)
- Simon Viel (Carleton)
- nEXO Collaboration
- nEXO Canada
- DarkSide / ARGO



**Fonds de recherche  
sur la nature  
et les technologies**



Regroupement Stratégique  
en Microsystèmes du Québec



## Teledyne DALSA Semiconducteur Inc

- Claude Jean (CEO)
- Stephane Martel
- Robert Groulx
- Maxime Côté



**Arthur B. McDonald**  
Canadian Astroparticle Physics Research Institute

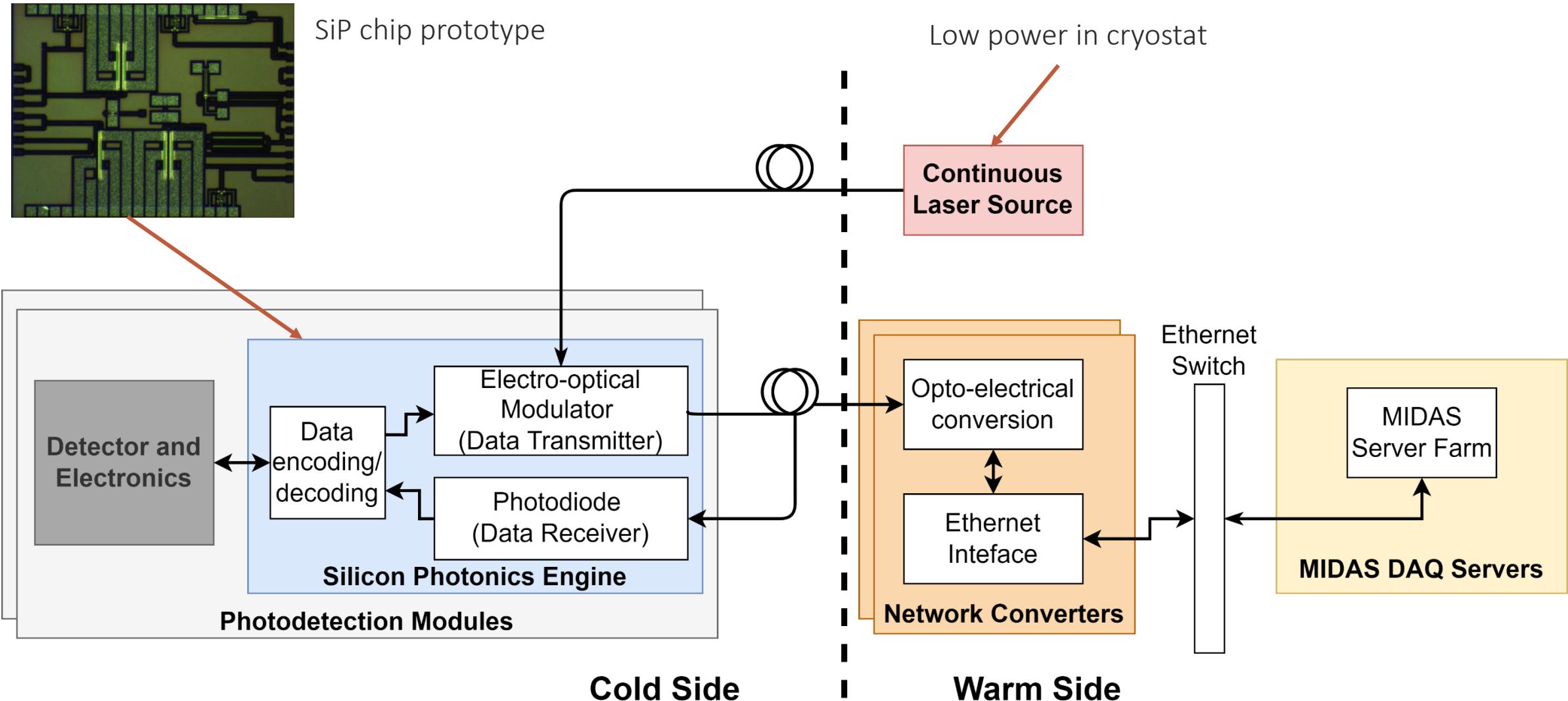


# Back up

# Silicon Photonics Data Acquisition System

- **Main goal:** Support a data acquisition system for a large array of photodetectors in cryogenic large scale detectors
- Needs and Requirements
  - Reusable systems for different types of photodetectors and experiments
  - Operate at cryogenic temperatures → among the first in SiP field (165K to 4K)
  - Low power budget → **external laser source**
  - Acquire data at ~1 Gb/s per module
  - Radio-pure materials inside the cryostat
- Benefits
  - Allows for high galvanic isolation
  - Allows for long range communication over optical fibers

# System Description



# Interposer Design Kit – Cadence, Mentor and Keysight

A multi-software design kit was developed to support 3 industry standard software to enable design, validation and simulation with the Sherbrooke-IZM interposer technology.

Cadence Virtuoso (IC6.17)	Mentor Calibre (2020.01)	Keysight ADS (2021U1)
Used for mask designs (1x scale)	Used for design verification	Used for RF simulations
<u>ASCII Technology File</u>	<u>Layout vs Schematic (LVS)</u>	<u>Simulation type:</u> Full wave Method of Moment (MOM) Finite element method (FEM)
<u>Schematic XL + Layout XL</u> ➤ Design Rule Driven (DRD) Editing ➤ Constraints Driven Design ➤ Analog Auto Placer ➤ Space-based Router	<u>Design Rule Check (DRC)</u> <u>Parasitic Extraction (PEX)</u> ➤ Distributed Resistance ➤ Distributed Capacitance ➤ Coupling Capacitance	<u>Custom material from measurements:</u> ➤ Conductivity ➤ Complex permittivity ( $\epsilon_r + j\epsilon_i$ )
<u>Custom SKILL PCells</u> ➤ PDC cluster		