INTRODUCTION

University of Sherbrooke (UQS) in partnership with Teledyne DALSA Semiconductor (TDS) is developing a photodetection module based on single-photon avalanche diodes (SPAD) where each pixel is vertically integrated to a CMOS electronic readout. 3D integration takes full advantage of the digital signal processing capabilities of CMOS electronics without compromising the photosensitive area of the detector [1].

For large-area experiments in particle physics, the photon-to-digital converter (PDC) is to be assembled on silicon interposers to prevent thermal expansion mismatches at cryogenic temperatures. The PDCs digitalized information is managed by a Xilinx controller and sent to the user by means of a silicon photonic communication module.

OBJECTIVES

The 3D SPAD technology is based on a frontside illuminated (FSi) TSV-less p n architecture. The SPAD and 3D integration processes were developed separately and reported previously [2]. In order to assess the first prototypes at TDS, in parallel to the development of the CMOS readout circuit, 3D SPADs were first vertically integrated to a mechanical substrate with signal routing.

3D SPAD process overview

The SPAD process relies on 3D integration technologies standard in the semiconductor industry. The SPAD junction profile and trenches are done first [1]. Then, the SPAD array frontside is bonded to a handle wafer (2) to act as a mechanical support during the SPAD backside thinning (3). SPADs are 3D-bonded at wafer-level using an eutectic bonding (4). Finally, the handle wafer is removed (5) to reveal the SPADs frontside and to make the metal contacts.

CHARACTERIZATION METHODS

Single SPADs are characterized using an external readout circuit (quenching circuit - QC). The QC detects and quenches the avalanche and, after a configurable period (holdoff delay), recharges the SPAD in its ready state.

SPADs are either characterized at wafer-level with the QC input channel fixed to a probe or at die-level with wirebonds [4-5].

REFERENCE