# Development of Single-Photon Avalanche Diode Array for Particle Physics and Medical Imaging

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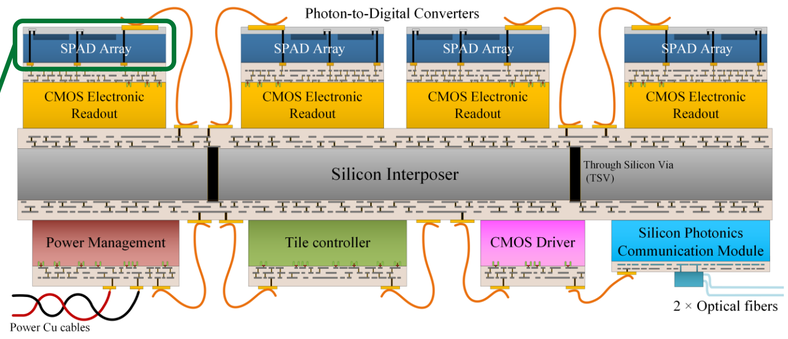
## INTRODUCTION

University of Sherbrooke (UdS) in partnership with Teledyne DALSA Semiconductor (TDS) is developing a photodetection module based on single-photon avalanche diodes (SPAD) where each pixel is vertically integrated to a CMOS electronic readout. 3D integration takes full advantage of the digital signal processing capabilities of CMOS electronics without compromising the photosensitive area of the detector [1].

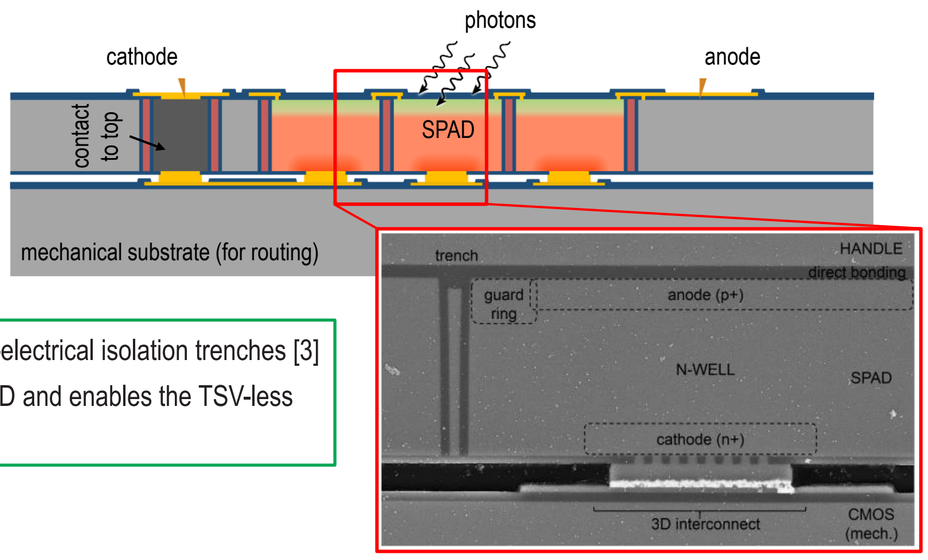
For large-area experiments in particle physics, the photon-to-digital converter (PDC) is to be assembled on silicon interposers to prevent thermal expension mismatches at cryogenic temperatures. The PDCs' digitalized information is managed by a tile controller and sent to the user by means of a silicon photonics communication module.

This poster presents the characterization of the SPAD array 3D-integrated to a redistribution layer wafer.




## OBJECTIVES

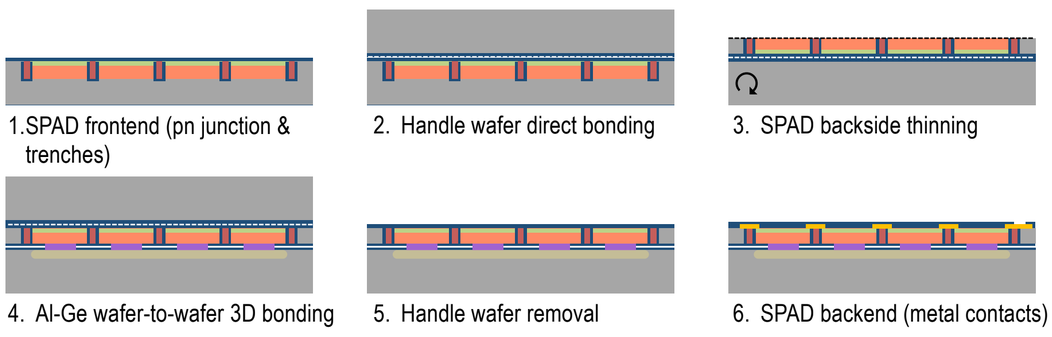
The 3D SPAD technology is based on a frontside illuminated (FSI) TSV-less $p^+n$ architecture. The SPAD and 3D integration processes were developed separately and reported previously [2]. In order to assess the first prototypes at TDS, in parallel to the development of the CMOS readout circuit, 3D SPADs were first vertically integrated to a mechanical substrate with signal routing.




Full-thickness opto-electrical isolation trenches [3] surround each SPAD and enables the TSV-less architecture.

### 3D SPAD process overview

The SPAD process relies on 3D integration technologies standard in the semiconductor industry. The SPAD junction profile and trenches are done first (1). Then, the SPAD array frontside is bonded to a handle wafer (2) to act as a mechanical support during the SPAD backside thinning (3). SPAD are 3D-bonded at wafer-level using an eutectic bonding (4). Finally, the handle wafer is removed (5) to reveal the SPADs frontside and to make the metal contacts.

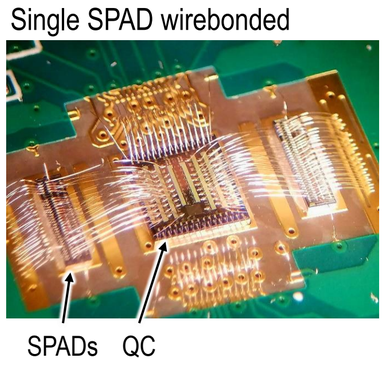



## CHARACTERIZATION METHODS

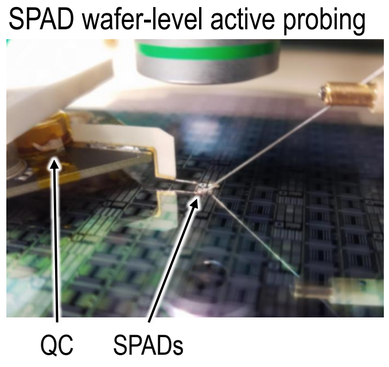
Single SPADs are characterized using an external readout circuit (quenching circuit - QC). The QC detects and quenches the avalanche and, after a configurable period (holdoff delay), recharges the SPAD in its ready state.

SPADs are either characterized at wafer-level with the QC input channel fixed to a probe or at die-level with wirebonds [4-5].

Single SPAD wirebonded



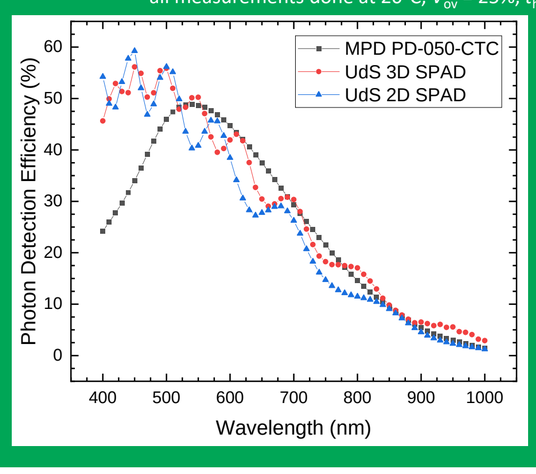

SPAD wafer-level active probing

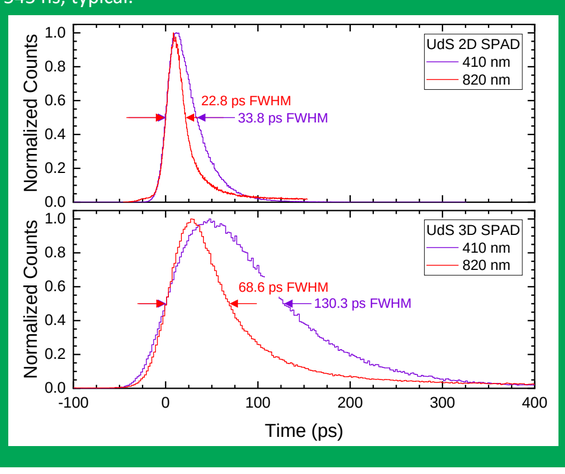



## Measurement Results

| | UdS 2D SPAD | UdS 3D SPAD |
|---|---|---|
| Breakdown voltage (V) | typ. 22.1 | typ. 24.3 |
| Dark Noise Rate (cps/μm²) | typ. 0.78 | typ. 0.05 |
| Afterpulsing (%) | < 5 | [10 – 15] |
| Photon Detection Efficiency peak (% at λ) | 59 (450 nm) | 56 (450 nm) |
| Photon Detection Efficiency >15% | ]400 – 740] nm | ]400 – 810] nm |
| Single-Photon Timing Resolution (ps FWHM at λ) | 33.8 (410 nm)<br>21.8 (820 nm) | 130.3 (410 nm)<br>68.6 (820nm) |

*all measurements done at 20°C, $V_{ov}$ = 25%, $t_{ho}$ = 545 ns, typical.



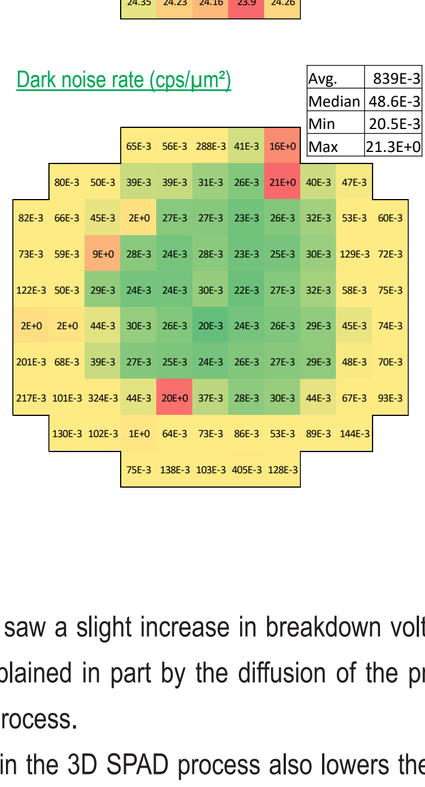




## 3D SPAD wafer mapping

- The breakdown voltage is uniform throughout the wafer with a slight decrease towards the lower right-hand side ($\sigma$ = 0.13V).
- The relative sensitivity of SPADs at λ = 462 nm is uniformally distributed and doesn't depend on the noise distribution.
- Concentric distribution of the dark noise is caused by metal contacts misalignment during in-process issues (known solution underway).
- Outliers represent less than 10% of the population.

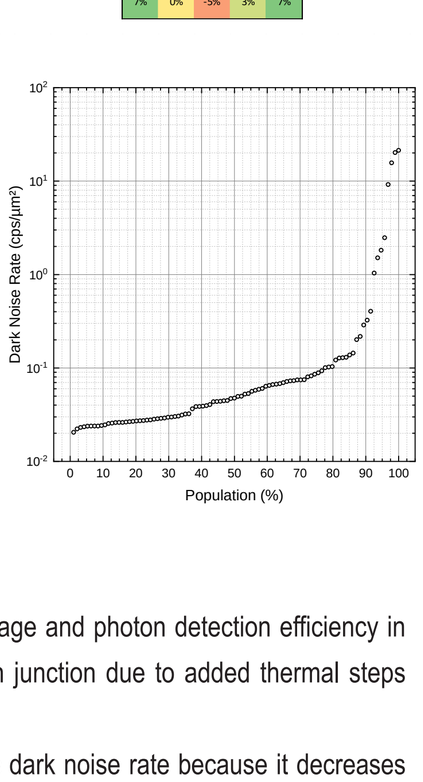
Breakdown voltage (V)

| | |
|---|---|
| Avg. | 24.30 |
| Median | 24.32 |
| Min | 23.90 |
| Max | 24.51 |




Relative sensitivity at λ = 462 nm

| | |
|---|---|
| Avg. | 0.5% |
| Median | 0% |
| Min | -7.7% |
| Max | +8.9% |




Dark noise rate (cps/μm²)

| | |
|---|---|
| Avg. | 839E-3 |
| Median | 48.6E-3 |
| Min | 20.5E-3 |
| Max | 21.3E+0 |







## DISCUSSION

- The 3D SPAD technology saw a slight increase in breakdown voltage and photon detection efficiency in the red spectrum. It is explained in part by the diffusion of the pn junction due to added thermal steps during the 3D integration process.
- Additionnal thermal steps in the 3D SPAD process also lowers the dark noise rate because it decreases the field-enhanced noise generation, helps cristal lattice damage reconstruction and reduces mid-gap defect state density.
- Further characterization is underway to assess the increase of the single-photon timing resolution and afterpulsing.

## CONCLUSION

This work demonstrates the TSV-less frontside illuminated 3D SPAD architecture in the context of the in-development photon-to-digital converter technology. The next major steps include the 3D SPAD integration with CMOS wafers to achieve 3D PDC prototypes as well as improving the technology readiness level at the TDS foundry.

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### REFERENCES

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