The CMS Pixel Detector for the High Luminosity LHC

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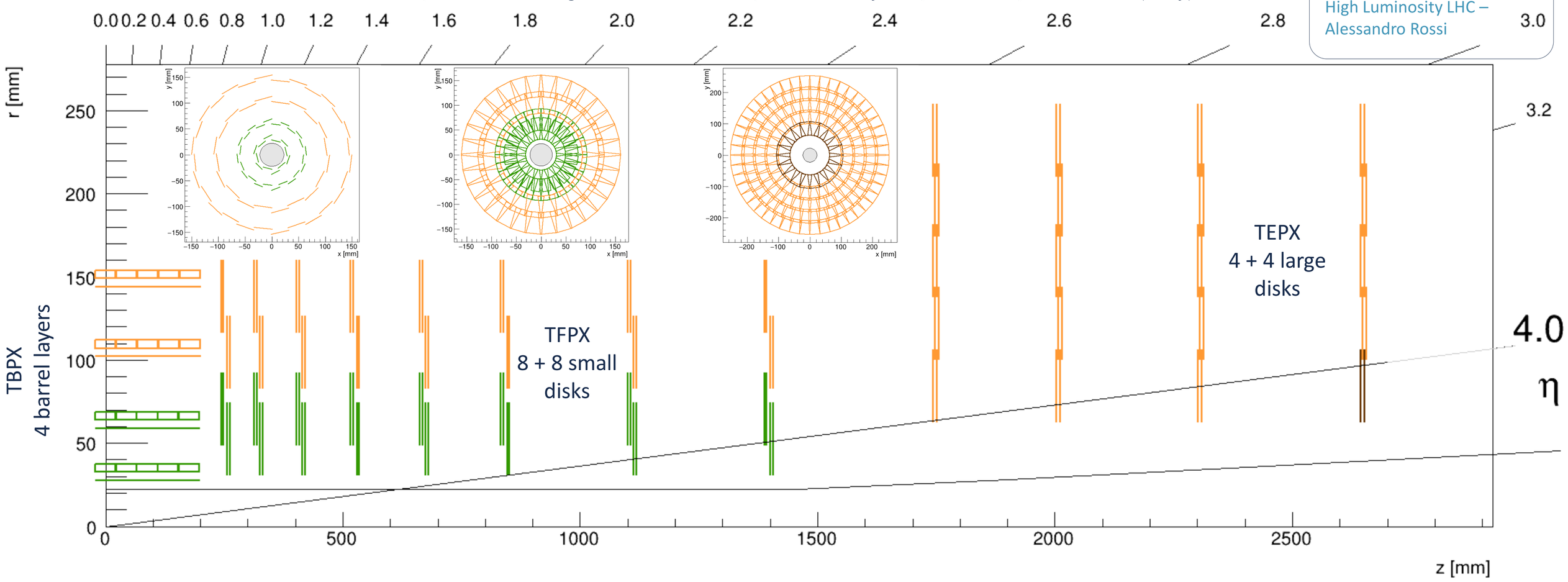
Talk: The CMS Tracker for the High Luminosity LHC – Alessandro Rossi



High Luminosity LHC

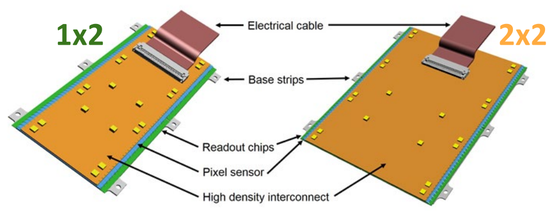
	LHC (after 2010)	HL-LHC
E_{CM} [TeV]	7 ÷ 14	14
L_{IST} [$cm^{-2}s^{-1}$]	2×10^{34}	$5 \div 7.5 \times 10^{34}$
PU	< 50 ÷ 60	140 ÷ 200
L_{INT} [fb^{-1}]	300	3000 ÷ 4500

Resulting in:
- Dose & fluence 10x higher
- 750 kHz L1 rate
- 12.5 µs L1 latency

→ The present CMS tracker cannot sustain the foreseen radiation levels and data rates and has to be completely replaced

CMS HL pixel detector

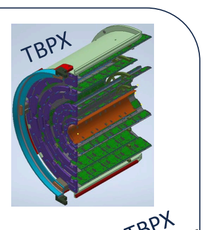
- High radiation tolerance:
  - > 2.3×10^{16} n_{eq}/cm^2, fluence
  - > 1.2 Grad, TID
- Improve tracks separation:
  - > High granularity
  - > Low material budget
  - > High bandwidth (up to 3.5 GHz/cm^2 occupancy)
- Extend tracking coverage ($|\eta| \leq 4$)
- Stringent space constraints
- Thin planar n-in-p and 3D silicon sensors
- Operation at -20°C
- Innovative power scheme

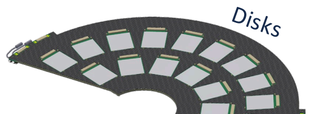


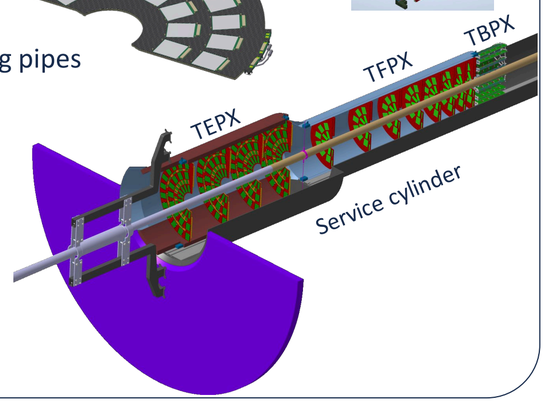
- Hybrid modules with 2 (1×2) or 4 (2×2) readout chips
- 3900 modules (1156 + 2736)
- 2×10^9 pixels
- 4.9 m^2

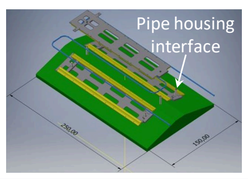
Mechanical structure

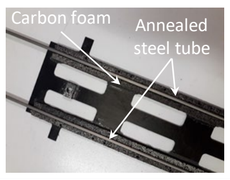
- Simple mechanics:
  - > Can be removed for maintenance
  - > Barrel splits in half at z ~ 0 (z != 0)
  - > Disks with planar geometry
- Light Carbon Fiber structures with embedded cooling pipes
- Features a two-phase -35°C CO_2 cooling system
  - > 1.8 mm OD stainless steel pipes
  - > 168 cooling loops
- 60kW power budget





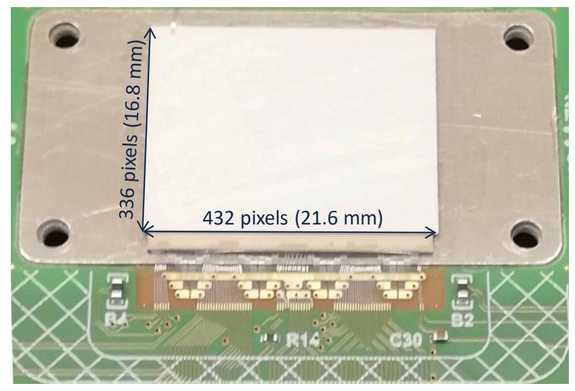






CMS Read Out Chip (CROC)

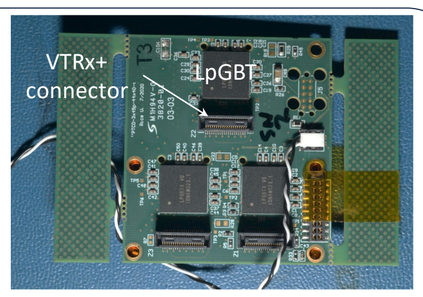
- CMS chip size (16.8×21.6 mm^2, 336×432 cells)
- 65 nm CMOS technology
- Dead time ≤1% @3.2 GHz/cm^2
- 1 Grad TID resistant
- Strongly protected against SEU effects
- 50×50 μm^2 cell
- Linear analog FE
- low threshold (≤ 1000 e-)
- High hit and trigger rate (up to 4×1.28 Gb/s output links)
- Serial powering capabilities



First wafer level test performed - Poster: Wafer level test of the readout chip of the CMS Inner Tracker for HL-LHC - Michael Grippo

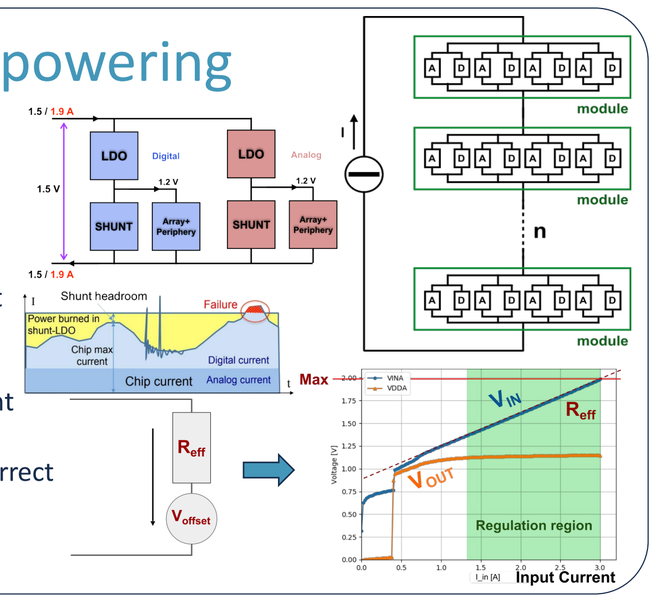
Services

- Portcards:
  - > 3 LpGBT
  - > 3 VTRX+
  - > 1 bPOL12V DC/DC converter
  - > 1 bPOL2V5 DC/DC converter
- Powering:
  - > Low voltage power with serial powering scheme over 576 chains
  - > High voltage distributed in parallel to modules in each serial chain
  - > ~ 350 pre-heaters meeded by cooling



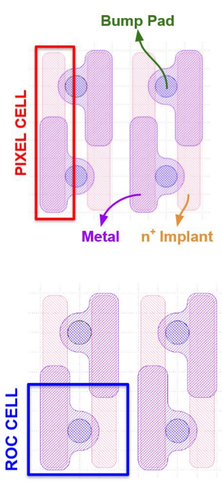
Serial powering

- Consecutive modules use the same current
- Current is shared in parallel between:
  - > ROCs in the same module (2 or 4)
  - > Analog and Digital domain on ROC
- Shunt-LDO:
  - > ROC IP block for serial powering support
  - > On chip solution
  - > Low mass, radiation hard, no extra ASIC
  - > Shunt functionality needed to implement the serial scheme
  - > LDO regulation needed to ensure the correct voltage to the electronics (~ 1.2 V)
  - > Equivalent to a resistor in series with a voltage source (R_{eff}, V_{offset})



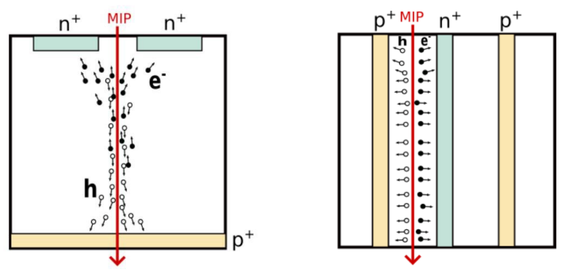
Sensors

- 25×100 μm^2 pixel cells
- 50×50 μm^2 bump bond pads
- Extensive R&D program
- Irradiations and test beams (CERN, Fermilab, Desy, FNAL)
- Simulations for geometry optimization
- Thin planar n-in-p sensors:
  - > 150 µm thickness
  - > Bitten implant, no punch-through bias dot
  - > Hit efficiency > 99% (after 2×10^{16} n_{eq}/cm^2)
- 3D pixel sensors on Barrel layer1:
  - > Lower high voltage power consuption
  - > Stable hit resolution up to 10^{16} n_{eq}/cm^2



Poster: Characterization of irradiated passive CMOS sensors for tracking in HEP experiments – Franz Glessgen

Poster: Study of irradiated 3D pixel sensors from CNM – Clara Lasaosa García



Poster: Performance of highly irradiated FBK 3D and planar pixel detectors – Rudy Ceccarelli