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A Silicon Vertex Detector with Timing for the Upgrade II of LHCb

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LHCb has recently submitted a physics case for an Upgrade II detector to begin operation in 2031. The upcoming upgrade is designed to run at instantaneous luminosities of $1.5 \times 10^{34} cm^{-2} s^{-1}$, to accumulate a sample of more than 300 fb^{-1}. The LHCb physics programme relies on an efficient and precise vertex detector (VELO). Compared to Upgrade I, the data output rates, radiation levels and occupancies will be about ten times higher during LHC runs 5 and 6. To cope with the pile-up increase, new techniques to assign b hadrons to their origin primary vertex, and to perform the real time pattern recognition are needed. To solve these problems, a new 4D hybrid pixel detector with enhanced rate and timing capabilities in the ASIC and sensor will be developed. This presentation will discuss the most promising technologies to be used in the future upgrade for the HL-LHC, with emphasis on the timing precision as a tool for vertexing in the next generation detectors. An initial simulation effort has been made to investigate what would be the required temporal resolution sufficient to mitigate pile-up and identify secondary vertices, which points to at least 20 ps per track. The most recent results from beam tests motivated by time measurements will be presented together with the R\& D scenarios for the future upgrade. Improvements in the mechanical design of the Upgrade II VELO will also be needed to allow for periodic module replacement. The design will be further optimised to minimise the material before the first measured point on a track and to achieve a fully integrated module design with thinned sensors and ASICs combined with a lightweight cooling solution.

Collaboration

LHCb

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