New results of the technological prototype of the CALICE highly granular silicon tungsten calorimeter

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Particle Flow Detectors at Higgs Factories

Basis: sep of H → WW/ZZ → 4j

– $\sigma_Z/M_Z \approx \sigma_W/M_W \approx 2.7\% \oplus 2.75\sigma_{sep}$

$\boxed{\Rightarrow \sigma_E/E \text{ (jets)} < 3.8\%}$

Large Tracker

– Precision and low X_0 budget

– Pattern recognition

High precision on Si trackers

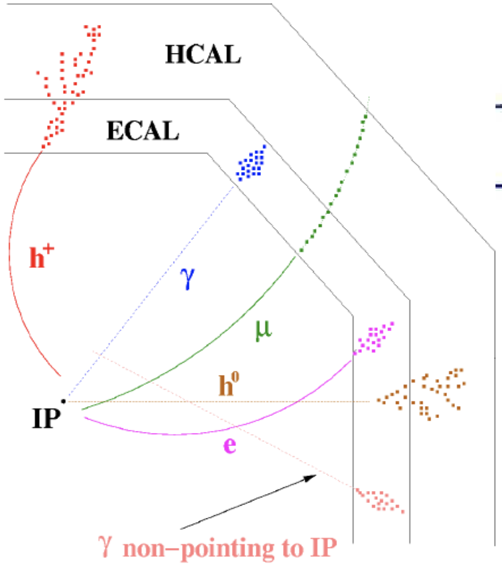
– Tagging of beauty and charm

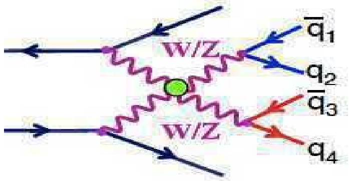
Large acceptance

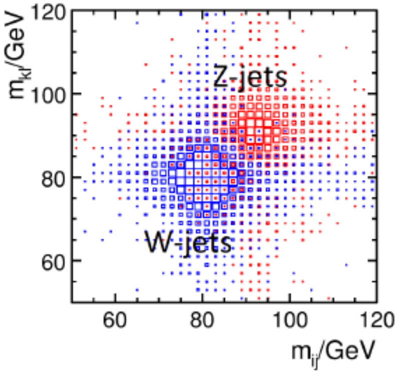
Fwd Calorimetry:

– lumi, veto, beam monitoring

Imaging Calorimetry







Particle Flow Algorithms :

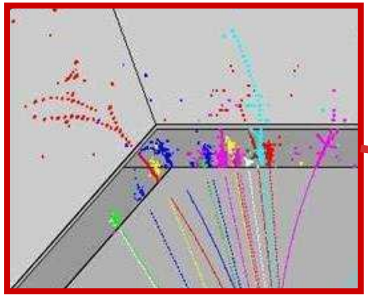
- Jets = 65% charged Tracks + 25% γ ECAL + 10% h^0 CALO's
- TPC $\delta p/p \sim 5 \cdot 10^{-5}$; VTX $\sigma_{x,y,z} \sim 10\ \mu m$ Particle ID

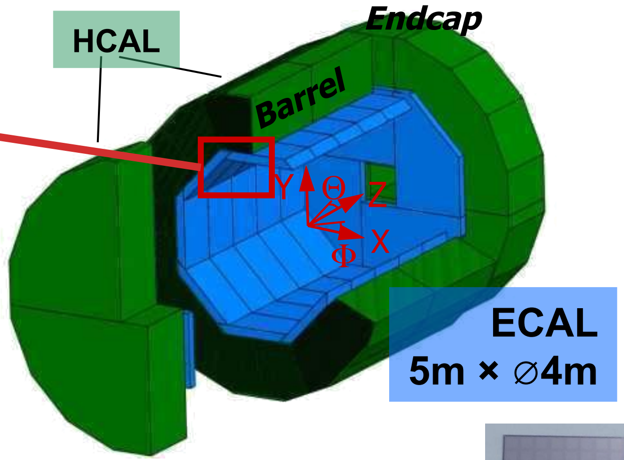
H. Videau and J. C. Brient, “Calorimetry optimised for jets,” (CALOR 2002)

Particle Flow ECAL should :

spot tracks & showers from charged ($h^\pm$, $e^\pm$)
measure Photons in jets & Tau physics (γ vs π_0)
measure 2/3 of neutral hadrons interacting in the ECAL
measure Time-of-Flight (10’s ps)

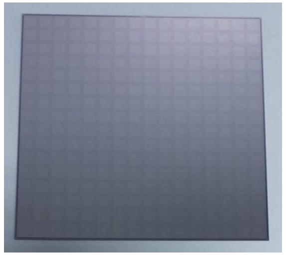
An Ultra-Granular SiW-ECAL for Higgs Factories

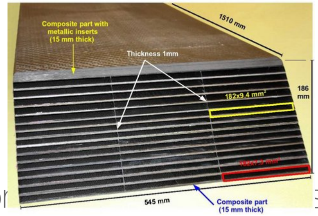




Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability (*E, (θ,φ), t*)
- PFlow requirements:
  - Extremely high granularity : **5×5 mm² × 30 layers**
  - Compacity (density)
- Technical requirements:
  - Electronics & Service Integration (power, cooling, …)
  - Scalability : **$\mathcal{O}$(100M) channels ⇒ $\mathcal{O}$(100k) boards**



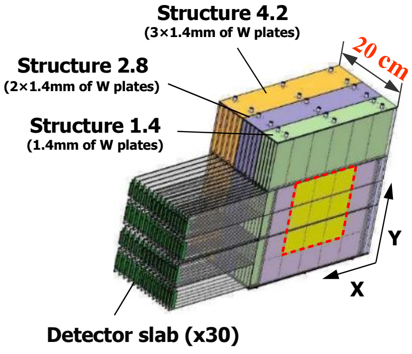


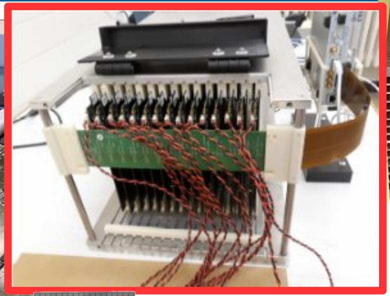
SiW+CFRC baseline choice for future Lepton Colliders:
(ILC/ILD, CLIC/det, FCC-ee/CLD, CEPC/Baseline)

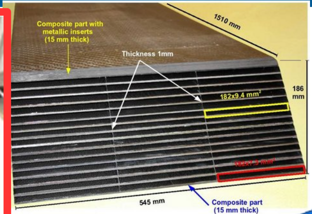
- Tungsten as absorber material
  - X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - **Support compact design: Sensor+RO≤2mm**
    - **Integration with Very-Front End Electronics**
  - Allows for ~any pixelisation
  - Robust technology
  - **Excellent signal/noise ratio: ≥10**
  - **Intrinsic stability (vs environment, aging)**
  - **Albeit expensive…**
- Tungsten–Carbon alveolar structure
  - **Minimal structural dead-spaces**
  - **Scalability**

To be assessed by prototypes

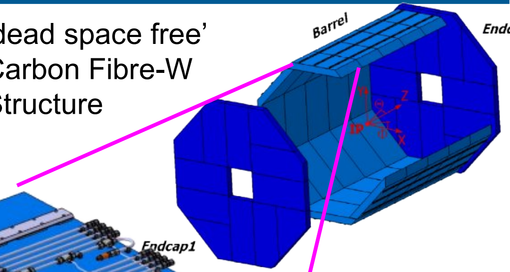
CALICE prototypes for ILC

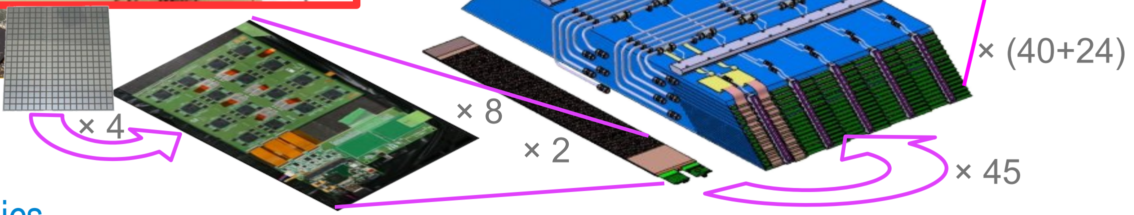






‘dead space free’ Carbon Fibre-W Structure





Physical (2005-11)

- 1×1 cm² on 500µm 6×6 cm² Pad glued on PCB Floating GR
- × 30 layers (10k chan).
- External readout
- Proof of principe

Technological (now)

- Embedded electronics
  - Power-Pulsed, Auto-Trig, delayed RO
  - S/N = (MPV/σ_{Noise}) ≥ ~12 (trig)
- Compatible w/ 8+ modules-slab
- 5×5 mm² on 320–650µm 9×9 cm² × 26–30 layers
  - 8k (slab) ~ 30k (calo) channels

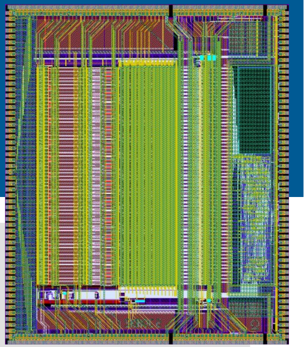
We are here

Pilote (2027?) ➡ Full Det (2035?)

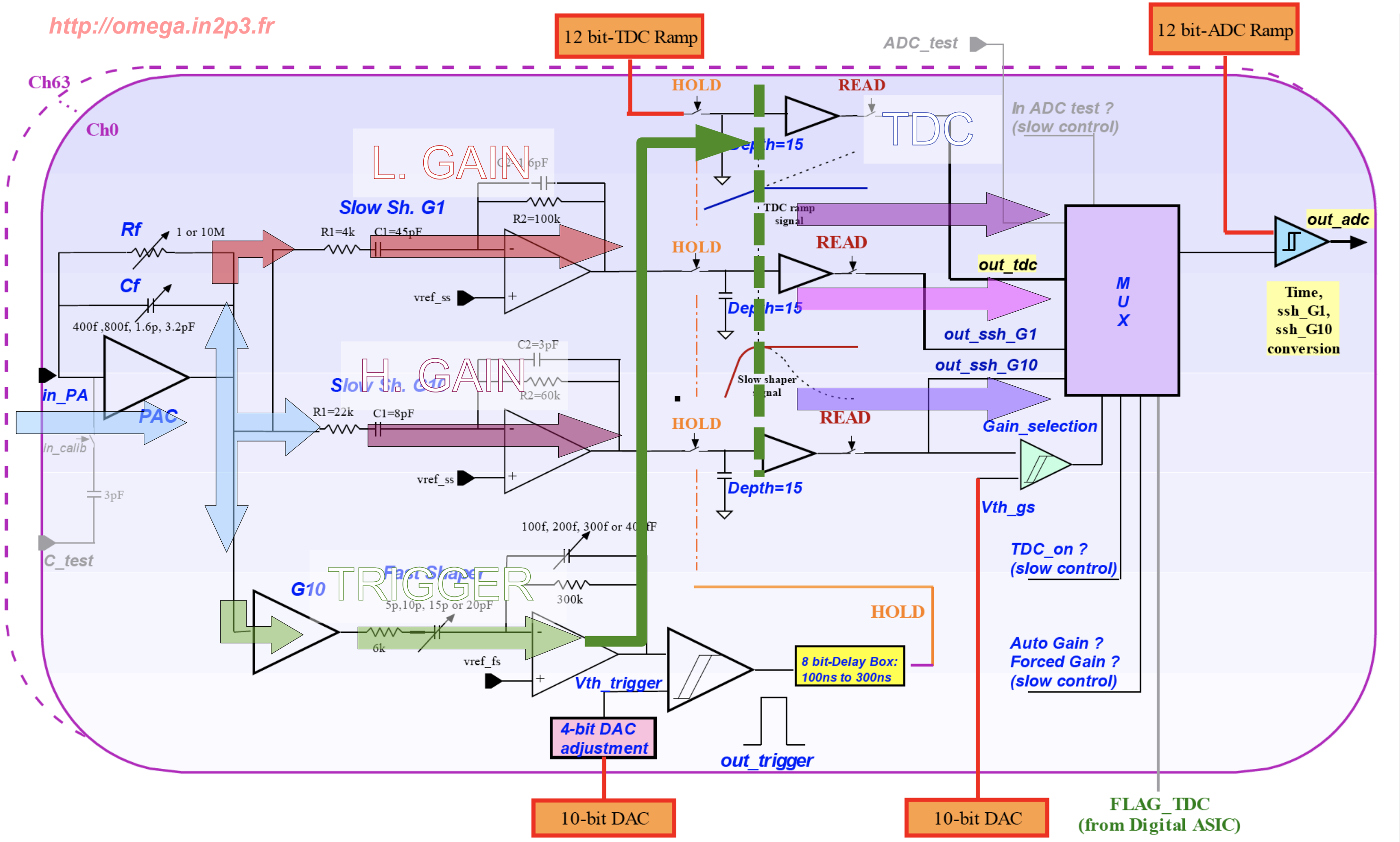
- 1M ➡ 70M channels
- on 750µm 12×12 cm² 8” Wafers ?
- Pre-industrial building
- Full integration (⊃ cooling)
- Final ASIC (Ωmega SK3 ?)

30 years

SKIROC2 / 2A Analogue core



http://omega.in2p3.fr

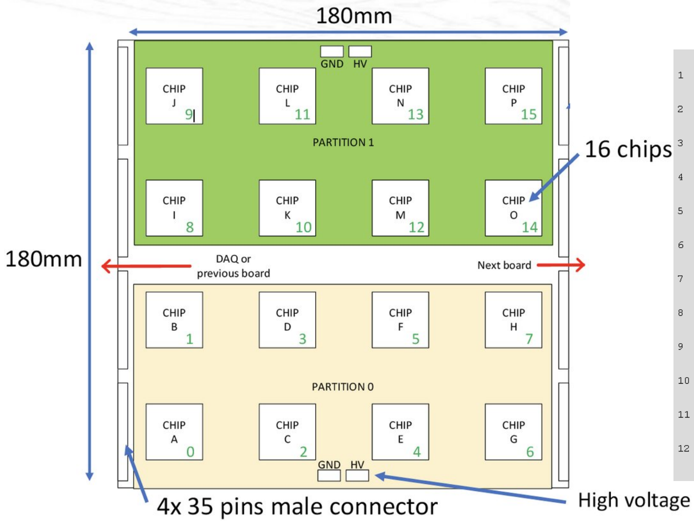


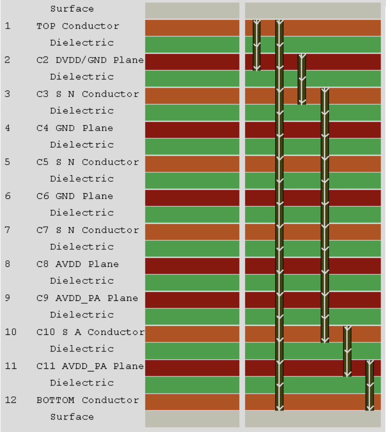
- **64 channels**
- **Auto-triggered**
  - per cell adj.
  - 1 cell triggers all
- Preamp
  \+ 2 Gains + Auto-select
  \+ TDC (~1.4ns)
- 15 (×2) analogue memories
- Dyn range 0.1 ~ 2500 mips
  - mip in 320 µm (4 fC)
  - 12 bits ADC's
- *616 config bits*
- Low consumption
  - 25 µW/ch with 0.5% ILC-like duty cycle
- Power-Pulsed

FEV's : 15 years of R&D

Most complex element:
electro-mechanical integration

- Powering, Distrib / Collect signals from ASICs, Analog & Digital with dyn. range ≥ 7500
  - Single End operation ➞ Chaining for 8–10 boards
- **Mechanical** placer & holder for Wafers
  ➞ ≤ 50μm lateral precision, flatness
- **Thickness** constraints ➞ Calorimeter Compactness



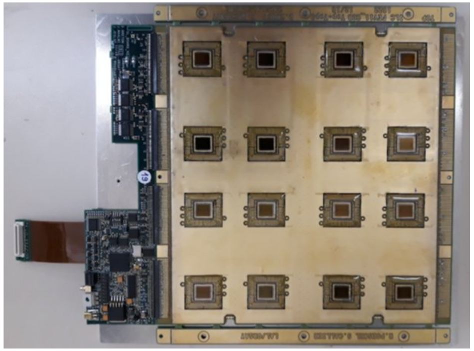


Milestone	Date	Object	Details	REM
1st ASIC proto	**2007**	SK1 on FEV4	36 ch, 5 SCA	proto, ≤ 2000 mips
1st ASIC	2009	SK2	64ch, 15 SCA	3000 mips
1st PCB proto	**2010**	FEV7	8 SK2	COB
1st working PCB	2011	FEV8	16 SK2 (1024 ch)	CIP (QGFP)
1st working ASU in BT	**2012**	FEV8	4 SK2 readout (256ch)	S/N ≤ ~ 14 (H Gain), no Power Pulsing retriggers 50–75%
1st run in PP	2013	FEV8-CIP		BGA, Power Pulsing
1st full ASU	**2015**	FEV10	4 units on test board 1024 channel	S/N ~ 17–18 (H Gain) retrigger ~ 50%
1st SLABs	2016	FEV11	10 units	Noise issues
pre-calo	**2017**	FEV 11	7 units	S/N ~ 20 $(12)_{\text{Trig,}}$ 6–8 % masked
1st technological ECAL	2018	FEV11, 12 13 Compact Calo Long Slab	SK2 & SK2a (⊃timing) 8 ASUs	Improved S/N Timing enabling
1st working COB, new DAQ	2019	FEV-COB	2×1/4 ASUs Cont. power.	Technical
2nd tech ECAL	20–22	5 types FEV's	H. Gain, Cont. Power	320, 500, 650 μm

Present ‘FEV-zoo’

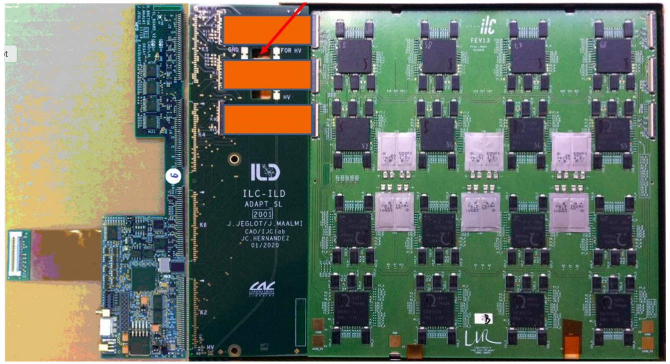
FEV10, 11, 12

- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main “Working horses” since 2014



FEV-COB

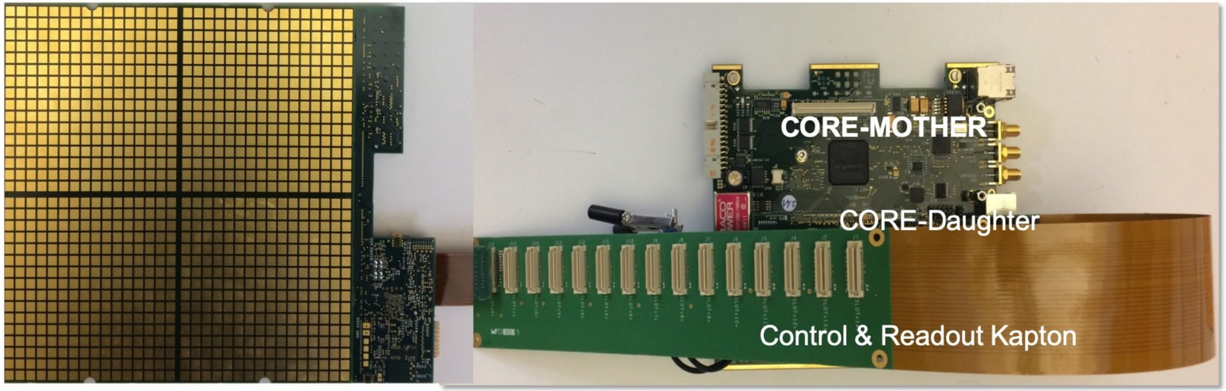
- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible



FEV13

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

Compact DAQ readout

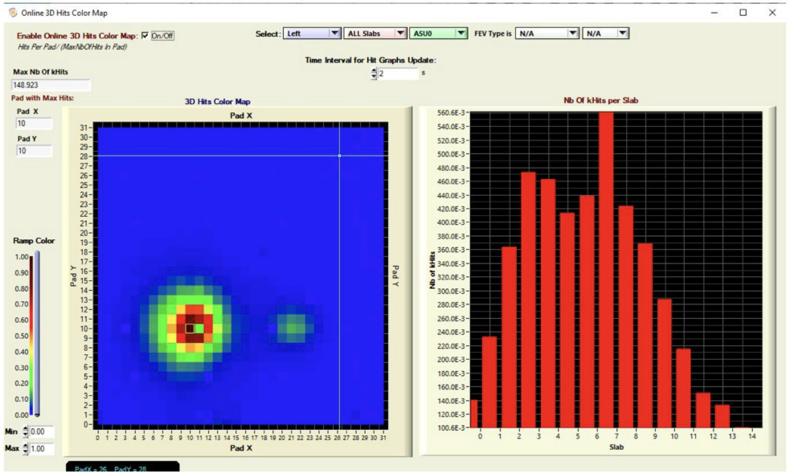


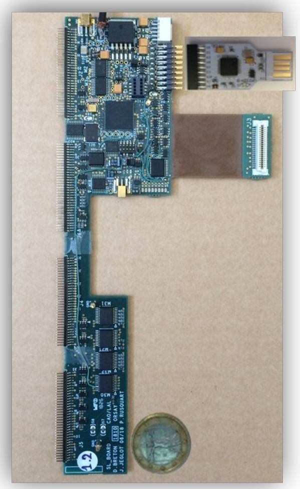
“Dead space free” granular calorimeters
➡ ~ 30 mm space ECAL–HCAL

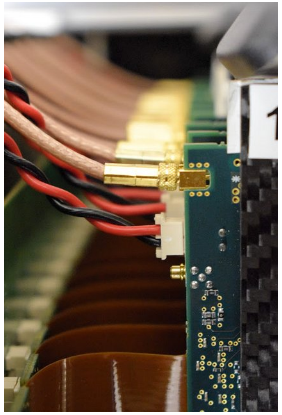
- Compact DAQ
- in use in BT since 2019

LabWindows + scriptings

- Full debug system
- ↔ EUDAQ
  - Combined running



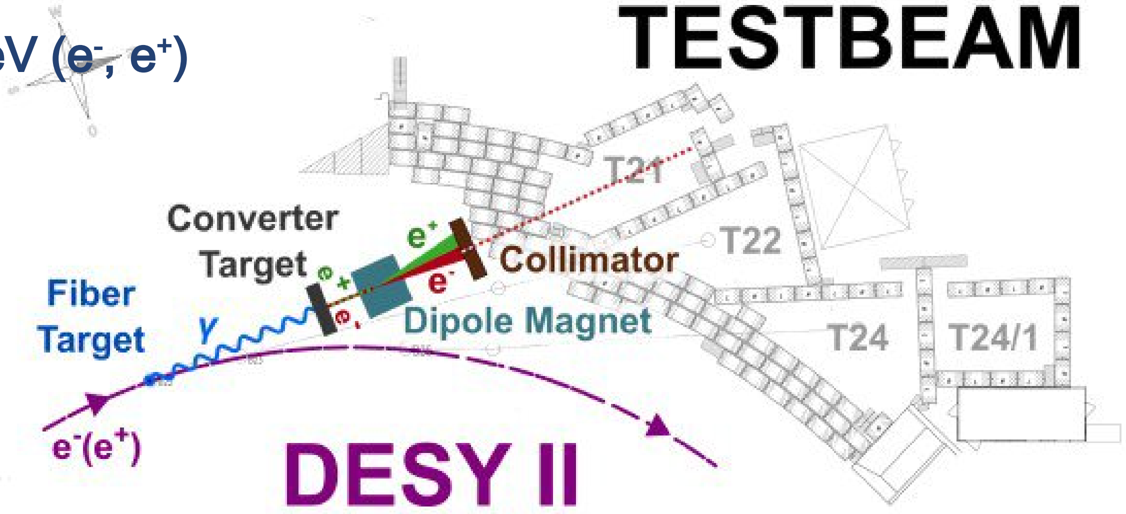




Beam Test at DESY-II Nov. 2021 + March 2022

DESY offers low-energetic beams of 1–6 GeV (e^-, e^+)

– 15 layers with 1024 readout cells each
  - 5.5 mm Si pads



The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

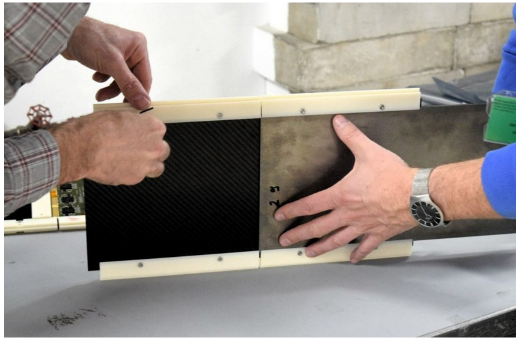
4 weeks in total

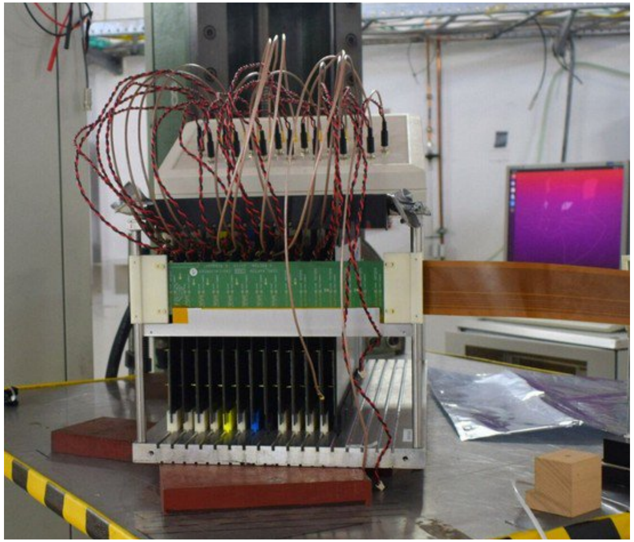
– ~3 weeks of commissioning and “training”
  - Mechanical structure (adding or removing the tungsten plates)
  - New and continuously improving DAQ and online monitoring tools
  - New semi-online monitoring tools
  - Hold values, gain optimization, Threshold optimization, single cell calibration, etc

Prototypes

November 2021

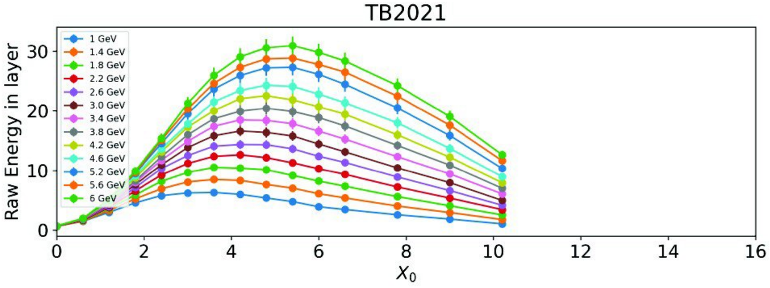
- Tungsten absorbers :
  11 × 2.1 mm (0.6 X_0)
  + 3 × 4.2 mm (1.2 X_0)
  total 10.2 X_0

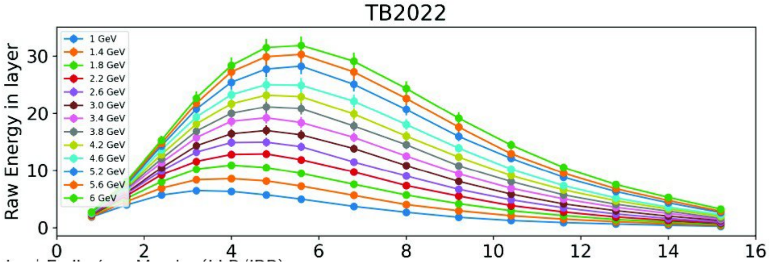


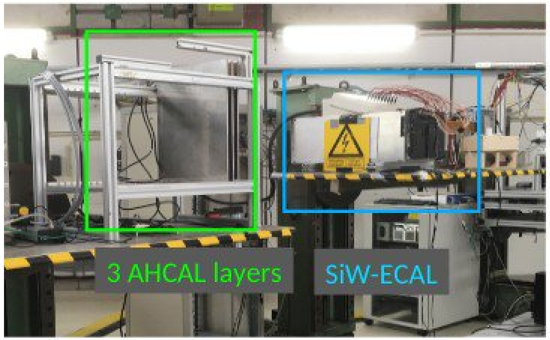


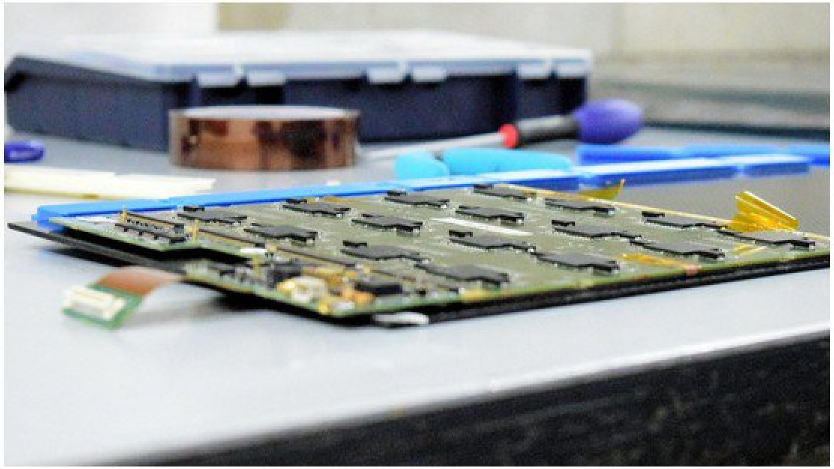
March 2022

- Tungsten absorbers :
  7× 2.8 mm (0.8 X_0)
  + 8 × 4.2 mm (1.2 X_0)
  total 15.2 X_0



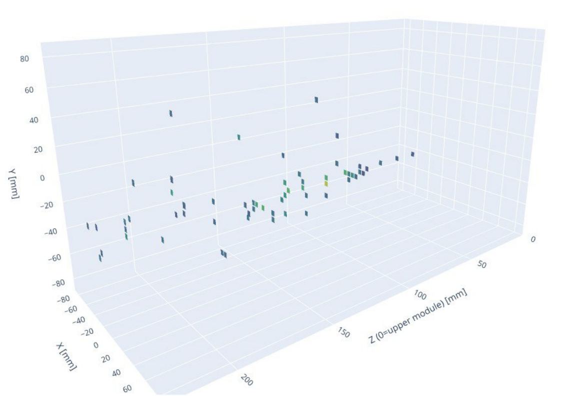







Hochspannung
Lebensgefahr
Danger
High voltage!

Noise studies



3 GeV electron shower

SKIROC2

- 1 hit (E_{chan}≥Thr.), 64 readouts
- Sparse showers ➡ many noise cells

Coherent vs Incoherent noise sources

- https://arxiv.org/pdf/1401.7095.pdf

Coherent noise source identification in multi channel analysis

T. Frisson*[1] and R. Poeschl[1]

[1]Laboratoire de L'accélerateur Linéaire (LAL), CNRS/IN2P3, Orsay, France

Analysis of collective Gaussian noise sources by correlation between channels

$$\sigma_i^2 = \sigma_{I_i}^2 + \sum_{j=1}^{N_c} \sigma_{C_i^j}^2 \quad (1)$$

The covariance matrix element from the two channels i and k is expressed by:

$$cov(i,k) = \delta_{ik}\sigma_{I_i}\sigma_{I_k} + \sum_{j=1}^{N_c} \sigma_{C_i^j}\sigma_{C_k^j} \quad (2)$$

where:

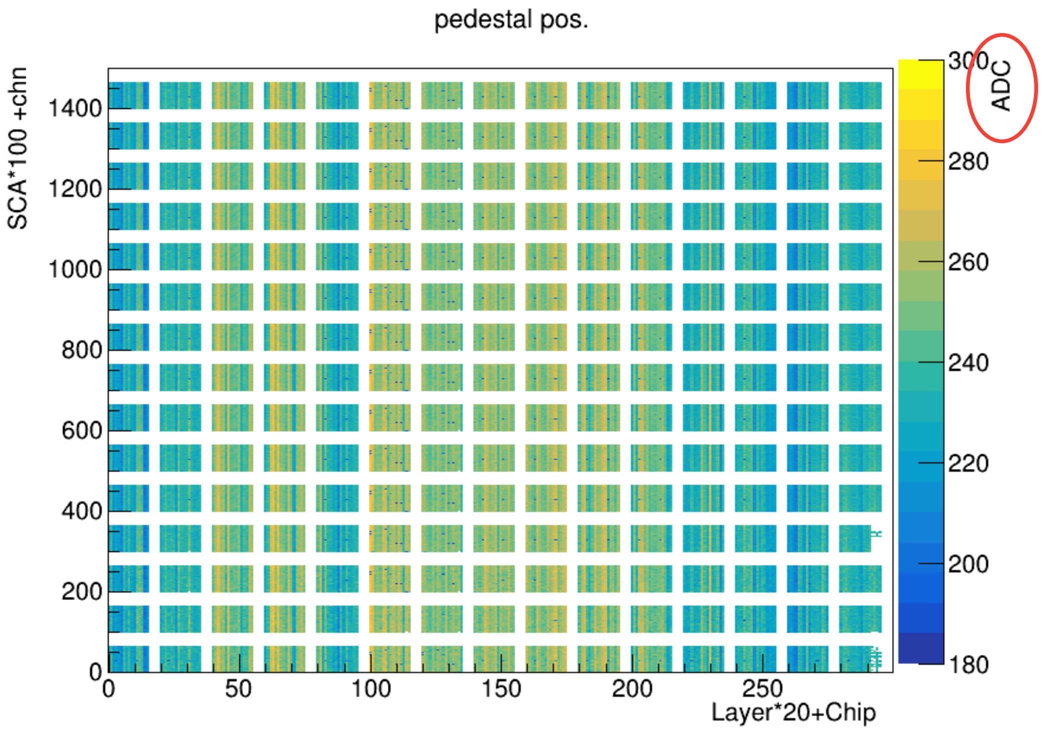
$$\delta_{ik} = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \quad (3)$$

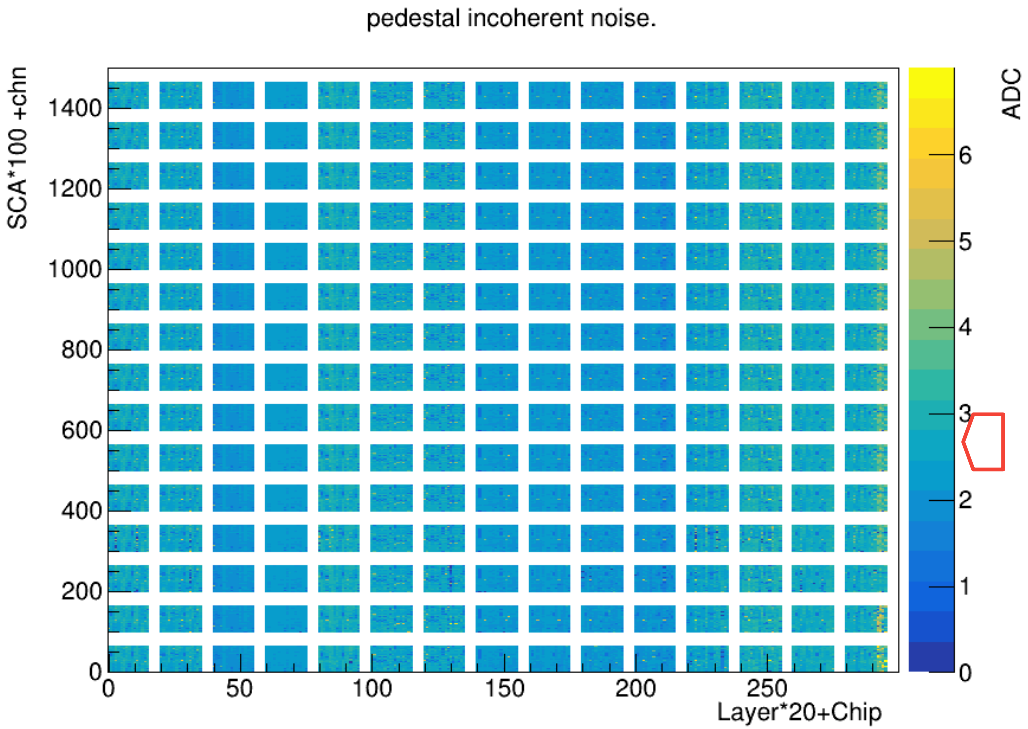
The covariance matrix element can also be determined from the data:

$$cov_{Data}(i,k) = \frac{\sum_{n=1}^{N_{event}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{event}} \quad (4)$$

15 layers ×1024 ch ×15 mem = 230k fits

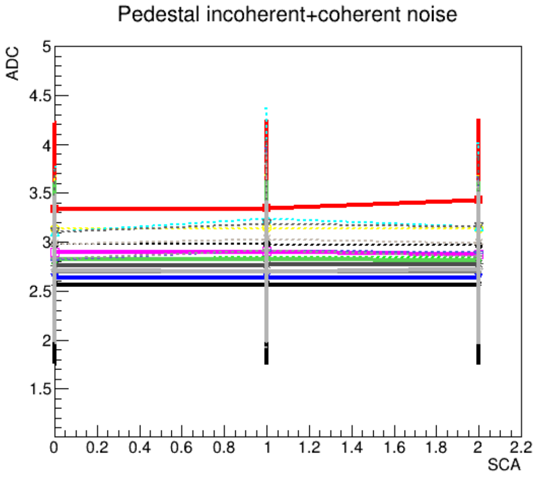
MIP ~ 70–140 adcc



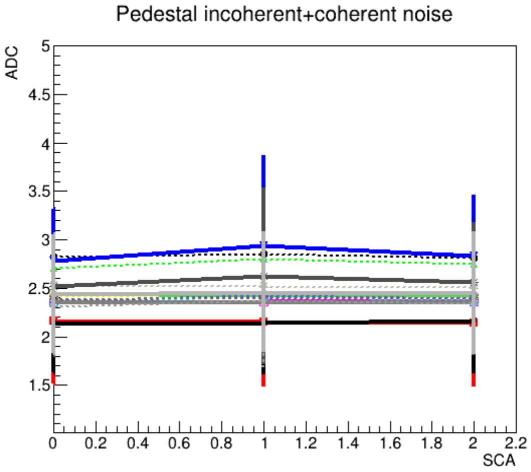


Pedestal widths, 1st memory cells, per asic

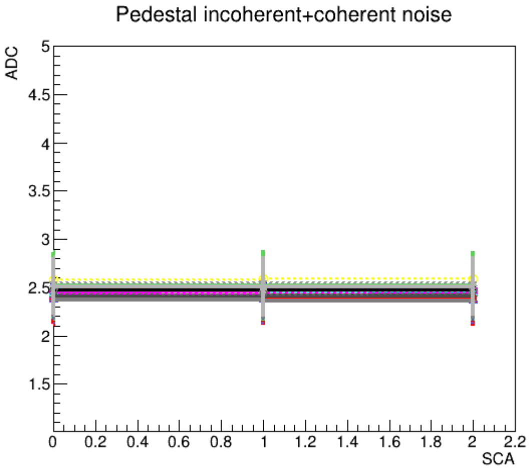
COB



FEV12

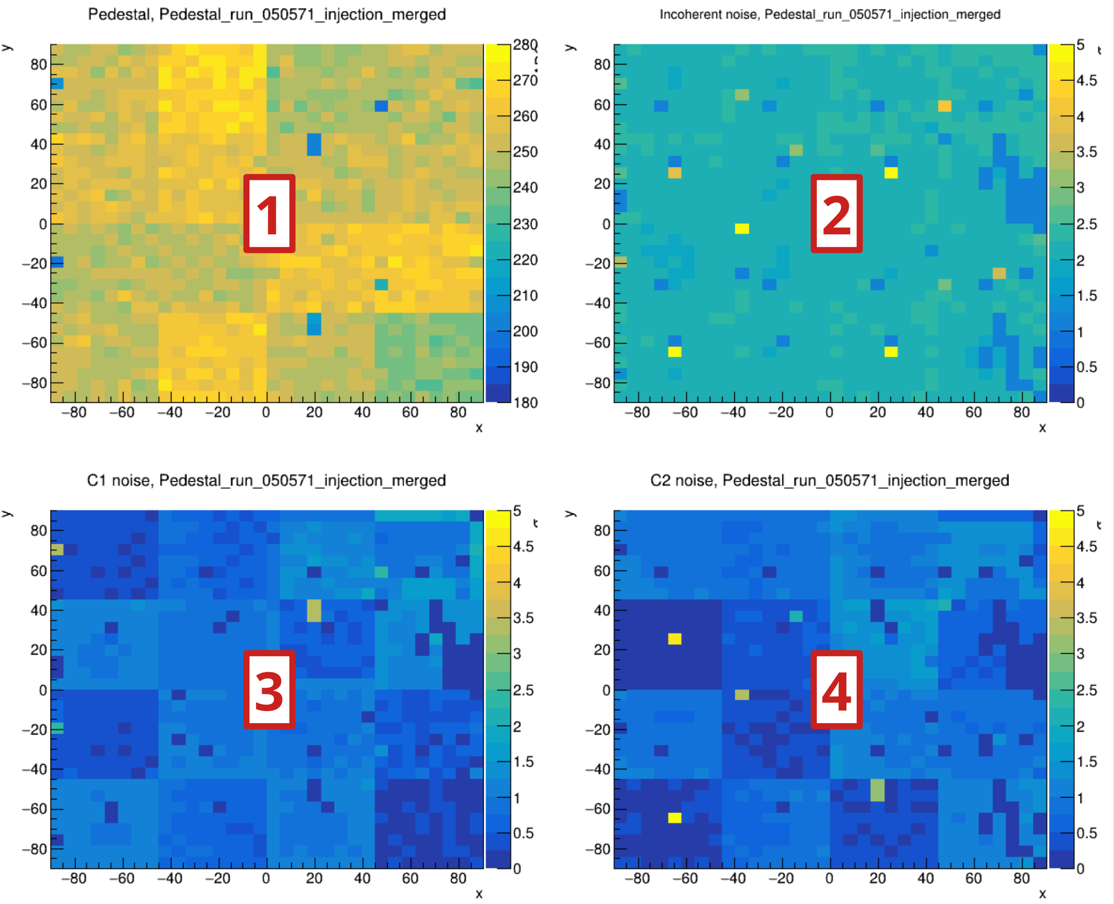


FEV13



- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors

Layer 7: FEV12 SK2a, 500 µm



Legend

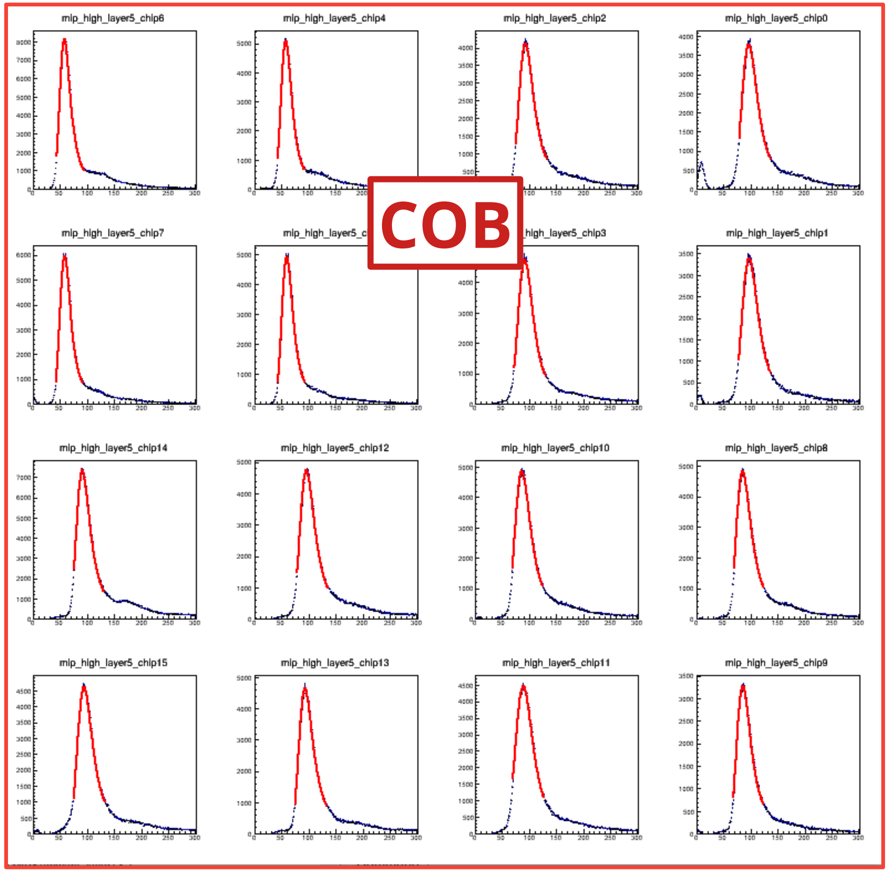
- 1) Pedestal map
- 2) Incoherent noise map
- 3) coherent noise map (c1)
- 4) coherent noise map (c2)

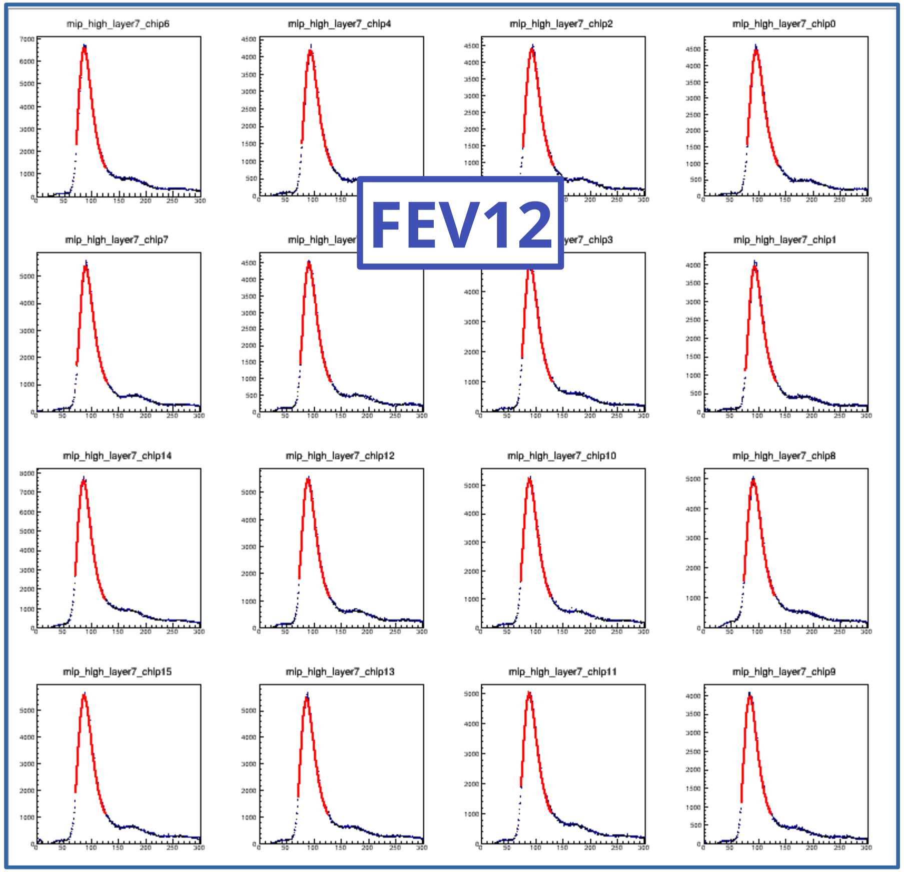
Outcomes:

- Few channels are off
  - These are usually seen as noise sources (FEV10/11/22)
- Routing issues
  - addressed in next generation

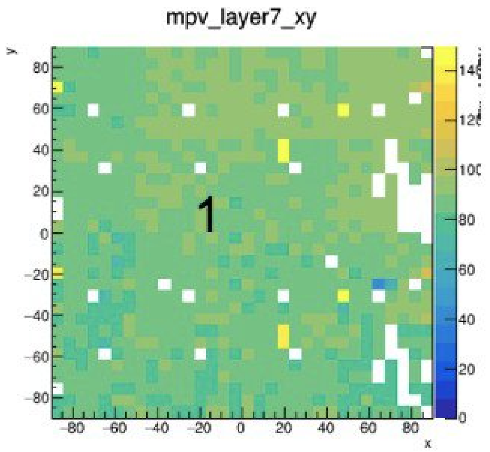
Reminder: Noise is THE enemy of local self-triggering with local storage FE readout.

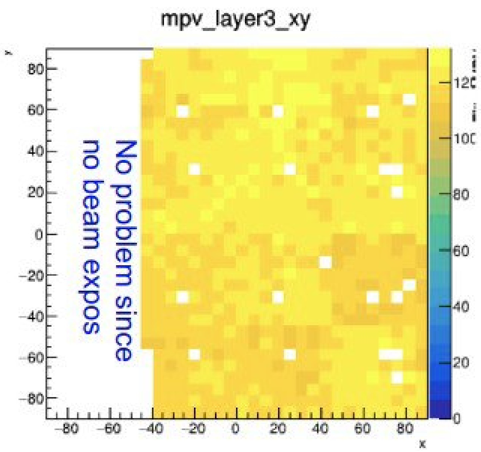
Mips response : no tungsten



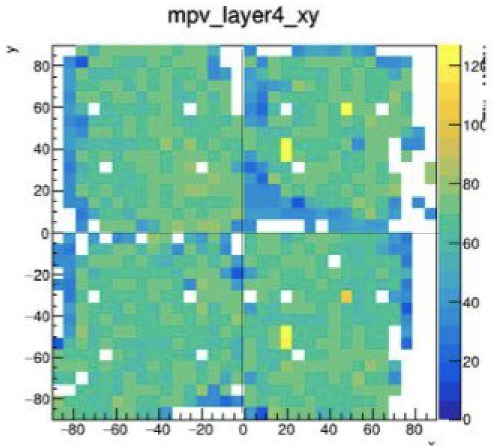


MIP calibration





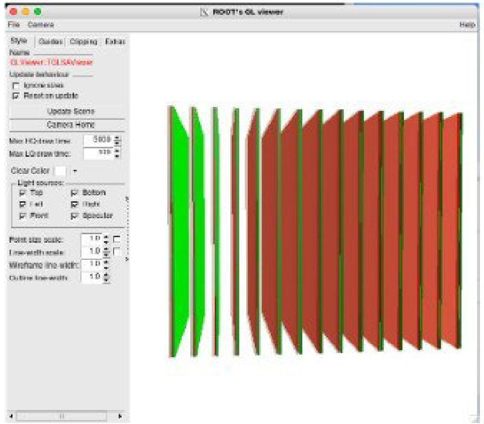
- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected



... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => <u>major</u> debugging tool
- In any case less good layers will be replaced in coming months

Simulation

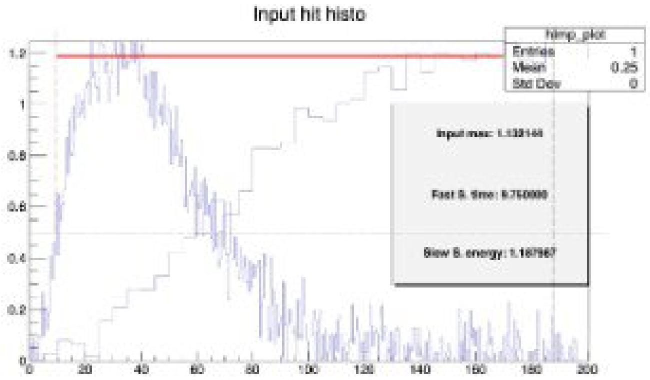


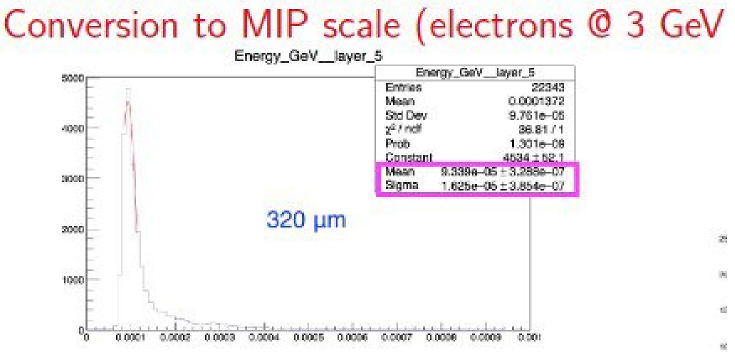
Done in DD4HEP framework (G4 overlayer)

- very flexible XML configuration
- derived from ILC soft

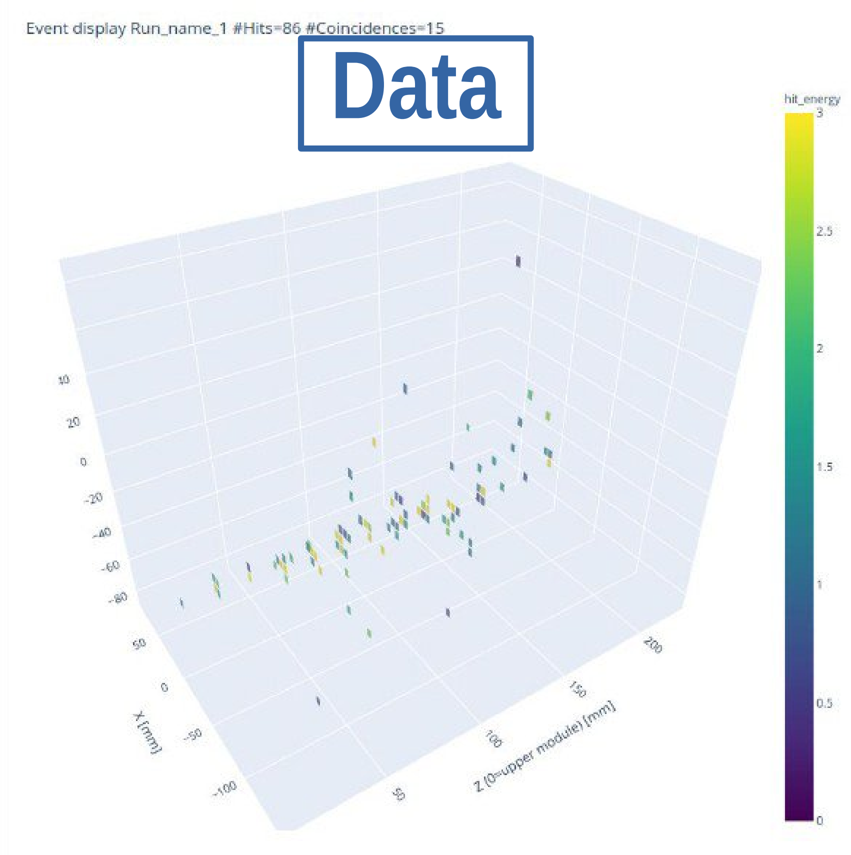
Digitization:

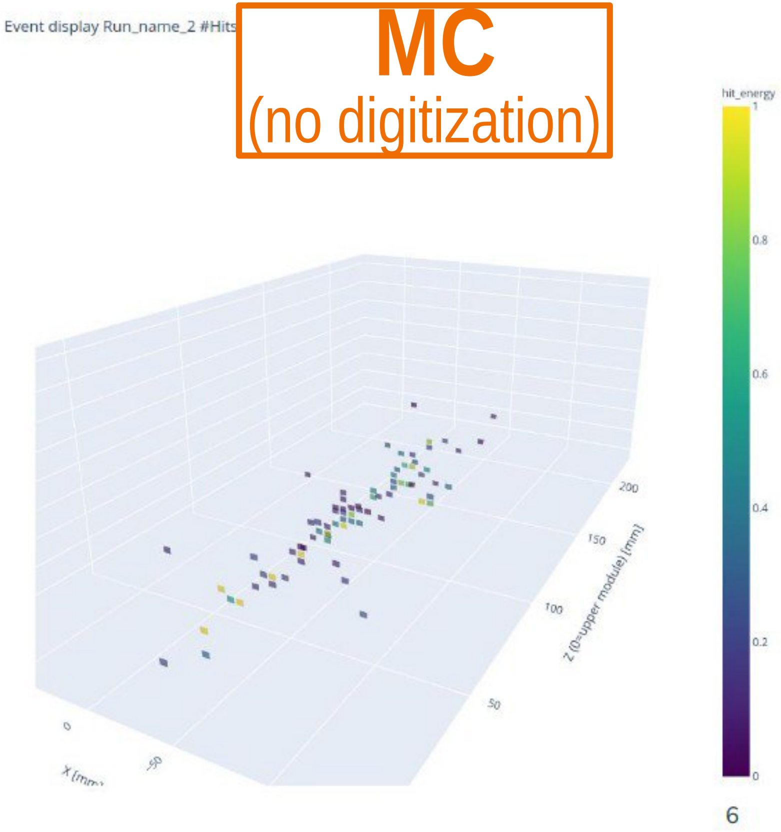
- Mimicking of the SKIROC2 ASICs
- Shaping in Fast and Slow Branch
  - MIP calibration in both branches
    - as in data
  - Application of thr. on Fast B,
  - ➡ Delay for Slow B. readout
- Parameters being adjusted on data



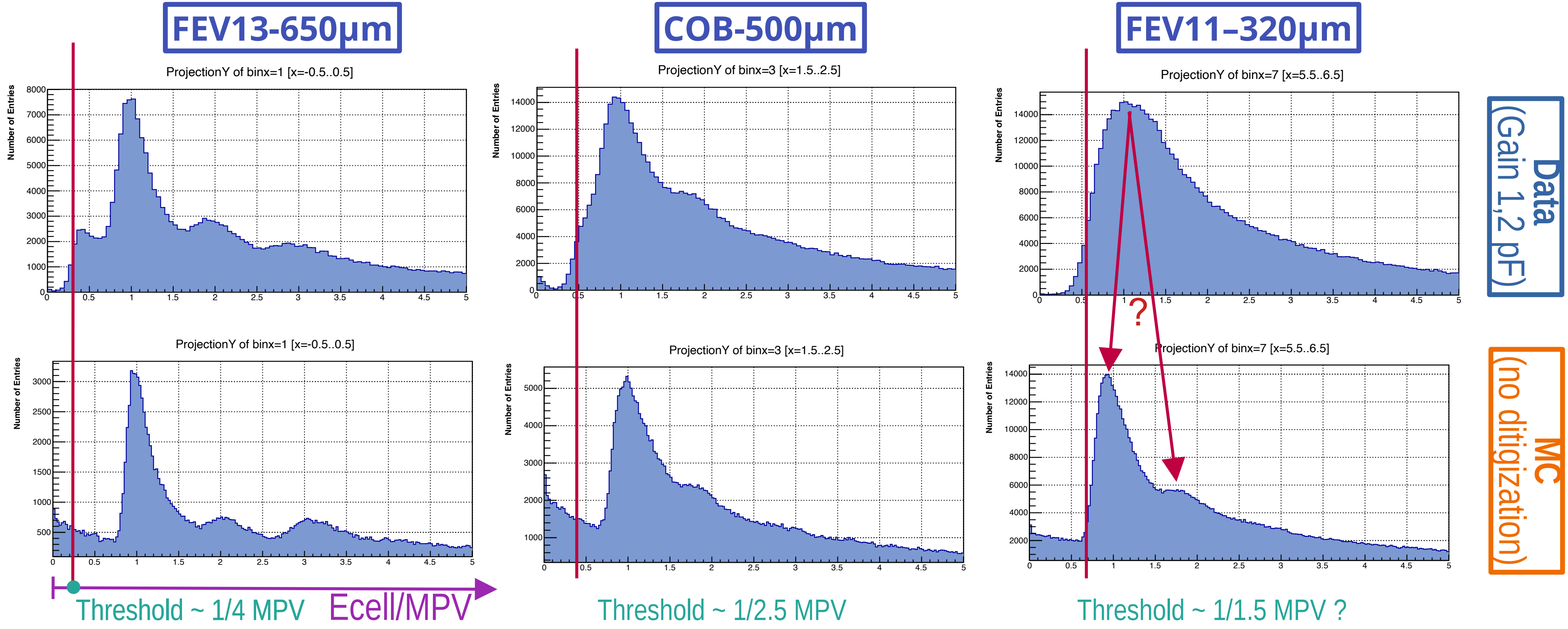


Electron Showers



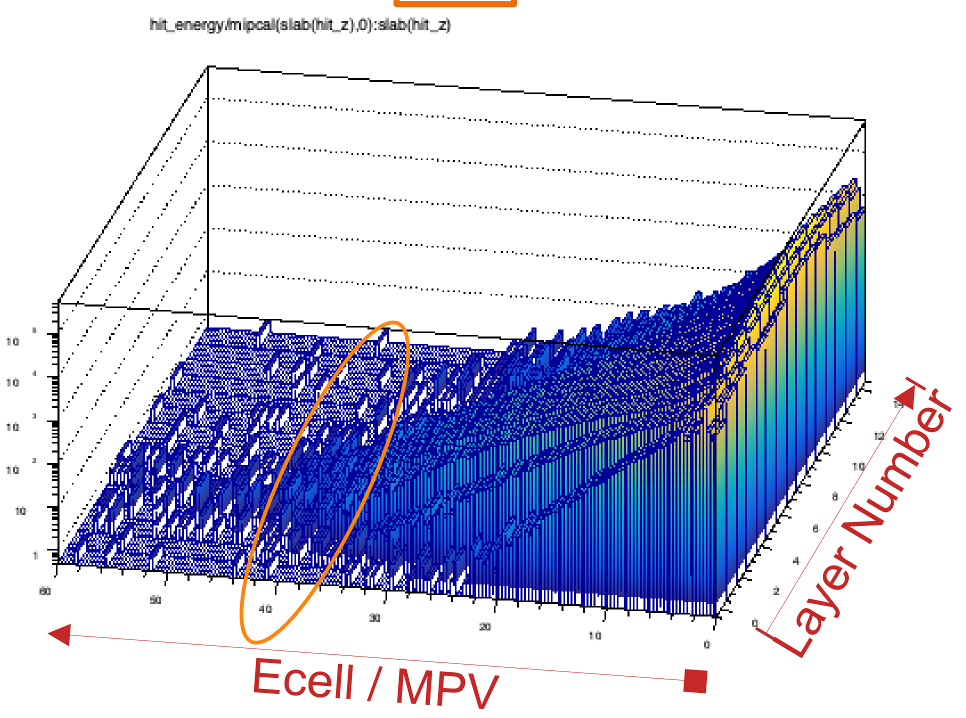


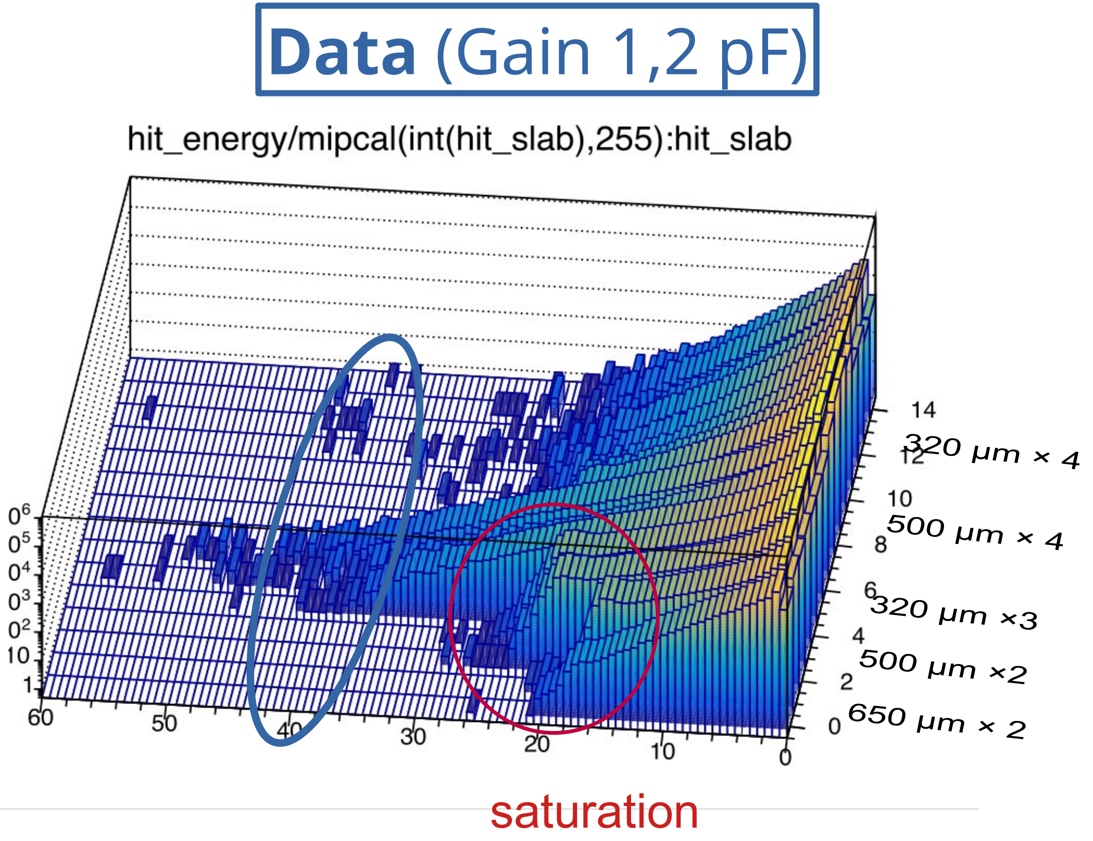
First look at in-shower spectrums (3 GeV)



MIP & Threshold calibration in-shower possible **… but requires a level of noise performance**

3 GeV Raw Hit Shower profiles – in High Gain

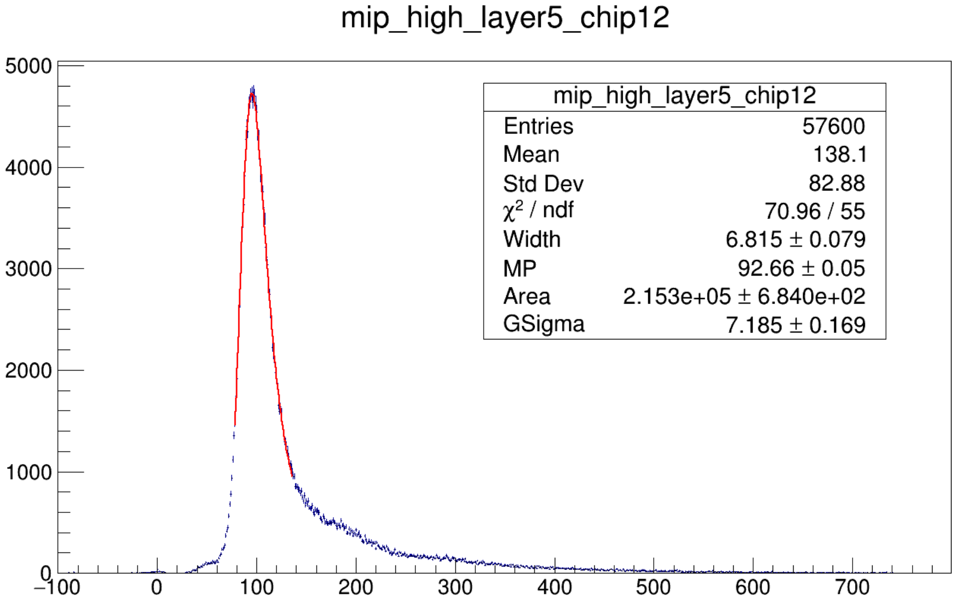




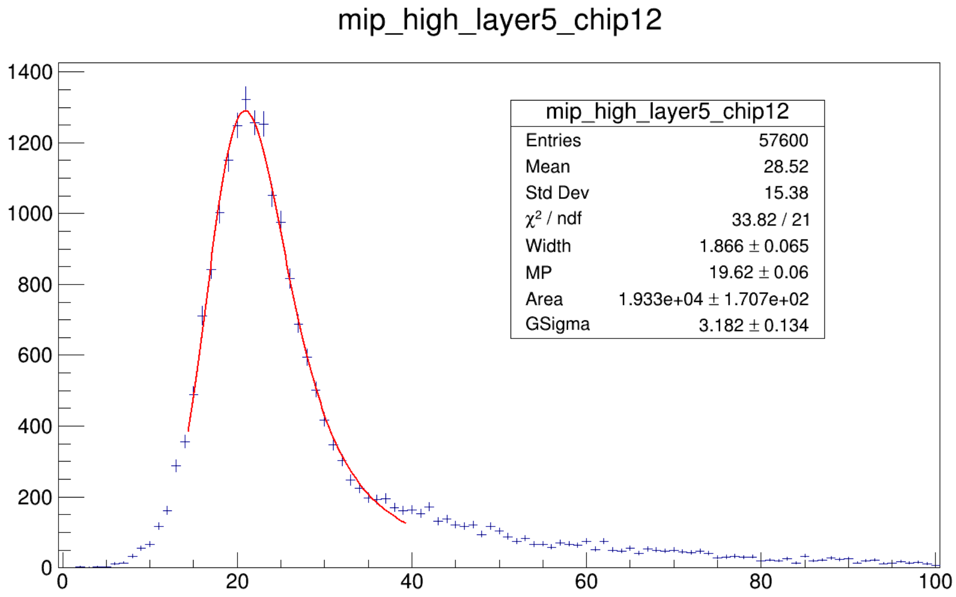
Escale → ≤ ~40 mips / cells

Gain adjustment

DESY (Ee ≤ 6 GeV)
(Gain 1,2 pF)



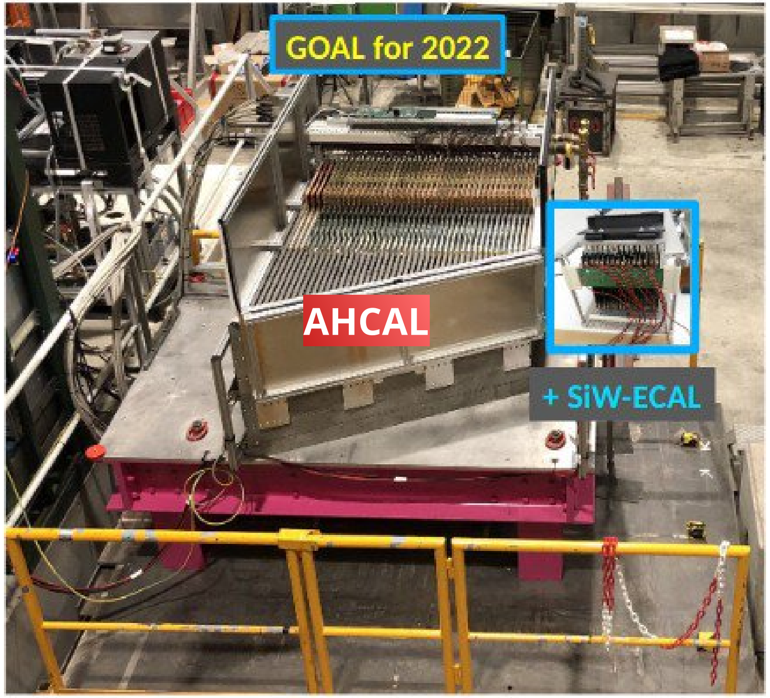
CERN, ILC (Ee ≤100 GeV)
(Gain 6 pF)



Preamplifier Gain 1.2 pF / 6 pF ~ × 4.73

Next steps

Beam test at CERN (June 22)



Preparation:

- Integration of more FEV13
- Commissioning with 6pF
  - Cosmics data taking on-going
- Increased W integration : 18.4 X_0

Finalising and testing the design of next gen FEV

- Improvement on power and signal routing
  ➡ better chaining, less induced noise
  ➡ more flexibility

Outlook

First Beam Tests (after 2 years of COVID)

- 1st test of a complete stack of the SiW-ECAL:
  - 15 layers (albeit heterogenous)
  - Two set-up 10.2 X_0 and 15.2 X_0

Training and Running phase

- New Compact DAQ (15 layers)
- Thin design (COB) operationnal
- Noise and Gain optimisations on particules

Most Layers operated as expected

- some noiser, some quieter
- Signs of conductive glue aging (wafer-PCB)

Low energy electrons:

- Punch-though ➡ MIP spectrums
  - MIP Calibration on-going
- Electron showers structure
  - First plots of resolution (not shown):
    - Correction of defects (masking, aging) need to be integrated.

To come:

- Adiabatic Increasing difficulty (Gain↘, Compactness↗)
- High Energy electrons (and Hadron): CERN June 22
- New FEV, with BGA design

Thank you for you attention

Thanks to
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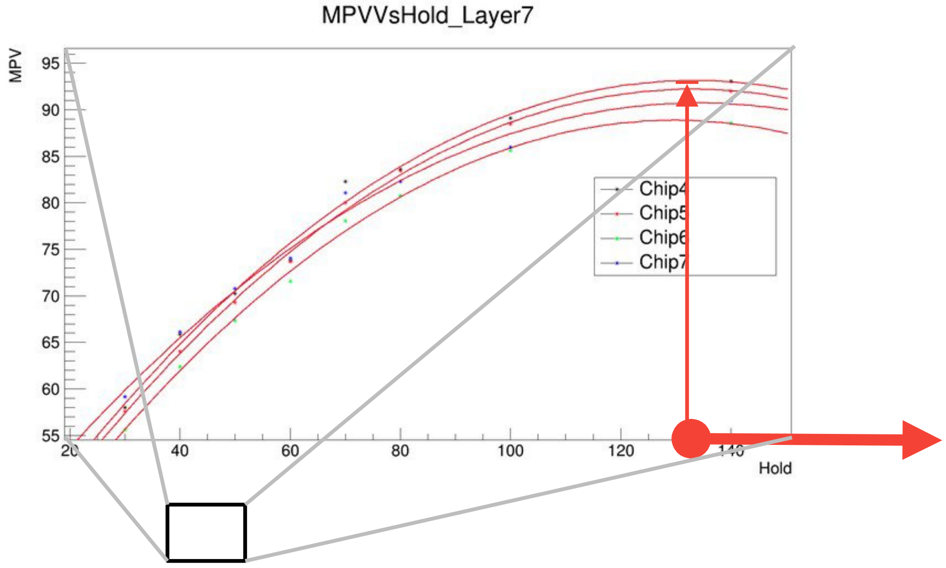
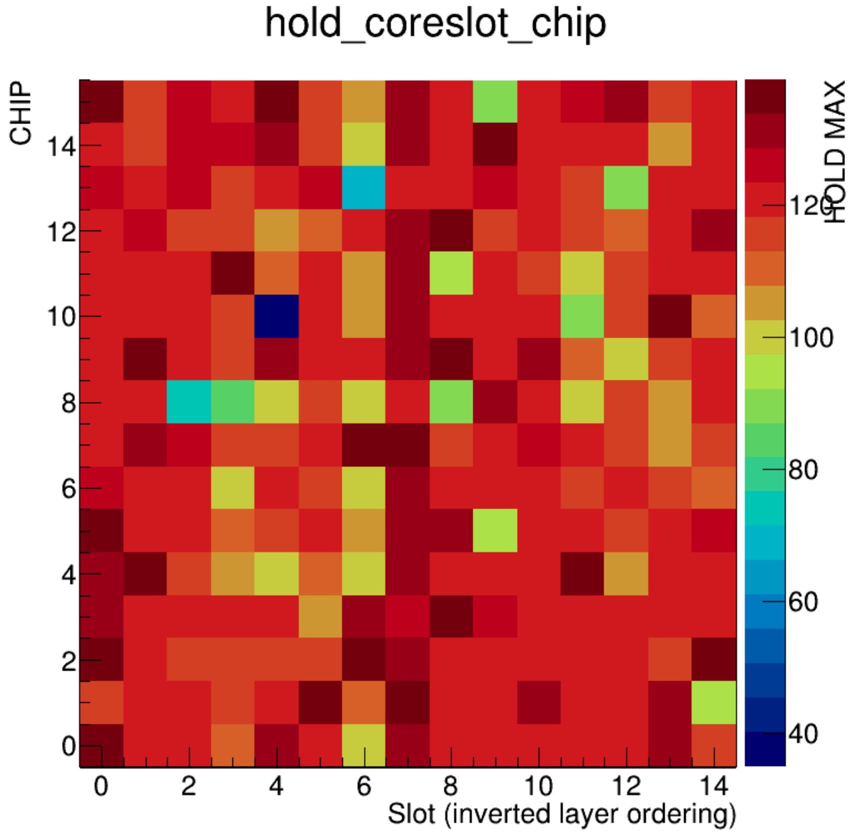
A. Irles, R. Poeschl, T. Suehara, S. Callier and many others
for material and inspiration for this talk

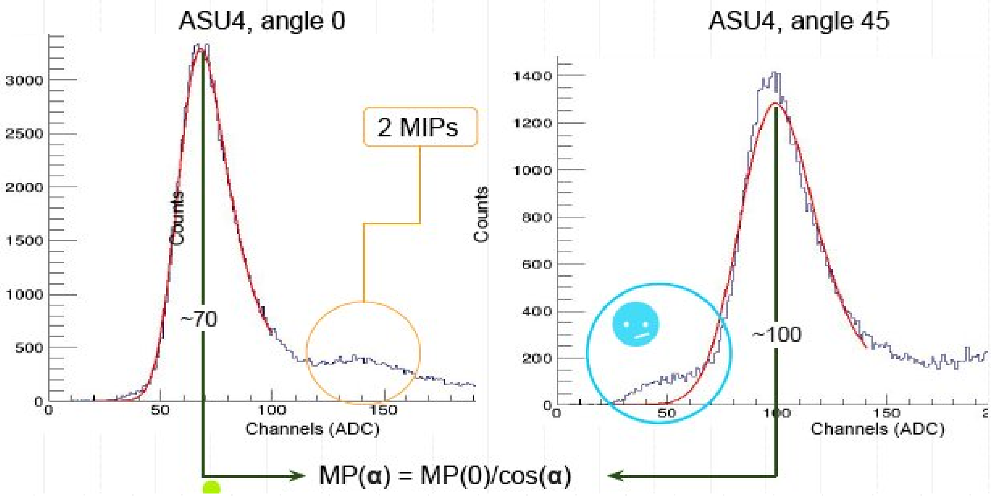
Thanks to the engineering teams of IJCLab, LPNHE and LLR
and to the Beam Test coordinators at DESY

Detector Commissioning on MIPs: max of shape

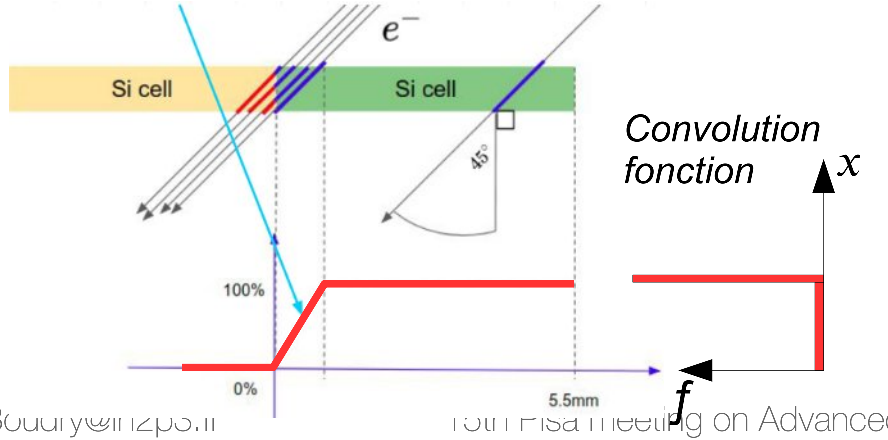




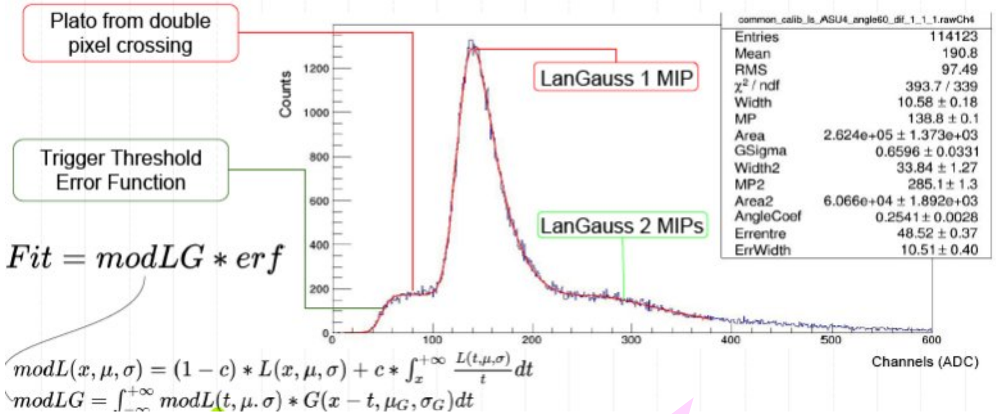
Mip analysis

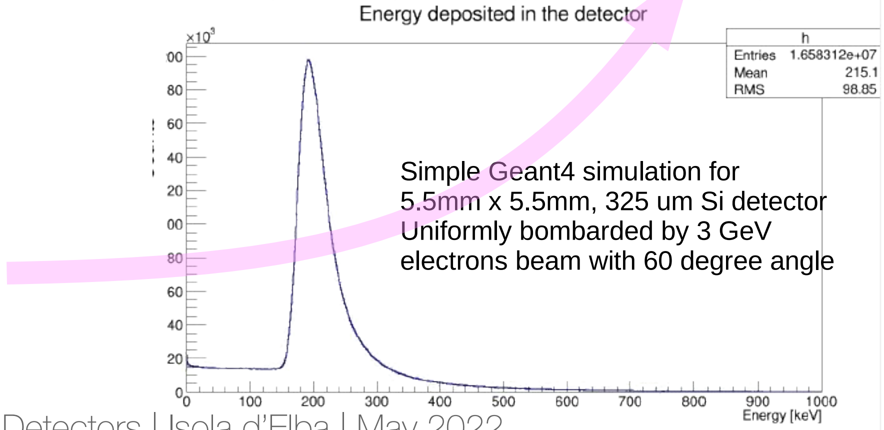


Pixel energy fraction depends linearly on crossing position



Fit with Mod LanGau function



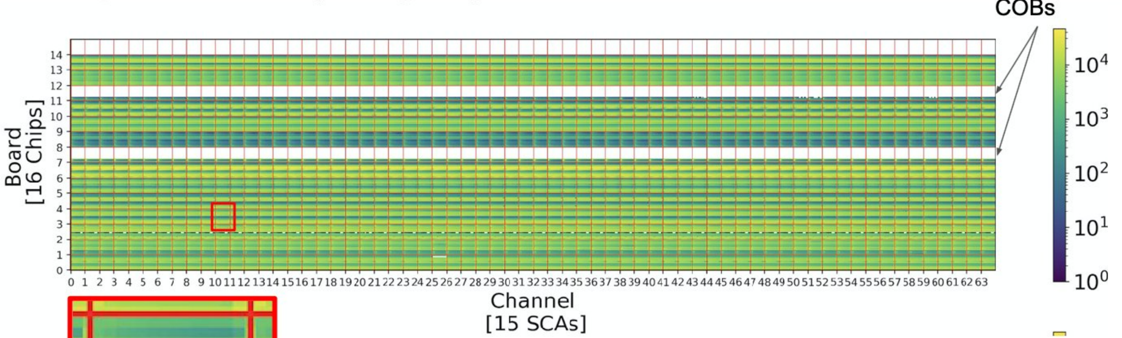


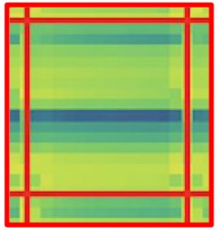
Simple Geant4 simulation for 5.5mm x 5.5mm, 325 um Si detector
Uniformly bombarded by 3 GeV electrons beam with 60 degree angle

Parameters

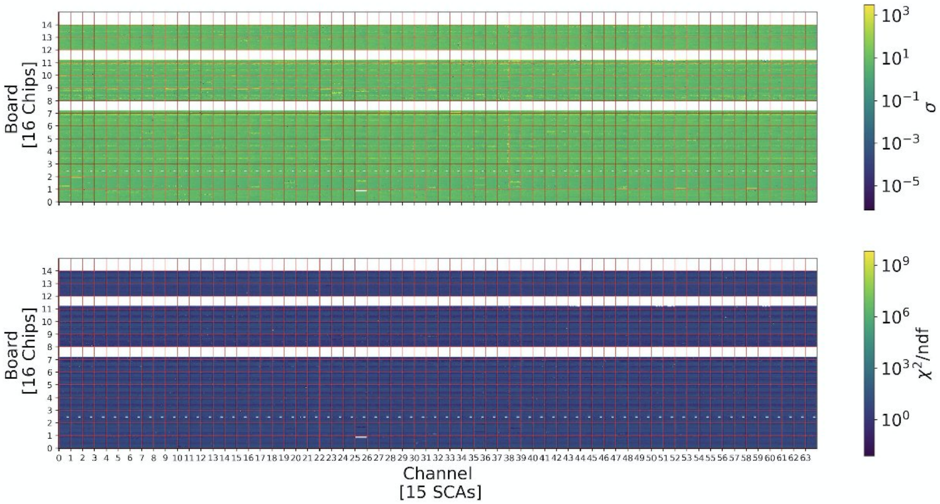
230k fits
(15 boards × 16 ASICs × 64 ch × 15 SCAs)

All pedestals (integral)





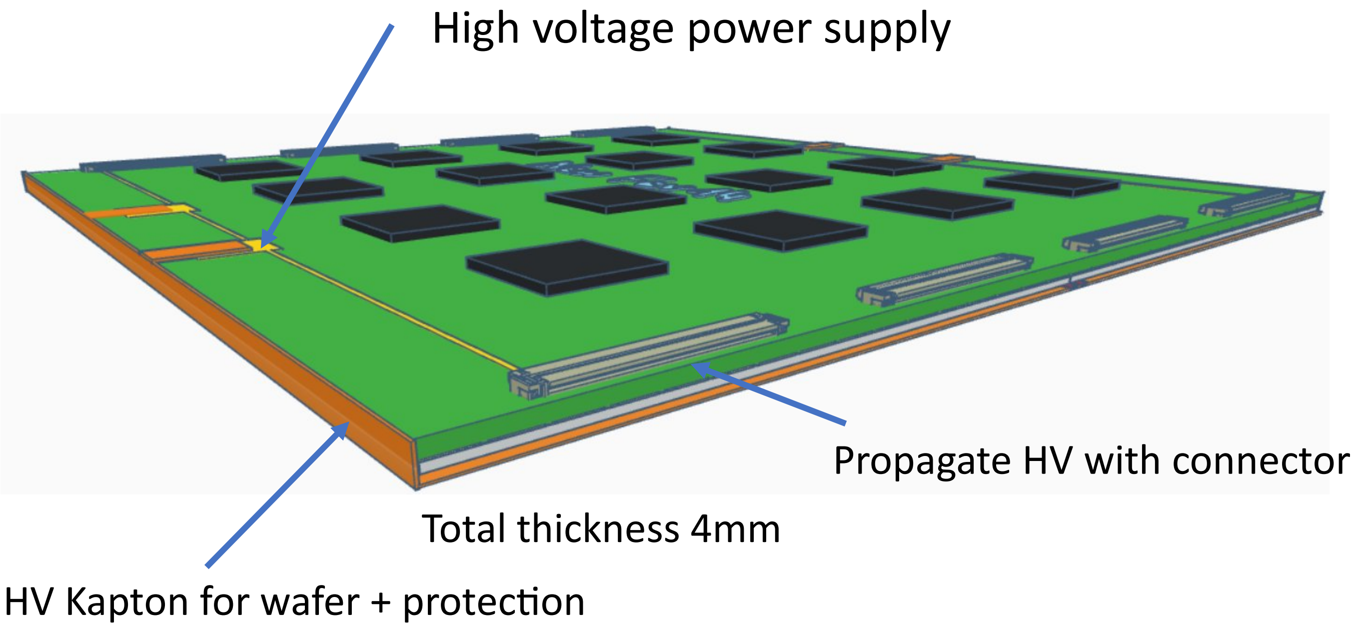
Typically channels present this two-partition pattern



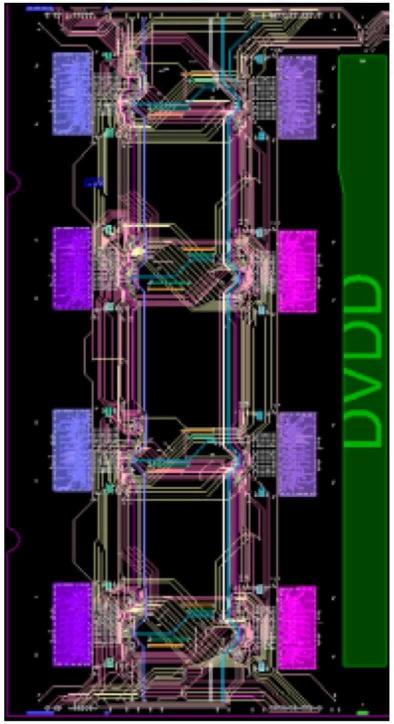
FEV2.0

Requirements

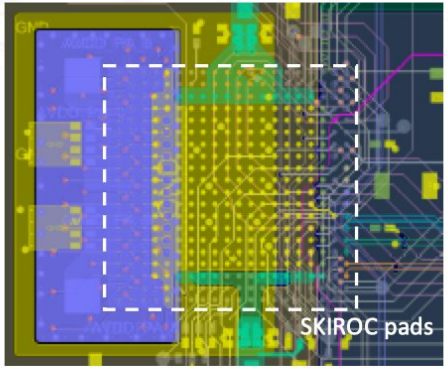
- Compatible FEV10,11,12
  - 16 ASICs
  - 4 Matrices 6'', 1024 chanels
- Improved mecanics, scalability & maintenance
  - Connectors
  - HV distribution & Filtering on PCB
  - 1 HV per card ⇒ independent test, exchangeabil
- LV Regulation on board with LDO
  - local Power-pulsing, lower currents (in B-field)
- Corrected data & clock distributions
  - Must be OK for 2,1 m (EndCaps) = 8 FEV
  - Timing ≤ 0,1 ns ? → for SK3 ?
- Compatibility new DAQ
- Improved noise & decoupling



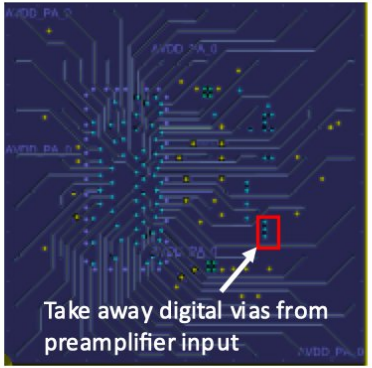
Layout optimizations



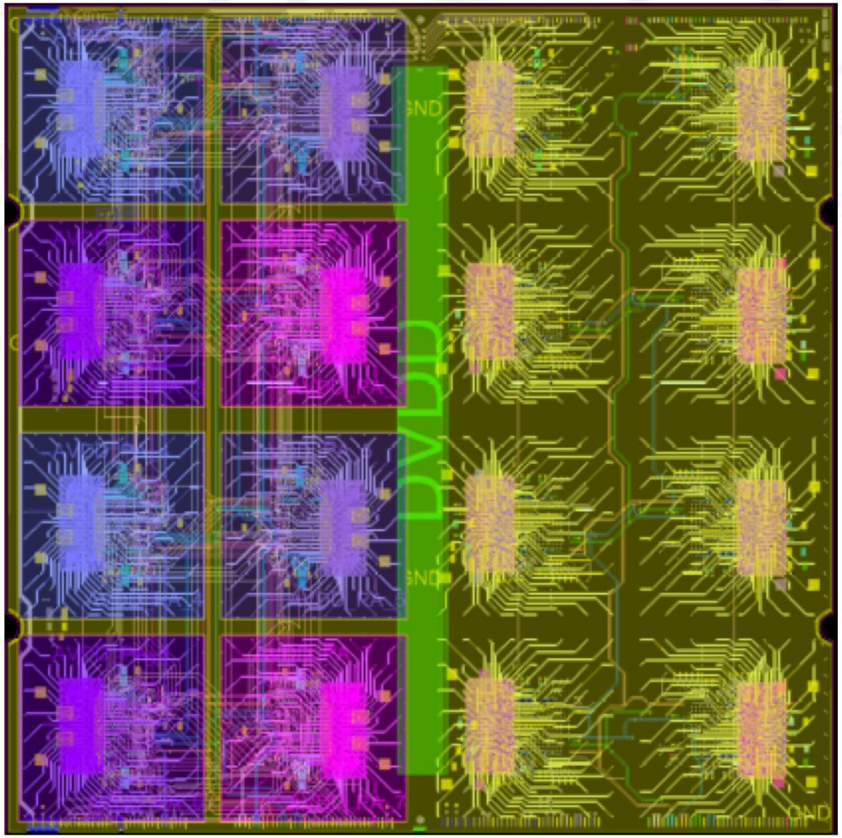
Digital lines optimized for long SLAB



Insulated input signals with GND ring



All patterns of input signal are identical



Board finished 45%

- 5% for LDO power
- 50% for partition duplication