New results of the technological prototype of the CALICE highly granular silicon tungsten calorimeter

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Particle Flow Detectors at Higgs Factories

Basis: sep of $H \rightarrow WW/ZZ \rightarrow 4j$
- $\sigma_{Z}/M_{Z} \approx \sigma_{W}/M_{W} \approx 2.7\% \oplus 2.75\sigma_{sep}$
  $\Rightarrow \sigma_{E}/E$ (jets) $< 3.8\%$

Large Tracker
- Precision and low $X_{0}$ budget
- Pattern recognition

High precision on Si trackers
- Tagging of beauty and charm

Large acceptance

Fwd Calorimetry:
- lumi, veto, beam monitoring

Imaging Calorimetry

Particle Flow Algorithms:
- Jets = 65% charged Tracks + 25% $\gamma$ ECAL + 10% $h^{0}$ CALO's
- TPC $\delta p/p \sim 5 \times 10^{-5}$; VTX $\sigma_{x,y,z} \sim 10 \mu$m

Particle Flow ECAL should:
- spot tracks & showers from charged ($h^{\pm}$, $e^{\pm}$)
- measure Photons in jets & Tau physics ($\gamma$ vs $\pi_{0}$)
- measure 2/3 of neutral hadrons interacting in the ECAL
- measure Time-of-Flight (10’s ps)

An Ultra-Granular SiW-ECAL for Higgs Factories

Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability ($E$, $(\theta, \phi)$, $t$)
- PFlow requirements:
  - Extremely high granularity: $5 \times 5$ mm$^2 \times 30$ layers
  - Compacity (density)
- Technical requirements:
  - Electronics & Service Integration (power, cooling, …)
  - Scalability: $\mathcal{O}(100M)$ channels $\Rightarrow \mathcal{O}(100k)$ boards

SiW+CFRC baseline choice for future Lepton Colliders:
(ILC/ILD, CLIC/det, FCC-ee/CLD, CEPC/Baseline)

- Tungsten as absorber material
  - $X_0 = 3.5$ mm, $R_M = 9$ mm, $\lambda_I = 96$ mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design: Sensor+RO≤2mm
  - Integration with Very-Front End Electronics
  - Allows for ~any pixelisation
  - Robust technology
  - Excellent signal/noise ratio: $\geq 10$
  - Intrinsic stability (vs environment, aging)
  - Albeit expensive...
- Tungsten–Carbon alveolar structure
  - Minimal structural dead-spaces
  - Scalability

To be assessed by prototypes
CALICE prototypes for ILC

Physical (2005-11)
- 1×1 cm² on 500μm 6×6 cm² Pad glued on PCB Floating GR
- × 30 layers (10k chan).
- External readout
- Proof of principe

Technological (now)
- Embedded electronics
  - Power-Pulsed, Auto-Trig, delayed RO
  - S/N = (MPV/σ_{Noise}) ≥ ~12 (trig)
- Compatible w/ 8+ modules-slab
- 5×5 mm² on 320–650μm 9×9 cm² × 26–30 layers
  - 8k (slab) ~ 30k (calo) channels

Pilote (2027?) ➡ Full Det (2035?)
- 1M ➡ 70M channels
- on 750μm 12×12 cm² 8” Wafers ?
- Pre-industrial building
- Full integration (~ cooling)
- Final ASIC (Ωmega SK3 ?)

30 years
We are here
**SKIROC2 / 2A Analogue core**

- 64 channels
- Auto-triggered
  - per cell adj.
  - 1 cell triggers all
- Preamp
  + 2 Gains + Auto-select
  + TDC (~1.4ns)
- 15 (×2) analogue memories
- Dyn range 0.1 ~ 2500 mips
  - mip in 320 μm (4 fC)
  - 12 bits ADC’s
- 616 config bits
- Low consumption
  - 25 μW/ch with 0.5% ILC-like duty cycle
- Power-Pulsed
FEV’s : 15 years of R&D

Most complex element: electro-mechanical integration

- Powering, Distrib / Collect signals from ASICs, Analog & Digital with dyn. range ≥ 7500
  - Single End operation → Chaining for 8–10 boards
- Mechanical placer & holder for Wafers → ≤ 50μm lateral precision, flatness
- Thickness constraints → Calorimeter Compactness

<table>
<thead>
<tr>
<th>Milestone</th>
<th>Date</th>
<th>Object</th>
<th>Details</th>
<th>REM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st ASIC proto</td>
<td>2007</td>
<td>SK1 on FEV4</td>
<td>36 ch, 5 SCA</td>
<td>proto, ≤ 2000 mips</td>
</tr>
<tr>
<td>1st ASIC</td>
<td>2009</td>
<td>SK2</td>
<td>64ch, 15 SCA</td>
<td>3000 mips</td>
</tr>
<tr>
<td>1st PCB proto</td>
<td>2010</td>
<td>FEV7</td>
<td>8 SK2</td>
<td>COB</td>
</tr>
<tr>
<td>1st working PCB</td>
<td>2011</td>
<td>FEV8</td>
<td>16 SK2 (1024 ch)</td>
<td>CIP (QGFP)</td>
</tr>
<tr>
<td>1st working ASU in BT</td>
<td>2012</td>
<td>FEV8</td>
<td>4 SK2 readout (256ch)</td>
<td>S/N ≤ ~ 14 (H Gain), no Power Pulsing retriggers 50–75%</td>
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<tr>
<td>1st run in PP</td>
<td>2013</td>
<td>FEV8-CIP</td>
<td>4 units on test board 1024 channel</td>
<td>BGA, Power Pulsing</td>
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<tr>
<td>1st full ASU</td>
<td>2015</td>
<td>FEV10</td>
<td>4 units on test board 1024 channel</td>
<td>S/N ~ 17–18 (H Gain) retrigger ~ 50%</td>
</tr>
<tr>
<td>1st SLABs</td>
<td>2016</td>
<td>FEV11</td>
<td>10 units</td>
<td>Noise issues</td>
</tr>
<tr>
<td>pre-calo</td>
<td>2017</td>
<td>FEV 11</td>
<td>7 units</td>
<td>S/N ~ 20 (12)_{\text{tag}}, 6–8 % masked</td>
</tr>
<tr>
<td>1st technological ECAL</td>
<td>2018</td>
<td>FEV11, 12 13 Compact Calo Long Slab</td>
<td>SK2 &amp; SK2a (no timing) 8 ASUs</td>
<td>Improved S/N Timing enabling</td>
</tr>
<tr>
<td>1st working COB, new DAQ</td>
<td>2019</td>
<td>FEV-COB</td>
<td>2x1/4 ASUs Cont. power.</td>
<td>Technical</td>
</tr>
<tr>
<td>2nd tech ECAL</td>
<td>20-22</td>
<td>5 types FEV’s</td>
<td>H. Gain, Cont. Power</td>
<td>320, 500, 650 μm</td>
</tr>
</tbody>
</table>
Present ‘FEV-zoo’

FEV10, 11, 12
- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main “Working horses” since 2014

FEV-COB
- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
  - Based on FEV11
  - External connectivity compatible

FEV13
- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity
Compact DAQ readout

“Dead space free” granular calorimeters ➞ ~ 30 mm space ECAL–HCAL

- Compact DAQ
- in use in BT since 2019

LabWindows + scriptings

- Full debug system
- → EUDAQ
  - Combined running
Beam Test at DESY-II Nov. 2021 + March 2022

DESY offers low-energetic beams of 1–6 GeV ($e^-, e^+$)

- 15 layers with 1024 readout cells each
  - 5.5 mm Si pads

4 weeks in total

- ~3 weeks of commissioning and “training”
  - Mechanical structure (adding or removing the tungsten plates)
  - New and continuously improving DAQ and online monitoring tools
  - New semi-online monitoring tools
  - Hold values, gain optimization, Threshold optimization, single cell calibration, etc

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)
Prototypes

**November 2021**
- Tungsten absorbers:
  - 11 × 2.1 mm (0.6 X₀)
  - + 3 × 4.2 mm (1.2 X₀)
  - total 10.2 X₀

**March 2022**
- Tungsten absorbers:
  - 7 × 2.8 mm (0.8 X₀)
  - + 8 × 4.2 mm (1.2 X₀)
  - total 15.2 X₀
Noise studies

SKIROC2

- 1 hit ($E_{\text{chan}} \geq \text{Thr.}$), 64 readouts
- Sparse showers ➞ many noise cells

Coherent vs Incoherent noise sources


Coherent noise source identification in multi channel analysis

T. Frisson$^{*1}$ and R. Poeschl$^1$

$^1$Laboratoire de L'accélérateur Linéaire (LAL), CNRS/IN2P3, Orsay, France

Analysis of collective Gaussian noise sources by correlation between channels

\[
\sigma_i^2 = \sigma_i^2 + \sum_{j=1}^{N_c} \sigma_{C_i,j}^2
\]  

(1)

The covariance matrix element from the two channels $i$ and $k$ is expressed by:

\[
cov(i, k) = \delta_{ik} \sigma_i \sigma_k + \sum_{j=1}^{N_c} \sigma_{C_i,j} \sigma_{C_k,j}
\]

(2)

where:

\[
\delta_{ik} = \begin{cases} 
1 & \text{if } i = k \\
0 & \text{if } i \neq k 
\end{cases}
\]

(3)

The covariance matrix element can also be determined from the data:

\[
cov_{\text{Data}}(i, k) = \frac{\sum_{n=1}^{N_{\text{event}}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{\text{event}}}
\]

(4)
15 layers $\times 1024$ ch $\times 15$ mem = 230k fits

MIP $\sim 70$–140 adcc
Pedestal widths, 1\textsuperscript{st} memory cells, per ASIC

- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors
Layer 7: FEV12 SK2a, 500 μm

Legend
- 1) Pedestal map
- 2) Incoherent noise map
- 3) coherent noise map (c1)
- 4) coherent noise map (c2)

Outcomes:
- Few channels are off
  - These are usually seen as noise sources (FEV10/11/22)
- Routing issues
  - addressed in next generation

Reminder: Noise is THE enemy of local self-triggering with local storage FE readout.
Mips response: no tungsten
MIP calibration

- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
  - Understood and will be corrected

... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
  - Have since last week access to the different stages of the ASICs
    - => major debugging tool
  - In any case less good layers will be replaced in coming months
Simulation

Done in DD4HEP framework (G4 overlayer)
- very flexible XML configuration
- derived from ILC soft

Digitization:
- Mimicking of the SKIROC2 ASICs

Shaping in Fast and Slow Branch
- MIP calibration in both branches
  - as in data
- Application of thr. on Fast B,
- ➞ Delay for Slow B. readout

Parameters being adjusted on data
Electron Showers

Data

MC (no digitization)
First look at in-shower spectrums (3 GeV)

MIP & Threshold calibration in-shower possible

... but requires a level of noise performance
3 GeV Raw Hit Shower profiles - in High Gain

**Data** (Gain 1.2 pF)

**MC**

Escale $\rightarrow \leq \sim 40$ mips / cells
Gain adjustment

**DESY (Ee ≤ 6 GeV)**
(Gain 1,2 pF)

**CERN, ILC (Ee ≤ 100 GeV)**
(Gain 6 pF)

**Preamplifier Gain 1.2 pF / 6 pF ~ × 4.73**

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<table>
<thead>
<tr>
<th></th>
<th>DESY (Ee ≤ 6 GeV)</th>
<th>CERN, ILC (Ee ≤ 100 GeV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Entries</td>
<td>57600</td>
<td>57600</td>
</tr>
<tr>
<td>Mean</td>
<td>138.1</td>
<td>28.52</td>
</tr>
<tr>
<td>Std Dev</td>
<td>82.88</td>
<td>15.38</td>
</tr>
<tr>
<td>$\chi^2 / \text{ndf}$</td>
<td>70.96 / 55</td>
<td>33.82 / 21</td>
</tr>
<tr>
<td>Width</td>
<td>6.815 ± 0.079</td>
<td>1.866 ± 0.065</td>
</tr>
<tr>
<td>MP</td>
<td>92.66 ± 0.05</td>
<td>19.62 ± 0.06</td>
</tr>
<tr>
<td>Area</td>
<td>2.153e+05 ± 6.840e+02</td>
<td>1.933e+04 ± 1.707e+02</td>
</tr>
<tr>
<td>GSigma</td>
<td>7.185 ± 0.169</td>
<td>3.182 ± 0.134</td>
</tr>
</tbody>
</table>
```
Next steps

Beam test at CERN (June 22)

Preparation:

- Integration of more FEV13
- Commissioning with 6pF
  - Cosmics data taking on-going
- Increased W integration : $18.4 \times X_0$

Finalising and testing the design of next gen FEV

- Improvement on power and signal routing
  ➞ better chaining, less induced noise
  ➞ more flexibility
Outlook

First Beam Tests (after 2 years of COVID)
- 1st test of a complete stack of the SiW-ECAL:
  - 15 layers (albeit heterogenous)
  - Two set-up 10.2 $X_0$ and 15.2 $X_0$

Training and Running phase
- New Compact DAQ (15 layers)
- Thin design (COB) operational
- Noise and Gain optimisations on particles

Most Layers operated as expected
- some noisier, some quieter
- Signs of conductive glue aging (wafer-PCB)

Low energy electrons:
- Punch-through $\rightarrow$ MIP spectrums
  - MIP Calibration on-going
- Electron showers structure
  - First plots of resolution (not shown):
    - Correction of defects (masking, aging)
      need to be integrated.

To come:
- Adiabatic Increasing difficulty (Gain $\downarrow$, Compactness $\uparrow$)
- High Energy electrons (and Hadron): CERN June 22
- New FEV, with BGA design
Thank you for your attention

Thanks to
H. García, J. Kunath, F. Jimenez, Y. Okugawa, A. Irles, R. Poeschl, T. Suehara, S. Callier and many others
for material and inspiration for this talk

Thanks to the engineering teams of IJCLab, LPNHE and LLR
and to the Beam Test coordinators at DESY
Detector Commissioning on MIPs: max of shape
Mip analysis

Pixel energy fraction depends linearly on crossing position

\[ \text{MP}(\alpha) = \text{MP}(0) \cos(\alpha) \]

Energy deposited in the detector

Simple Geant4 simulation for 5.5mm x 5.5mm, 325 um Si detector
Uniformly bombarded by 3 GeV electrons beam with 60 degree angle
Parameters

230k fits
(15 boards × 16 ASICs × 64 ch × 15 SCAs)

Typically channels present this two-partition pattern
FEV2.0

Requirements

- Compatible FEV10,11,12
  - 16 ASICs
  - 4 Matrices 6”, 1024 channels
- Improved mechanics, scalability & maintenance
  - Connectors
  - HV distribution & Filtering on PCB
  - 1 HV per card → independent test, exchangeability
- LV Regulation on board with LDO
  - Local Power-pulsing, lower currents (in B-field)
- Corrected data & clock distributions
  - Must be OK for 2,1 m (EndCaps) = 8 FEV
  - Timing ≤ 0,1 ns ? → for SK3 ?
- Compatibility new DAQ
- Improved noise & decoupling

High voltage power supply

Total thickness 4mm

HV Kapton for wafer + protection

Propagate HV with connector
Layout optimizations

Digital lines optimized for long SLAB

Insulated input signals with GND ring

All patterns of input signal are identical

Board finished 45%
  ▪ 5% for LDO power
  ▪ 50% for partition duplication