Development of a hybrid single-photon detector with pixelated anode and integrated CMOS analog and digital front-end

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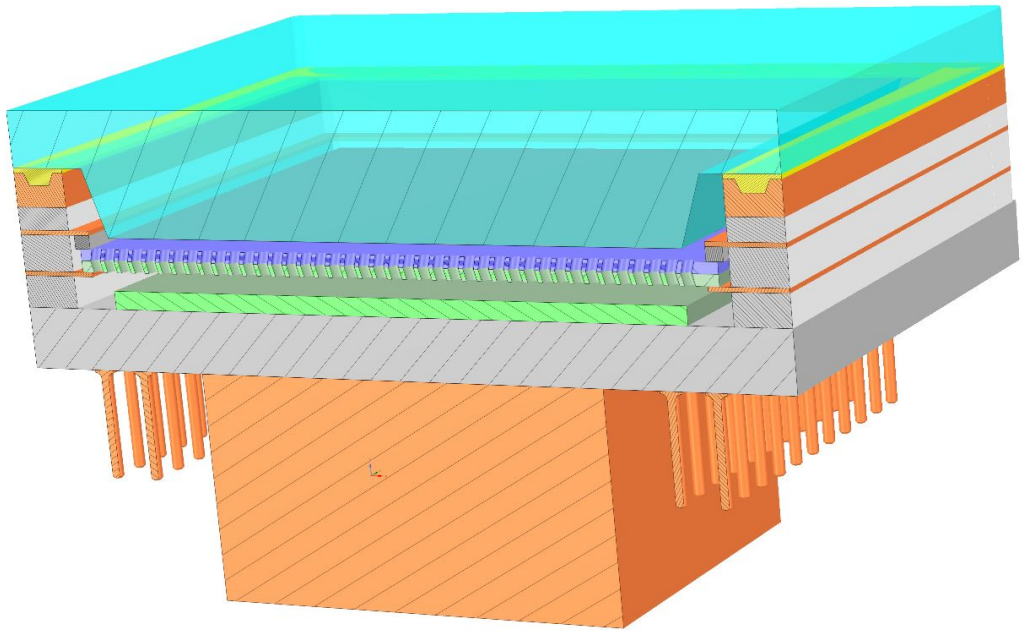
European Research Council

15th Pisa Meeting on Advanced Detectors

European Research Council

Overview

- The hybrid detector concept
- The Timepix4 ASIC
- Expected performance
- Design status



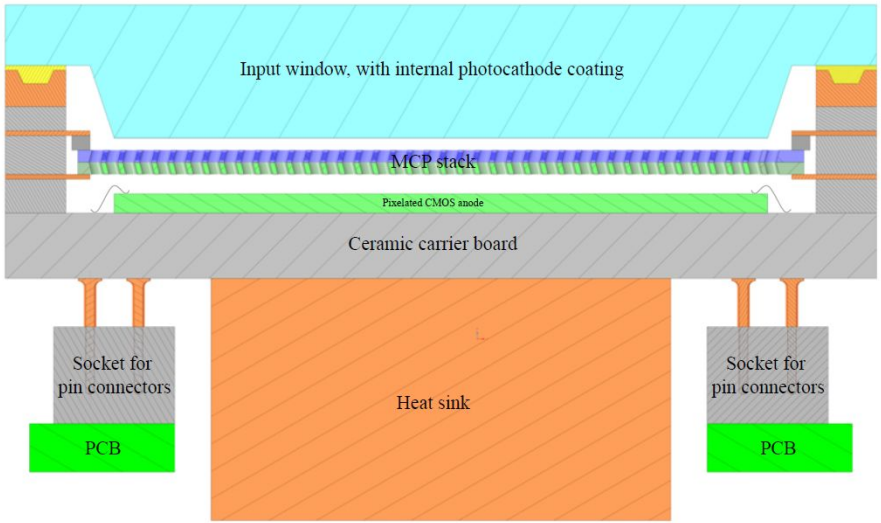
The ‘hybrid’ detector [M. Fiorini et al. JINST 13 (2018) C12005]

We are developing a single-photon detector:

- based on a vacuum tube
- transmission photocathode with high QE in the spectral region of interest
- dual micro-channel plate stack
- a pixelated CMOS read-out anode with integrated front end electronics

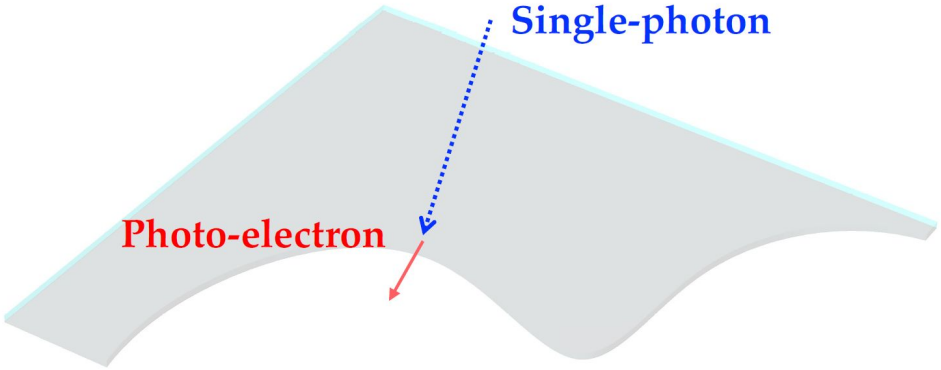
Timing resolution	few 10 ps
Position resolution	5-10 μm
Maximum rate	10^9 hits/s (ASIC)
Dark count rate	10^2 counts/s
Active area	~7 cm^2
Channel density	0.23 M channels

The detector assembly



- Vacuum-based detector
  - Assembly under high vacuum (10^{-10} mbar)
- Assembly and bonding to minimize distance between components
- High-speed connections through pins in ceramic carrier board
  - custom PGA - 2.54 mm pitch
  - socket for detector I/O and low voltage
- Heat sink under ASIC
  - Assembly < 21° C with ASIC @ peak power
- PCB allows connection to FPGA-based DAQ system

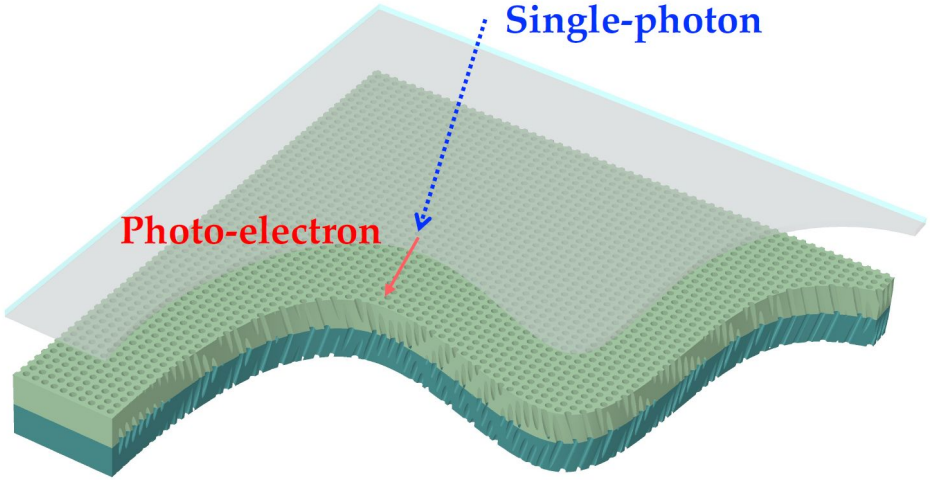
The hybrid detector: entrance window + photocathode



Photon conversion using high Quantum Efficiency (QE) Photocathode

- E.g. bialkali photocathode
  - Up to 40-50% QE
  - O(10^2) Hz/cm^2 dark count rate @300 K
  - Best for timing
- Flexible design allows to use different photocathodes

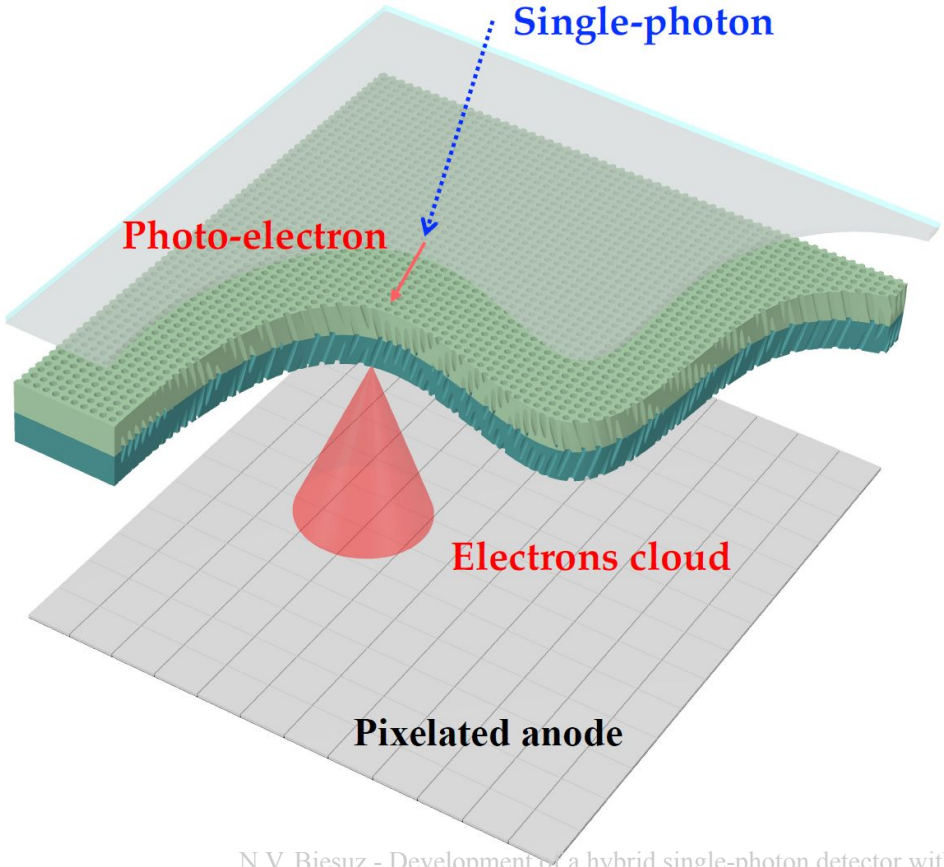
The hybrid detector: microchannel plate stack



Microchannel plate stack (chevron)

- > 10^4 gain
- 5-10 μm pore size
- Atomic layer deposition for increased lifetime:
  - >20 C/cm^2 integrated anode charge
- Short distance from MCP to cathode and anode for best time and position resolution

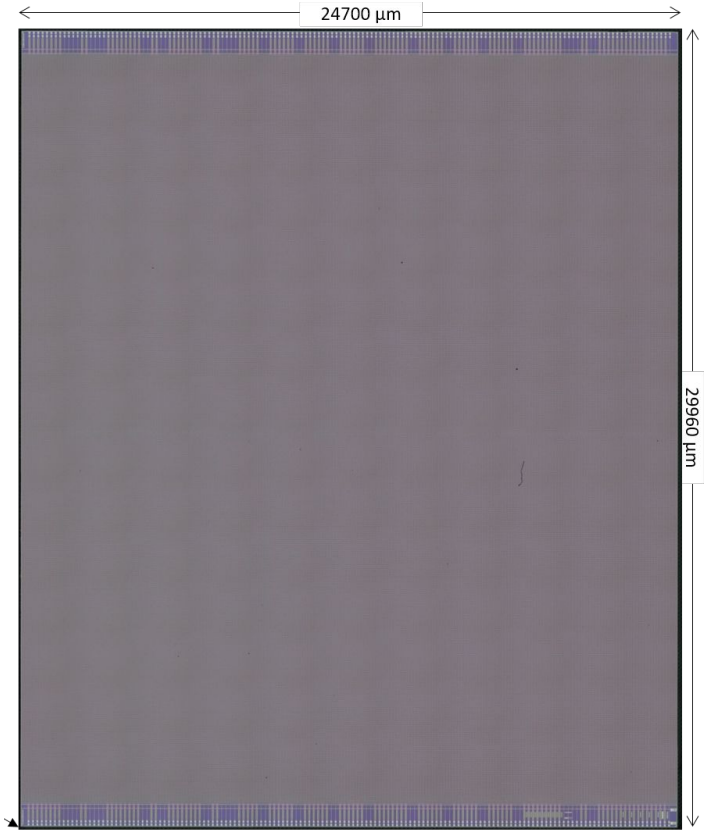
The hybrid detector: pixelated anode



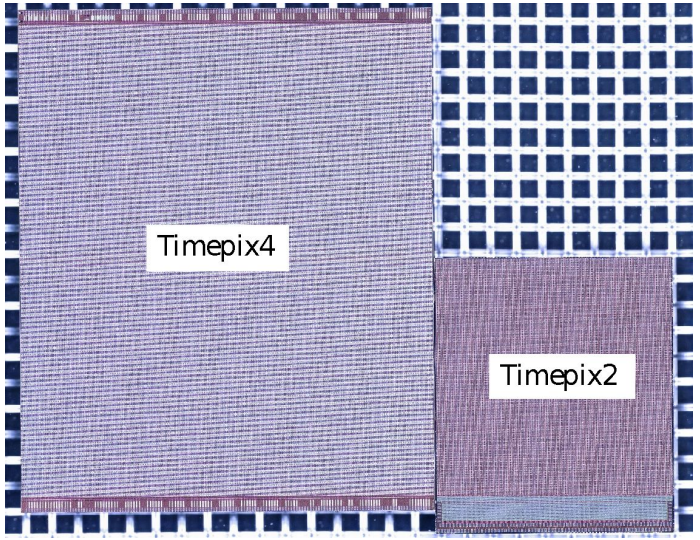
Pixelated anode

- Electron cloud spread over a number of pixels
- Anode is an ASIC
- it integrates digital and analog front-end
  - pixels coordinates
  - pixels Time of Arrival
  - pixels Time over Threshold
- Output:
  - 64 bits of data per event and per pixel with 64B/66B encoding
  - transmitted on 16 high speed links @ 10 Gbps

The Timepix4 ASIC

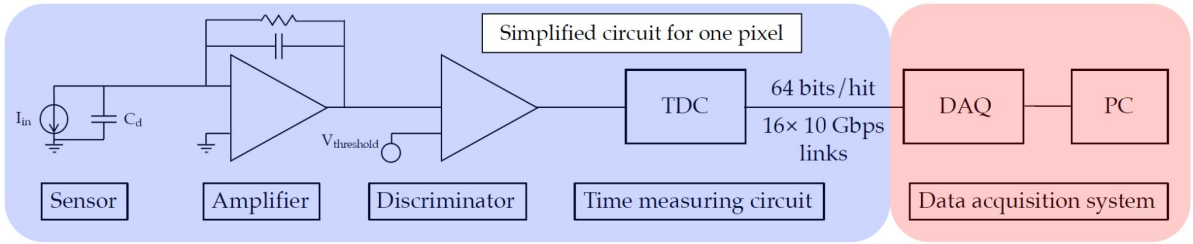


- 65 nm CMOS (TSMC)
- ASIC productions:
  - Timepix4_v0 (Q1 2020)
  - Timepix4_v1 (Q4 2020)
  - Timepix4_v2 (Q3 2021)



The Timepix4 ASIC

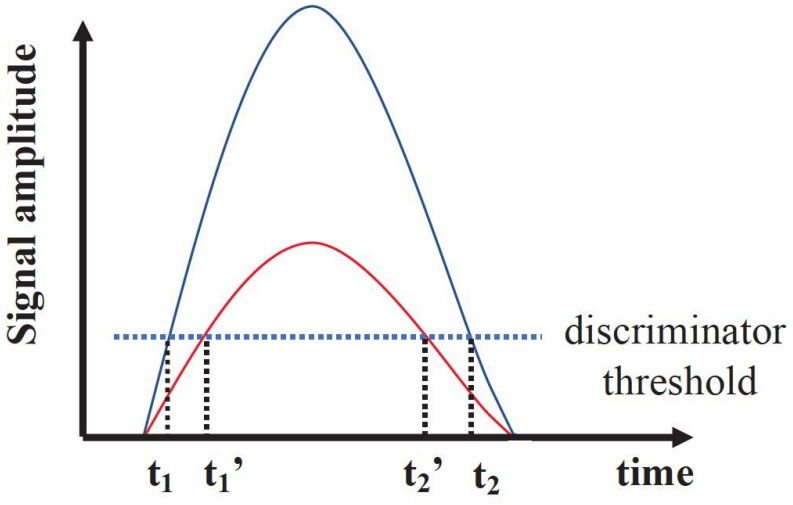
- Timepix4 ASIC in 65nm CMOS
  - Developed by the Medipix Collaboration for hybrid pixel detectors



- 512 × 448 pixels (use bump pad as anode)
  - square pitch: 55 μm
- Integrates Time to Digital Converter (TDC)
  - 195 ps bin size (56 ps rms resolution)
- High data rate capability
  - 160 Gbps
  - **$5 \cdot 10^9$ hits/mm^2/s**
- Large Active Area: 7 cm^2

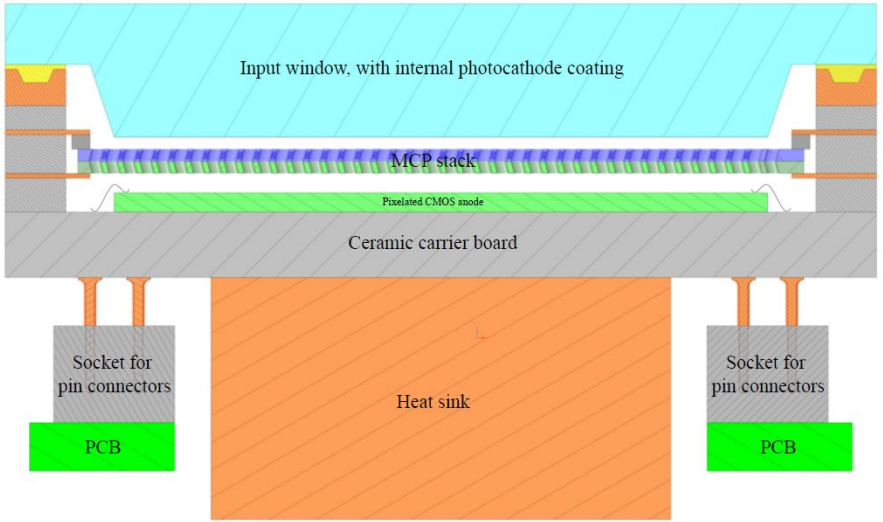
The Timepix4 ASIC: improving resolution

- For each pixel, it provides combined measure of:
  - Time-of-Arrival [t_1]
  - Time-over-Threshold [t_2 - t_1]
- Time over Threshold used to:
  - Correct for time-walk effect [t_1 - t_1']
  - Improve resolution on cluster centroid
    - **~16µm → ~5µm**
  - 3D clustering (space and time)
    - Improve timing resolution by multiple sampling
    - Cluster Time of Arrival Resolution **few 10s ps**



Design status

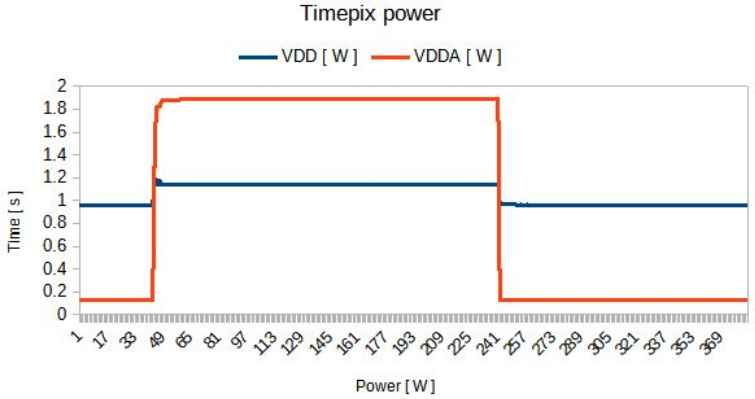
- 2nd version of the Timepix4 ASIC available
  - currently study of ASIC performance
  - designing control software
  - designing control firmware
- Ceramic carrier studies ongoing
  - engineering mock–ups
    - effect of ceramics on MGT lines
    - mechanics/tolerances
    - components connection

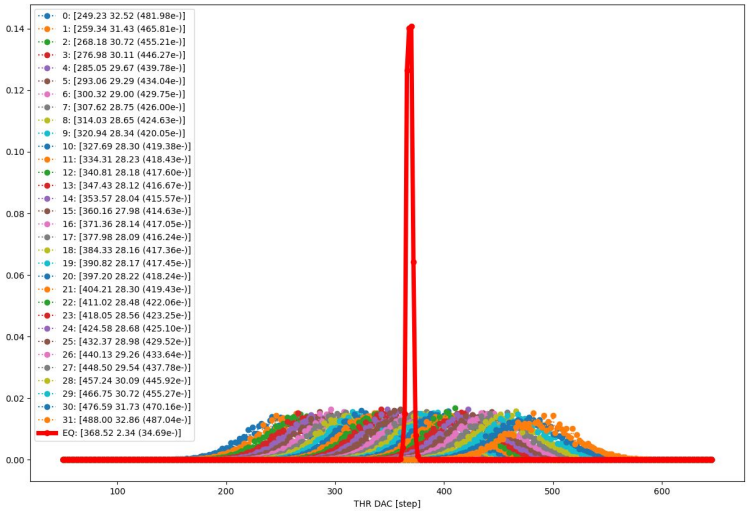


Timepix4 tests

Preliminary measurements on Timepix4 to establish:

- cooling requirements
  - expected peak-power
  - power profile
- equalization procedure
  - select optimal Threshold per pixel
  - 5 DAC per pixel
    - 14-bit DAC code
    - 4-bit gain setting
- calibration procedure
- parameter optimization
  - compensation current
  - noisy pixel detection (sensor related)





Ceramic-carrier tests

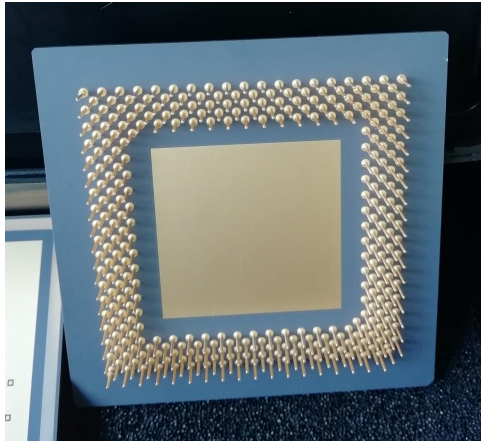
Foreseen dedicated testbed
- electrical
- mechanical

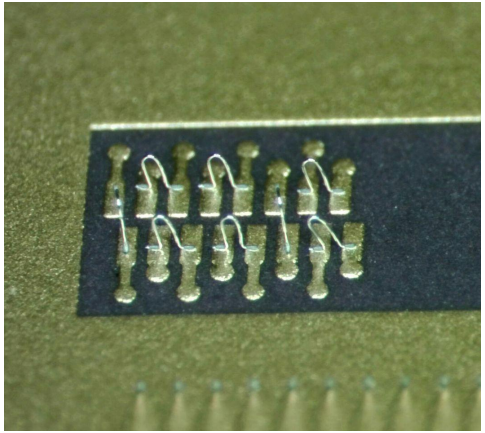
Electrical design critical due to 10 Gbps lines

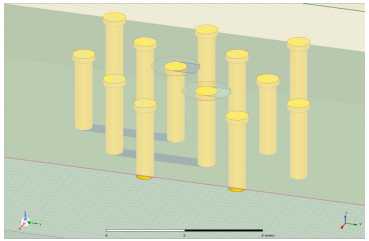
First qualitative electrical measures
- existing devices (loop-back)
- simulations

PGA not limiting factor per se
- industry standard for photo-tubes
- existing sockets
  - -1dB @ < 30 GHz
- requires careful placing of pins
- low pin density

Main contributor to signal degradation
- parasitic capacitance
  - Aluminium oxide multilayer PCB
  - Pads (wire-bond and pin pads)







Software and DAQ

Timepix4 control software and DAQ mandatory:

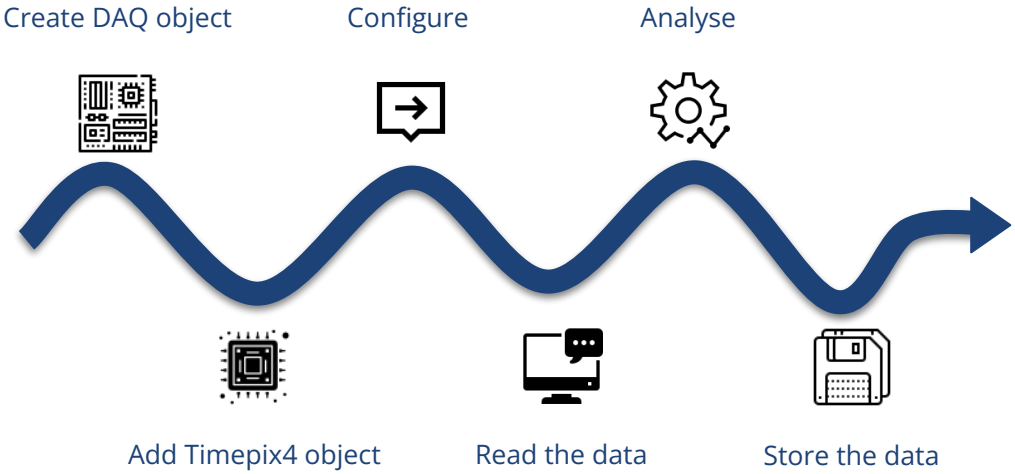
- full test of produced device

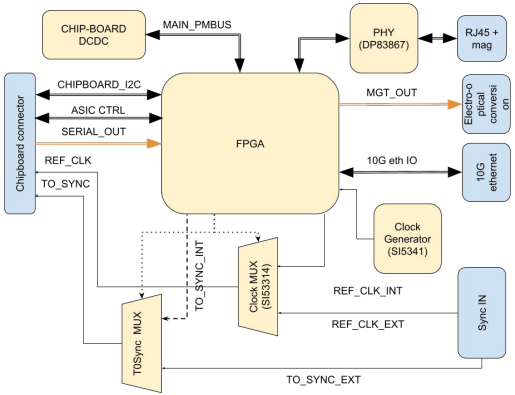
Existing version of software and DAQ by NIKHEF:

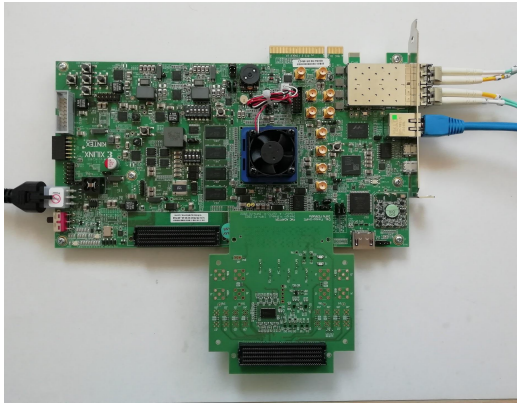
- great tool for preliminary test
- not fully open SW/FW/HW

Great effort to produce our own

- software
- firmware
- hardware







Summary

We are developing a detector for visible single photons:

- based on a vacuum tube
- a bare Timepix4 CMOS ASIC (anode)
- a Micro Channel Plate stack

This detector will allow the detection of up to 10^9 photons/s with simultaneous measurement of time and position with excellent resolutions

- Fully exploit both timing and position resolutions of a MCP
- High-performance data acquisition (up to ~160 Gbps)

Detector will be produced together with a dedicated

- DAQ & socket
- control software
- cooling system

Development is ongoing…

Thank you!

4D PHOTON Team

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BACK UP!

Timepix4

			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	$0.43x10^6$ hits/mm^2/s	**$3.58x10^6$ hits/mm^2/s**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s
TOT energy resolution			< 2KeV	**< 1Kev**
TOA binning resolution			1.56ns	**195ps**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**
Target global minimum threshold			<500 e^-	<500 e^-