Development of a hybrid single-photon detector with pixelated anode and integrated CMOS analog and digital front-end

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for the 4DPHOTON team

15th Pisa Meeting on Advanced Detectors
Overview

- The hybrid detector concept
- The Timepix4 ASIC
- Expected performance
- Design status

We are developing a single-photon detector:

- based on a vacuum tube
- transmission photocathode with high QE in the spectral region of interest
- dual micro-channel plate stack
- a pixelated CMOS read-out anode with integrated front end electronics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timing resolution</td>
<td>few 10 ps</td>
</tr>
<tr>
<td>Position resolution</td>
<td>5-10 μm</td>
</tr>
<tr>
<td>Maximum rate</td>
<td>$10^9$ hits/s (ASIC)</td>
</tr>
<tr>
<td>Dark count rate</td>
<td>$10^2$ counts/s</td>
</tr>
<tr>
<td>Active area</td>
<td>~7 cm²</td>
</tr>
<tr>
<td>Channel density</td>
<td>0.23 M channels</td>
</tr>
</tbody>
</table>
The detector assembly

- Vacuum-based detector
  - Assembly under high vacuum ($10^{-10}$ mbar)

- Assembly and bonding to minimize distance between components

- High-speed connections through pins in ceramic carrier board
  - Custom PGA - 2.54 mm pitch
  - Socket for detector I/O and low voltage

- Heat sink under ASIC
  - Assembly < 21°C with ASIC @ peak power

- PCB allows connection to FPGA-based DAQ system
The hybrid detector: entrance window + photocathode

Photon conversion using high Quantum Efficiency (QE) Photocathode

- E.g. bialkali photocathode
  - Up to 40-50% QE
  - $O(10^2) \text{ Hz/cm}^2$ dark count rate @300 K
  - Best for timing

- Flexible design allows to use different photocathodes
The hybrid detector: microchannel plate stack

Microchannel plate stack (chevron)

- $> 10^4$ gain
- 5-10 μm pore size
- Atomic layer deposition for increased lifetime:
  - $>20$ C/cm$^2$ integrated anode charge
- Short distance from MCP to cathode and anode for best time and position resolution

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The hybrid detector: pixelated anode

Pixelated anode

- Electron cloud spread over a number of pixels
- Anode is an ASIC
- It integrates digital and analog front-end
  - pixels coordinates
  - pixels Time of Arrival
  - pixels Time over Threshold
- Output:
  - 64 bits of data per event and per pixel with 64B/66B encoding
  - transmitted on 16 high speed links @ 10 Gbps

Pixelated anode

Electrons cloud

Photo-electron

Single-photon

Electrons cloud

Pixelated anode

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The Timepix4 ASIC

- 65 nm CMOS (TSMC)
- ASIC productions:
  - Timepix4_v0 (Q1 2020)
  - Timepix4_v1 (Q4 2020)
  - Timepix4_v2 (Q3 2021)
The Timepix4 ASIC

- Timepix4 ASIC in 65nm CMOS
  - Developed by the Medipix Collaboration for hybrid pixel detectors

  - 512 × 448 pixels (use bump pad as anode)
    - square pitch: 55 μm

- Integrates Time to Digital Converter (TDC)
  - 195 ps bin size (56 ps rms resolution)

- High data rate capability
  - 160 Gbps
  - $5 \times 10^9$ hits/mm²/s

- Large Active Area: 7 cm²
For each pixel, it provides combined measure of:

- Time-of-Arrival \[ t_1 \]
- Time-over-Threshold \[ t_2 - t_1 \]

Time over Threshold used to:

- Correct for time-walk effect \[ t_1 - t_1' \]
- Improve resolution on cluster centroid
  - \(~16\mu m \rightarrow ~5\mu m\)
- 3D clustering (space and time)
  - Improve timing resolution by multiple sampling
  - Cluster Time of Arrival Resolution few 10s ps

\[ \text{Signal amplitude} \]

\[ \text{discriminator threshold} \]

\[ \text{time} \]

\[ t_1, t_1', t_2, t_2' \]
Design status

- 2\textsuperscript{nd} version of the Timepix4 ASIC available
  - currently study of ASIC performance
  - designing control software
  - designing control firmware
- Ceramic carrier studies ongoing
  - engineering mock–ups
    - effect of ceramics on MGT lines
    - mechanics/tolerances
    - components connection
Timepix4 tests

Preliminary measurements on Timepix4 to establish:

- cooling requirements
  - expected peak-power
  - power profile

- equalization procedure
  - select optimal Threshold per pixel
  - 5 DAC per pixel
    - 14-bit DAC code
    - 4-bit gain setting

- calibration procedure

- parameter optimization
  - compensation current
  - noisy pixel detection (sensor related)
Ceramic-carrier tests

Foreseen dedicated testbed
- electrical
- mechanical

Electrical design critical due to 10 Gbps lines

First qualitative electrical measures
- existing devices (loop-back)
- simulations

PGA not limiting factor per se
- industry standard for photo-tubes
- existing sockets
  - -1dB @ < 30 GHz
- requires careful placing of pins
- low pin density

Main contributor to signal degradation
- parasitic capacitance
  - Aluminium oxide multilayer PCB
  - Pads (wire-bond and pin pads)
Software and DAQ

Timepix4 control software and DAQ mandatory:
- full test of produced device

Existing version of software and DAQ by NIKHEF:
- great tool for preliminary test
- not fully open SW/FW/HW

Great effort to produce our own
- software
- firmware
- hardware
We are developing a detector for visible single photons:

- based on a vacuum tube
- a bare Timepix4 CMOS ASIC (anode)
- a Micro Channel Plate stack

This detector will allow the detection of up to $10^9$ photons/s with simultaneous measurement of time and position with excellent resolutions

- Fully exploit both timing and position resolutions of a MCP
- High-performance data acquisition (up to ~160 Gbps)

Detector will be produced together with a dedicated

- DAQ & socket
- control software
- cooling system

Development is ongoing…
Thank you!
4D PHOTON Team

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BACK UP!
# Timepix4

<table>
<thead>
<tr>
<th>Readout Modes</th>
<th>Technology</th>
<th>Pixel Size</th>
<th>Pixel arrangement</th>
<th>Sensitive area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data driven (Tracking)</td>
<td>130nm – 8 metal</td>
<td>55 x 55 μm</td>
<td>3-side buttable 256 x 256</td>
<td>1.98 cm²</td>
</tr>
<tr>
<td>Frame based (Imaging)</td>
<td>65nm – 10 metal</td>
<td>55 x 55 μm</td>
<td>4-side buttable 512 x 448</td>
<td>6.94 cm²</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>Event Packet Mode</td>
<td>48-bit</td>
<td>64-bit</td>
</tr>
<tr>
<td>Max rate</td>
<td>0.43x10⁶ hits/mm²/s</td>
<td>3.58x10⁶ hits/mm²/s</td>
</tr>
<tr>
<td>Max Pix rate</td>
<td>1.3 KHz/pixel</td>
<td>10.8 KHz/pixel</td>
</tr>
<tr>
<td>PC (10-bit) and iTOT (14-bit)</td>
<td>CRW: PC (8 or 16-bit)</td>
<td></td>
</tr>
<tr>
<td>Zero-suppressed (with pixel addr)</td>
<td>Full Frame (without pixel addr)</td>
<td></td>
</tr>
<tr>
<td>~0.82 x 10⁹ hits/mm²/s</td>
<td>~5 x 10⁹ hits/mm²/s</td>
<td></td>
</tr>
<tr>
<td>TOT energy resolution</td>
<td>&lt; 2KeV</td>
<td>&lt; 1Kev</td>
</tr>
<tr>
<td>TOA binning resolution</td>
<td>1.56ns</td>
<td>195ps</td>
</tr>
<tr>
<td>TOA dynamic range</td>
<td>409.6 μs (14-bits @ 40MHz)</td>
<td>1.6384 ms (16-bits @ 40MHz)</td>
</tr>
<tr>
<td>Readout bandwidth</td>
<td>≤5.12Gb (8x SLVS@640 Mbps)</td>
<td>≤163.84 Gbps (16x @10.24 Gbps)</td>
</tr>
<tr>
<td>Target global minimum threshold</td>
<td>&lt;500 e⁻</td>
<td>&lt;500 e⁻</td>
</tr>
</tbody>
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