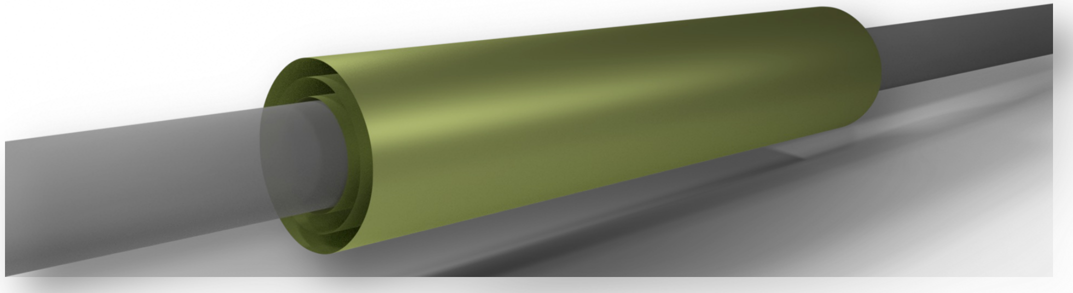
Developments of Stitched Monolithic Pixel Sensors towards the application in the ALICE ITS3

Gianluca AGLIERI RINELLA

On behalf of the ALICE Collaboration



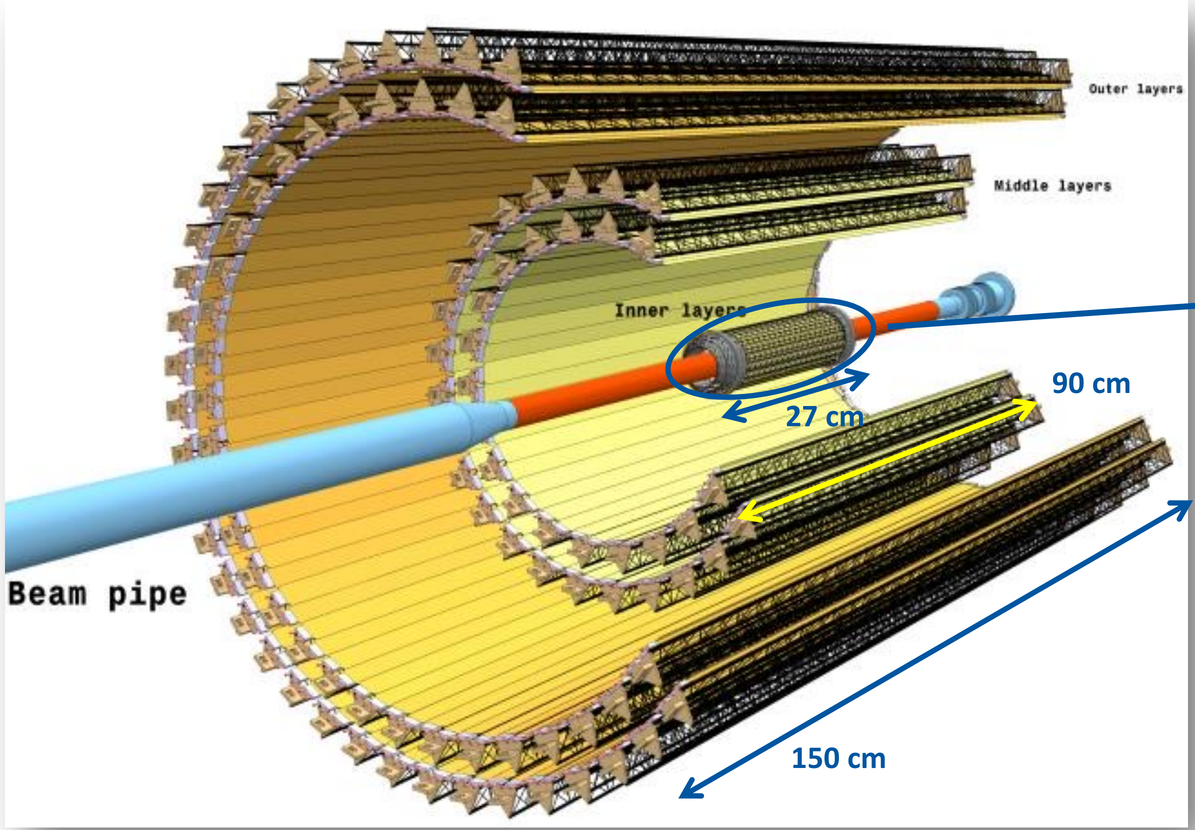
Outline

Introduction to ALICE ITS3

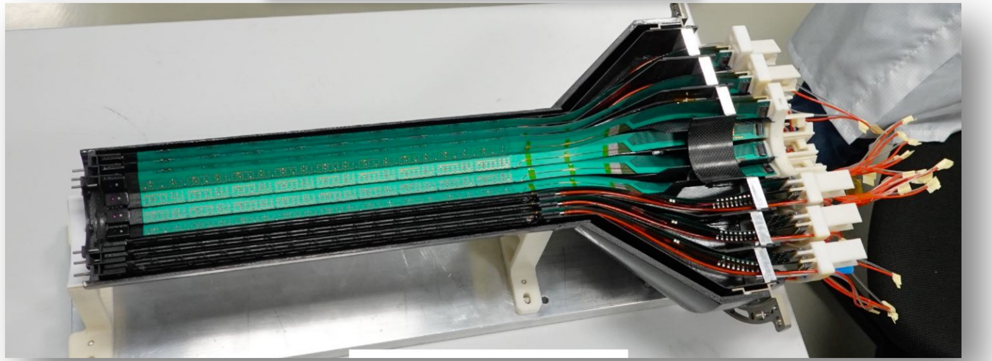
Sensor Developments

Monolithic Stitched Sensor Prototype (MOSS)

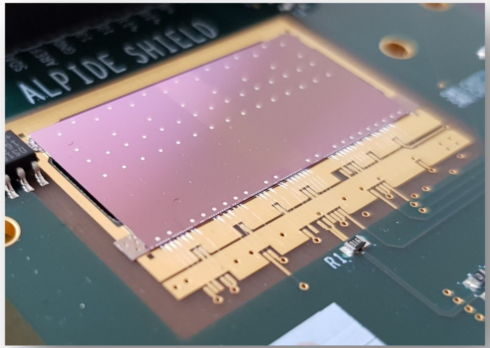
ALICE ITS2 Inner Tracking System

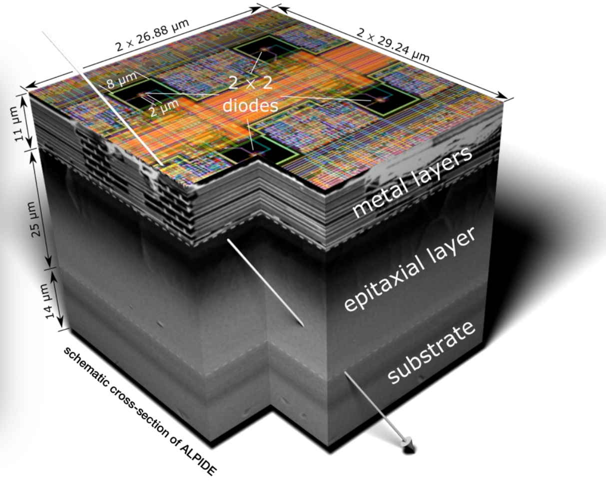


ITS2 Half Inner Barrel



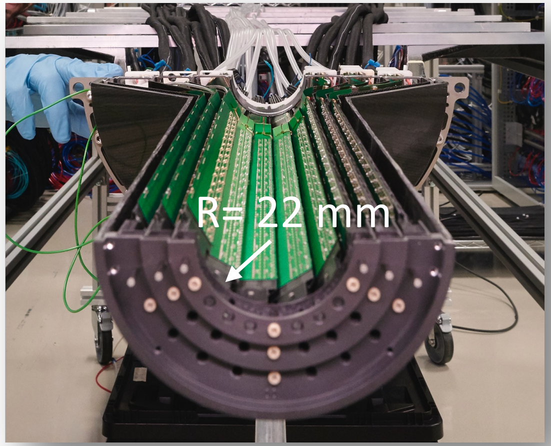
~12.5 Gpixels, 10 m^2 sensitive area
24120 **ALPIDE** Pixel Sensors (CMOS 180 nm)

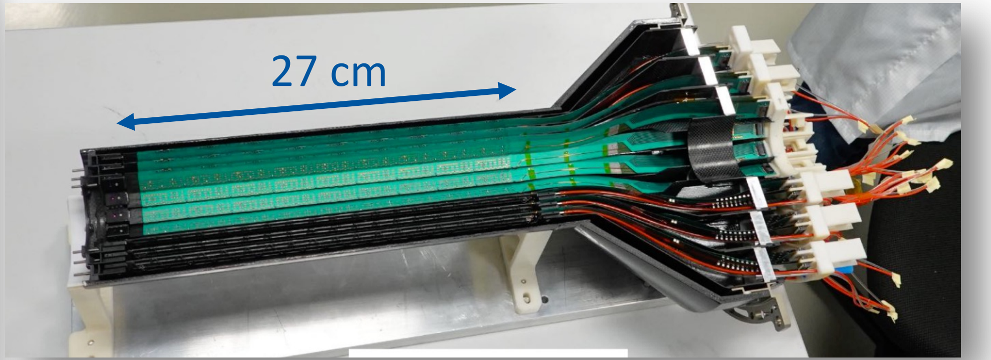




ITS3 Concept

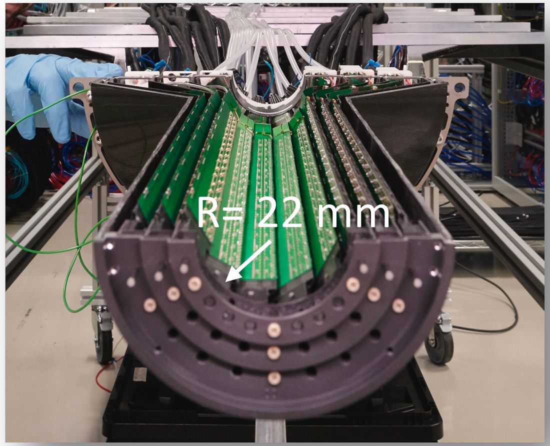
ITS2 Half Inner Barrel
3 Inner Layers

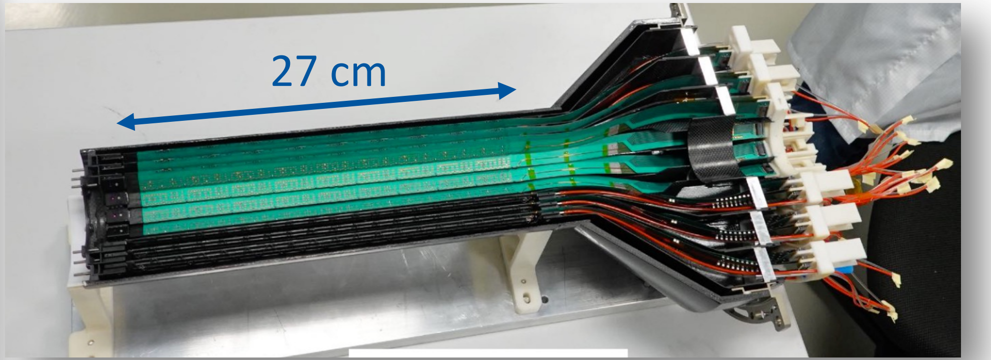




ITS3 Concept

ITS2 Half Inner Barrel
3 Inner Layers

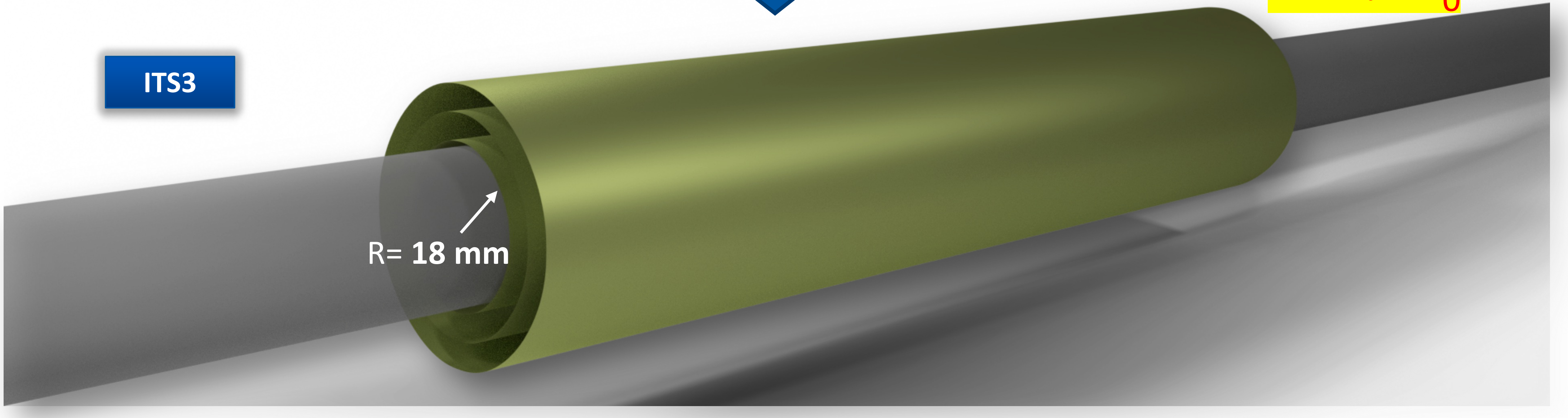




$0.35\% \ X_0$

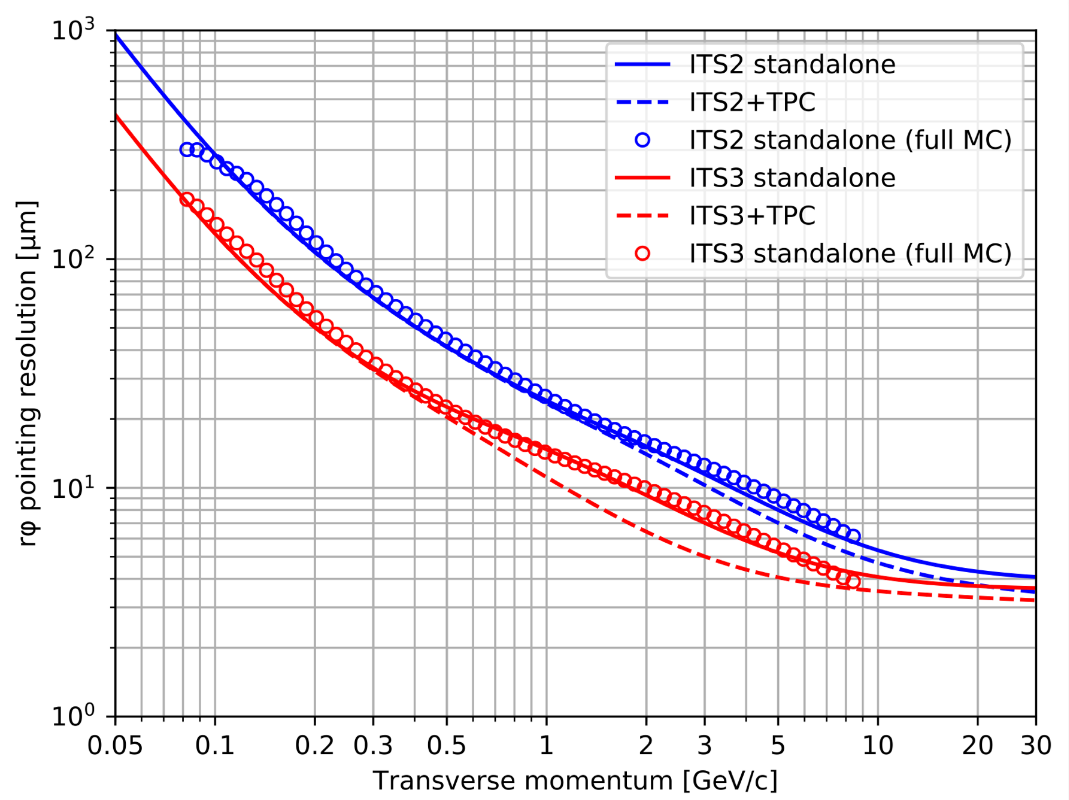
$0.05\% \ X_0$

ITS3



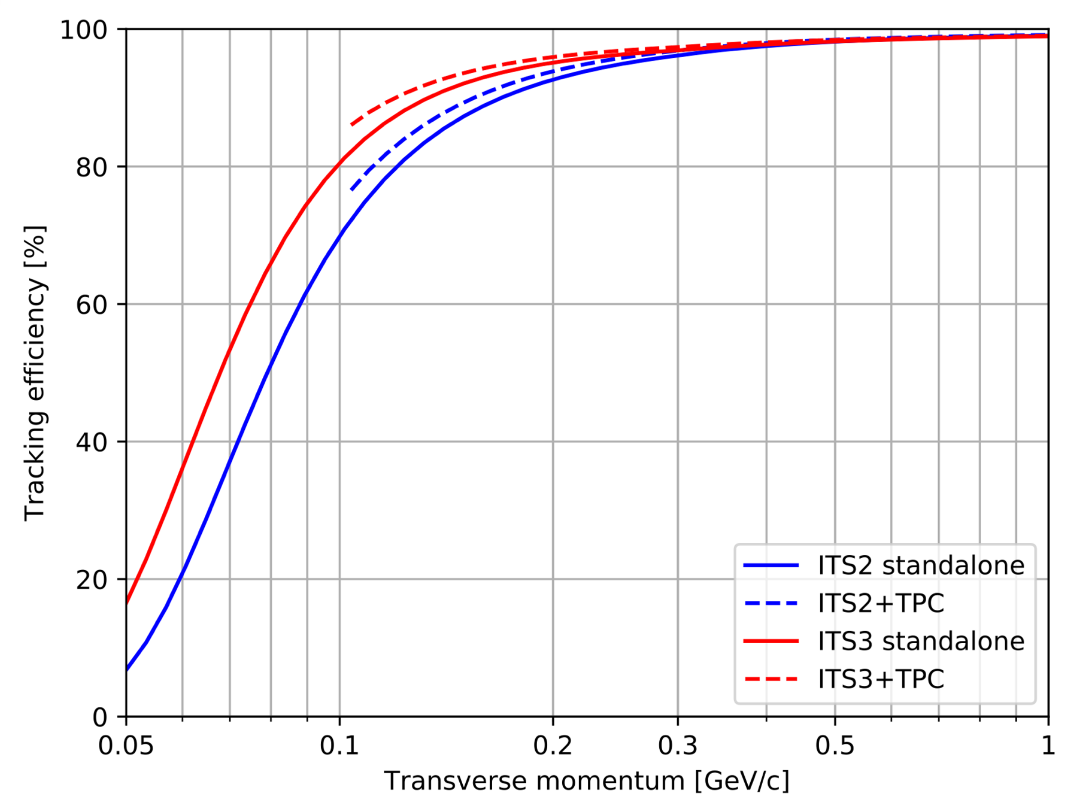
Enhanced Tracking Performance

pointing resolution



improvement of factor 2 over all momenta

tracking efficiency



large improvement for low transverse momenta

ITS3 Layout and Requirements

3 Cylindrical layers

Made with **6 curved wafer-scale single-die** Monolithic Active Pixel Sensors

Radii 18/24/30 mm, length **27 cm**

Thinned down to **<50 µm**

Position resolution ~5 µm

-> Pixels **Θ(20 µm)**

Electro-mechanical integration

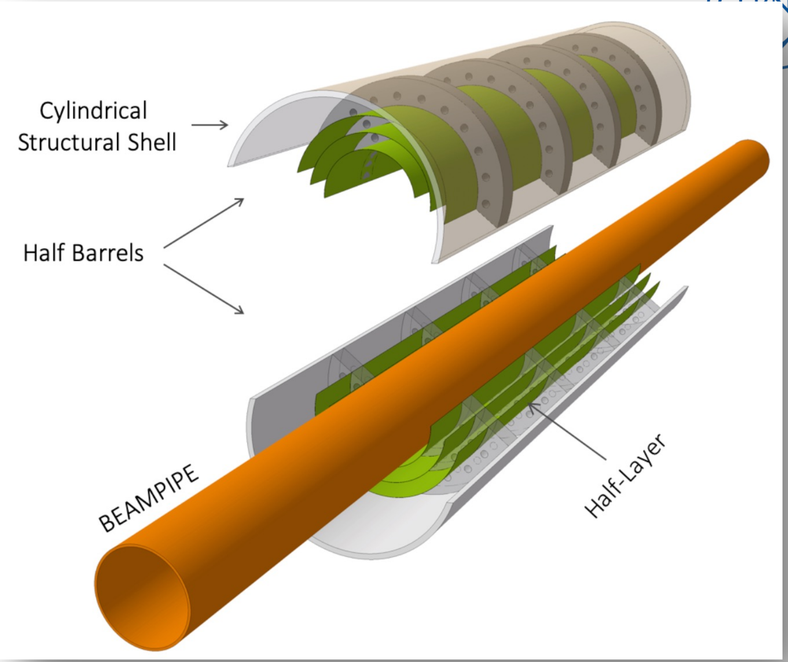
No flexible circuits in the active area

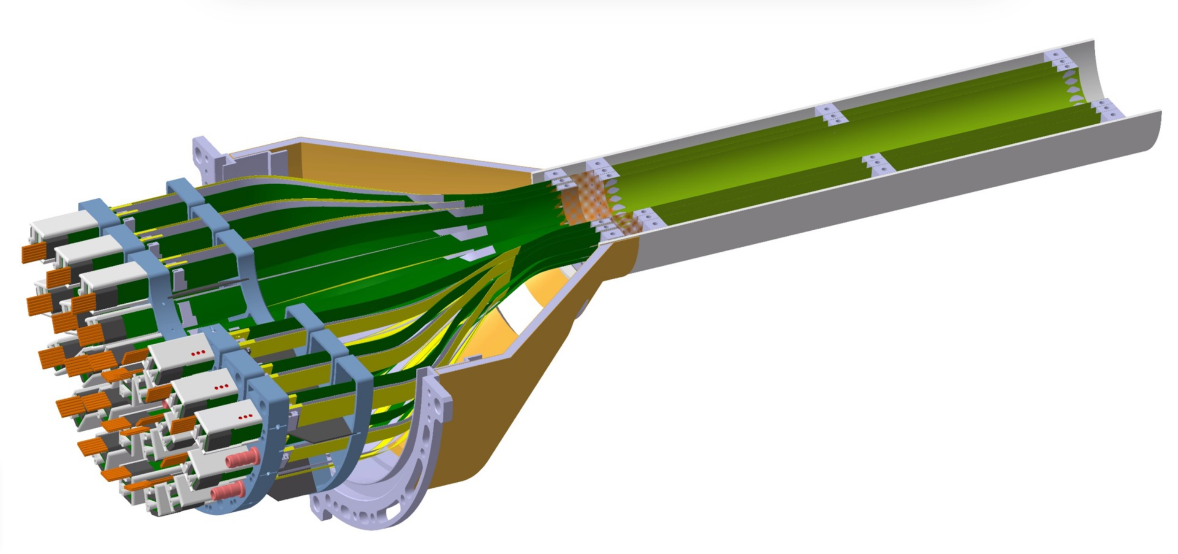
-> Distribute supply and transfer data on chip to the short edge

Cooling by air flow

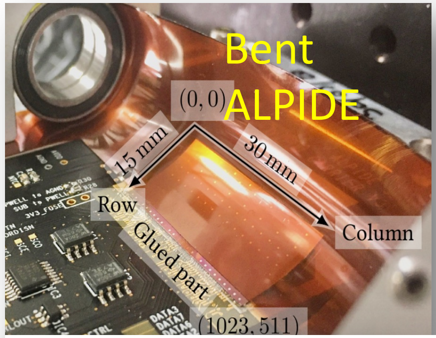
-> Dissipate less than 20 mW/cm^2

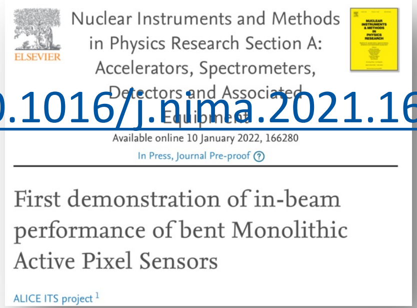
ALICE ITS3 LoI CERN-LHCC-2019-018 / LHCC-I-034





Can Bent Sensors Actually Work?




Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Available online 10 January 2022, 166280

In Press, Journal Pre-proof

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS project [1]

doi:10.1016/j.nima.2021.166280

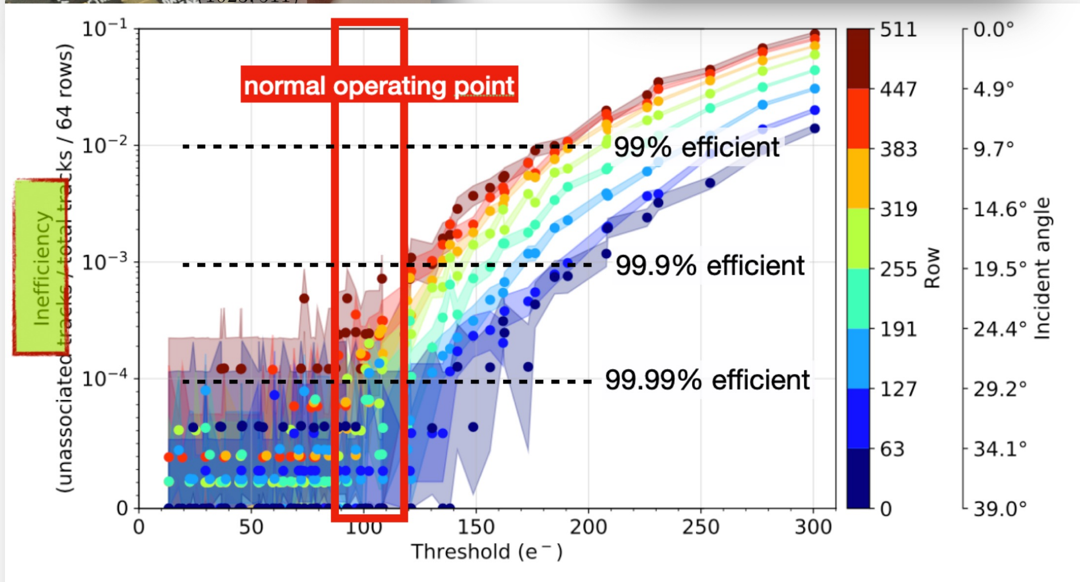
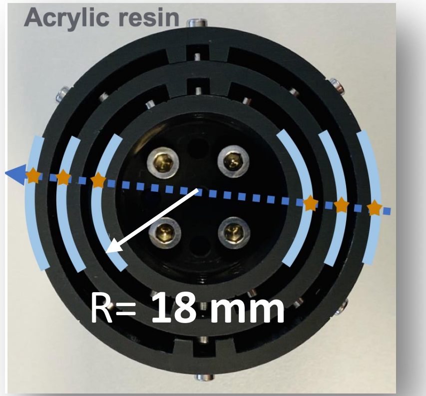
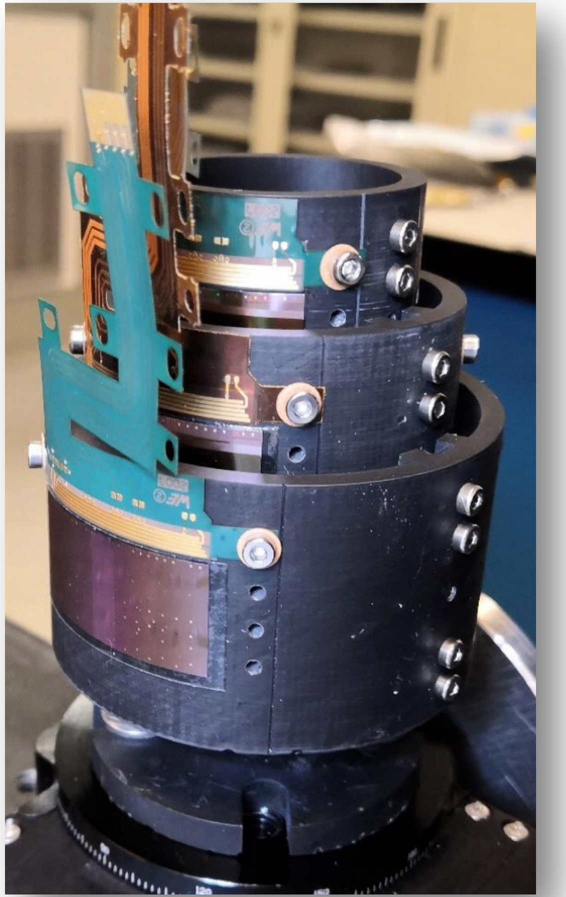


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

Series of beam tests with bent ALPIDE chips

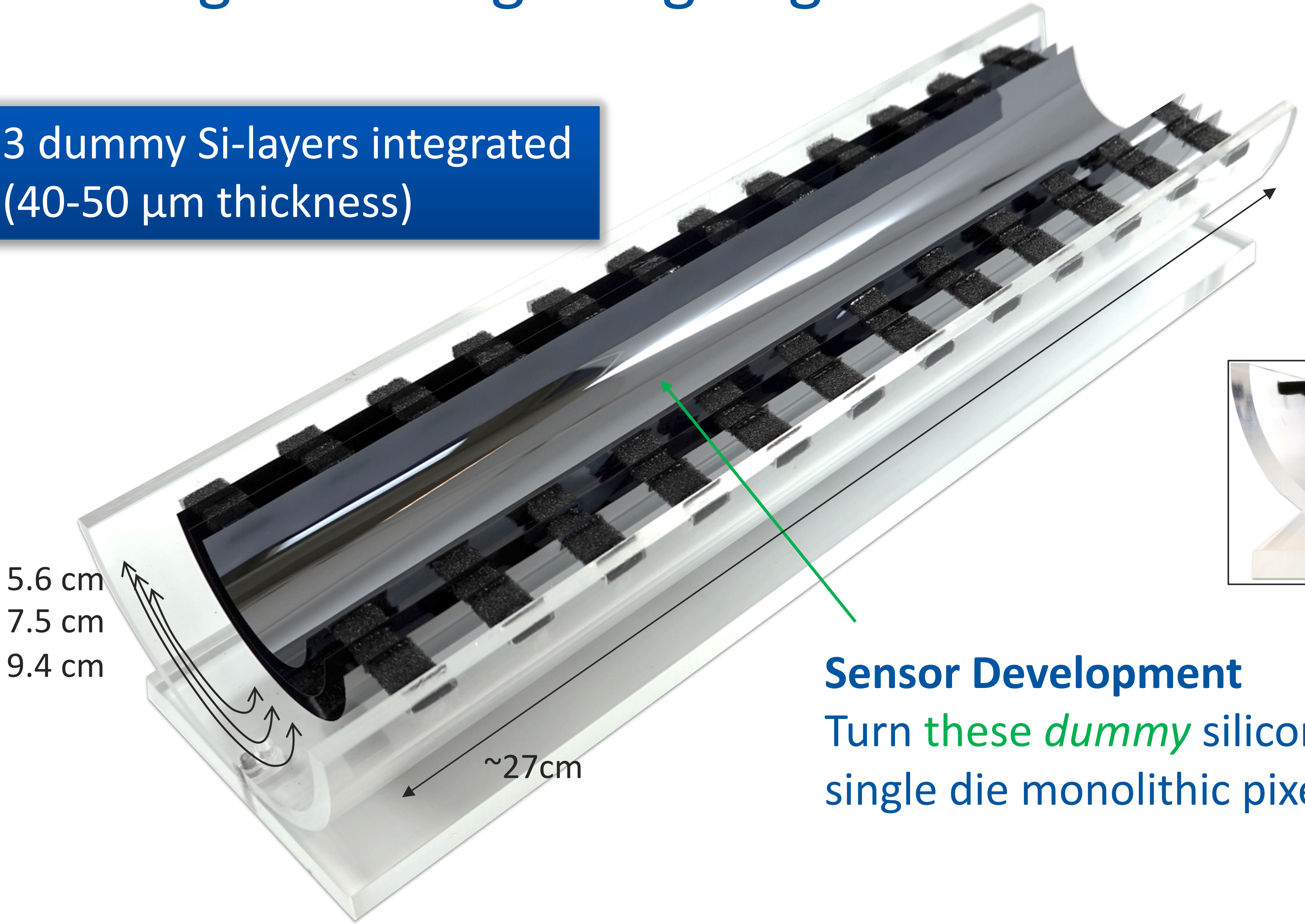


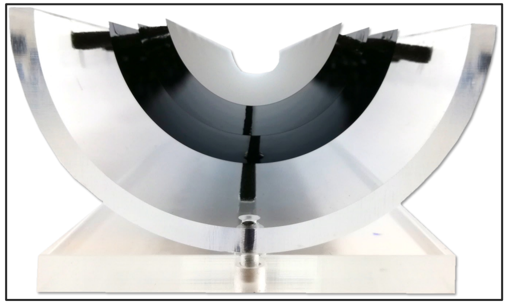


Working of bent sensors demonstrated with ALPIDE

Bending and Integrating large-thin silicon dies

3 dummy Si-layers integrated
(40-50 µm thickness)





Sensor Development

Turn these *dummy* silicon chips into *true* single die monolithic pixel sensors

Sensor Development Roadmap

Technology

TPSCo ISC 65 nm CMOS Imaging
300 mm wafers + Stitching

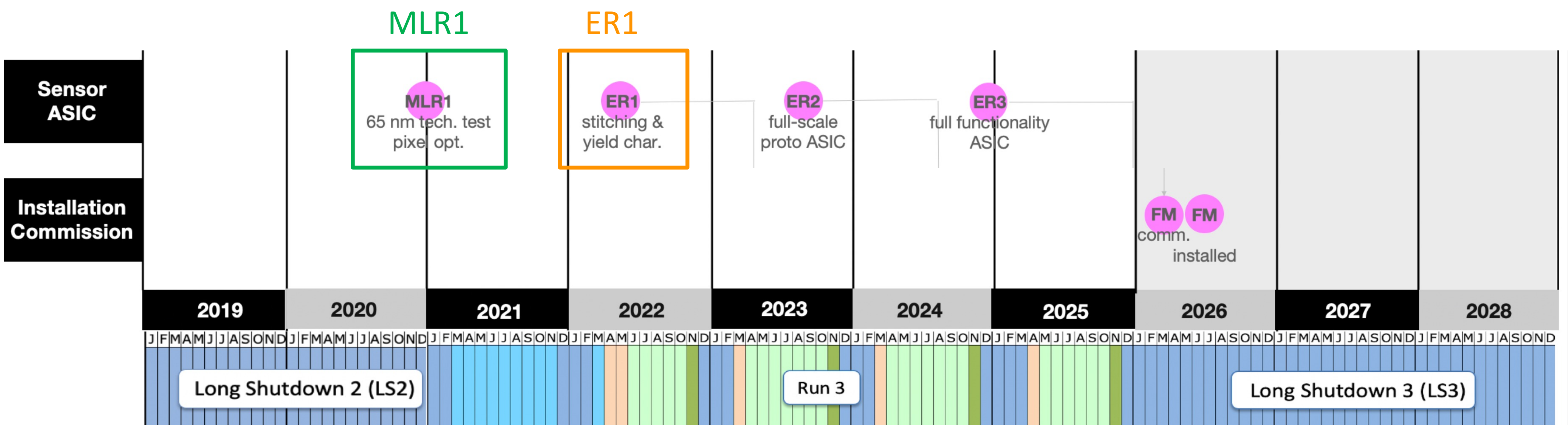
Silicon submissions

MLR1 (Q4 2020)

ER1 (Q2 2022)

Design activities framed within **CERN EP RnD WP1.2**

Share and coordinate development and design efforts by several teams and institutes inside and outside ALICE



MLR1 Submission – December 2020

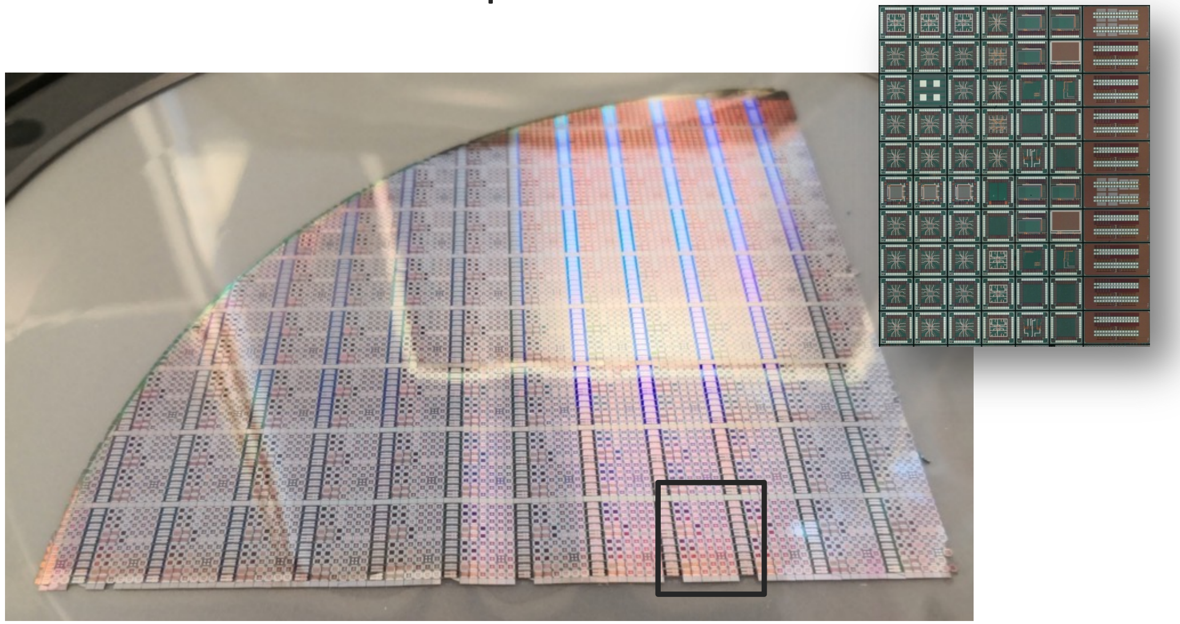
First submission in 65 nm CMOS Imaging

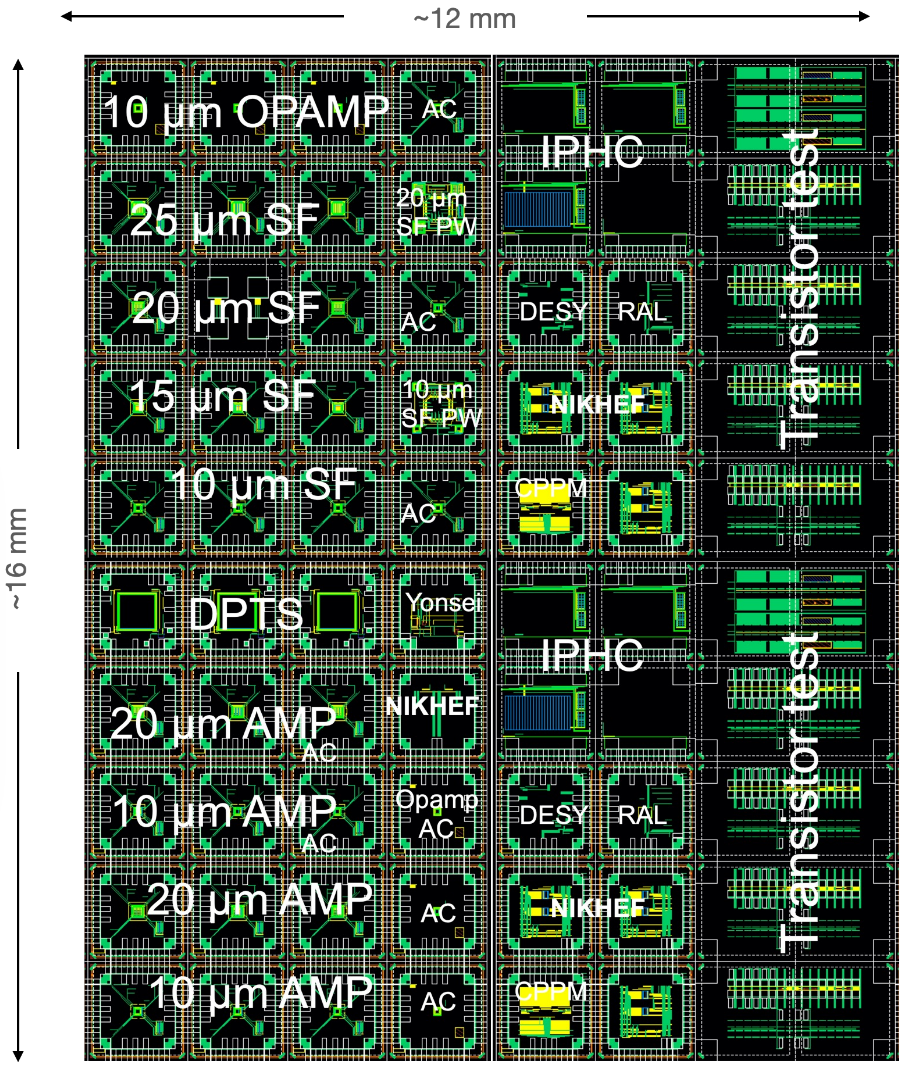
Learn technology features

Characterize devices

Prototype circuits, blocks and pixel structures

1.5×1.5 mm^2 test chips





MLR1 Learnings

Transistors Tests Structures

Working as expected and similar to other 65 nm technology characterized for HEP

Building blocks proven in silicon

Bandgap, DACs, Temperature sensor, VCO

Pixel Prototypes

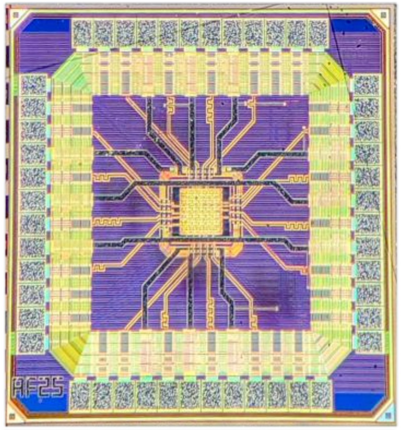
APTS, DPTS, CE65

Detailed characterisation ongoing

Process Optimisation

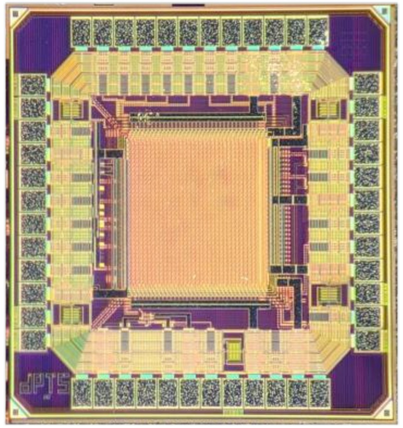
Increase margins on sensing performance

1.5 mm



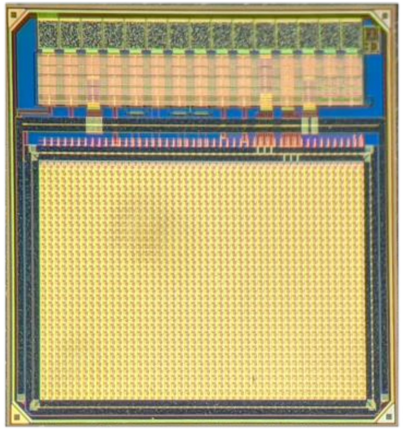
APTS

4x4 pixel matrix
10, 15, 20, 25 μm pitches
Pixel variants
Direct analogue readout



DPTS

32 × 32 pixels
15 μm pitch
Asynchronous digital readout
ToT information



CE65

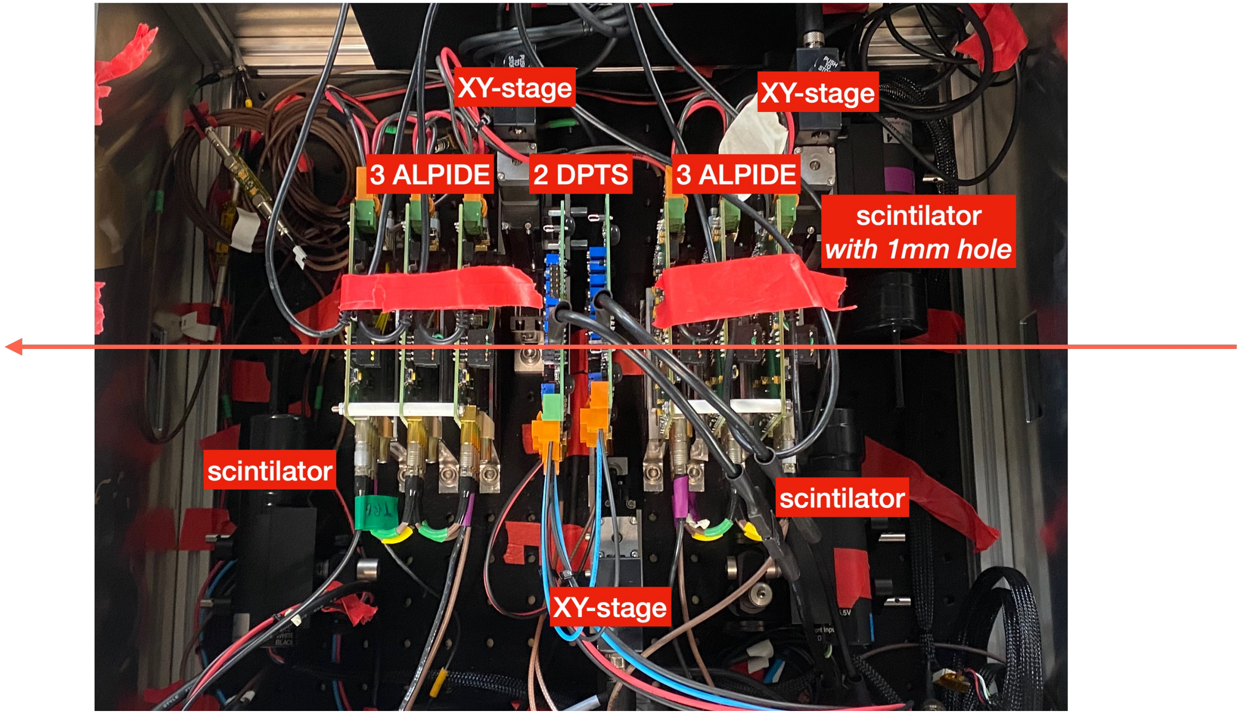
64 × 32 pixels
15 μm pitch
Rolling shutter analog readout
3 pixel architectures

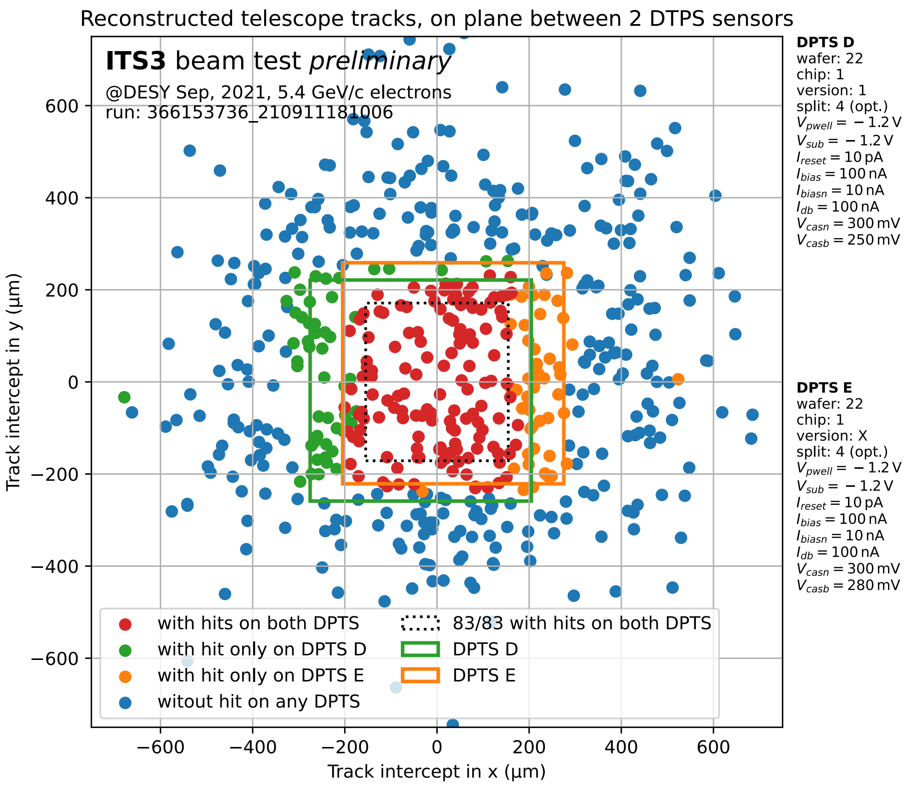
Selected Example: Beam Tests with DPTS chips

Detection efficiency >99.5%

Multiple beam tests

Detailed analysis ongoing, including irradiated samples

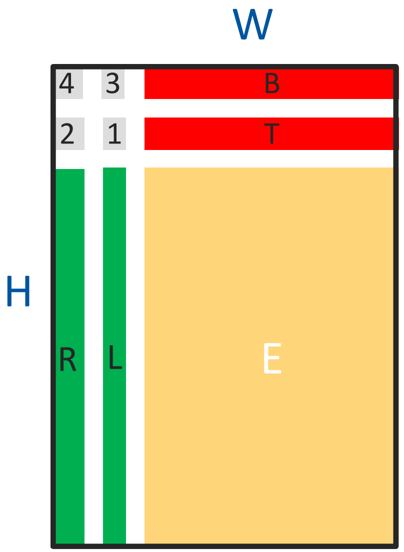




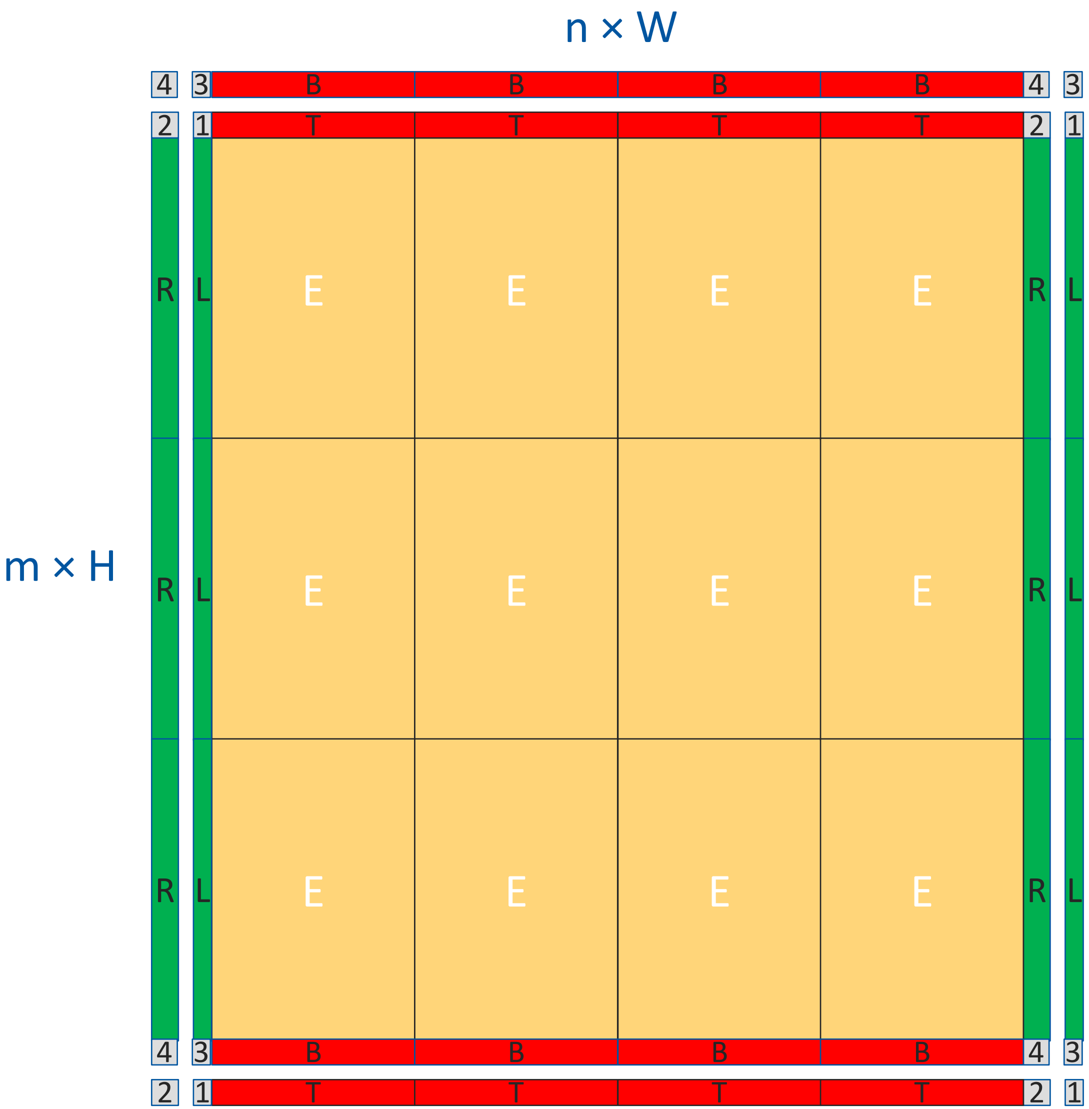
CERN EP Detector Seminar 24/09/2021

Stitching

Design Reticle (typ. 2×3 cm)



Circuits on wafer



ER1 Submission

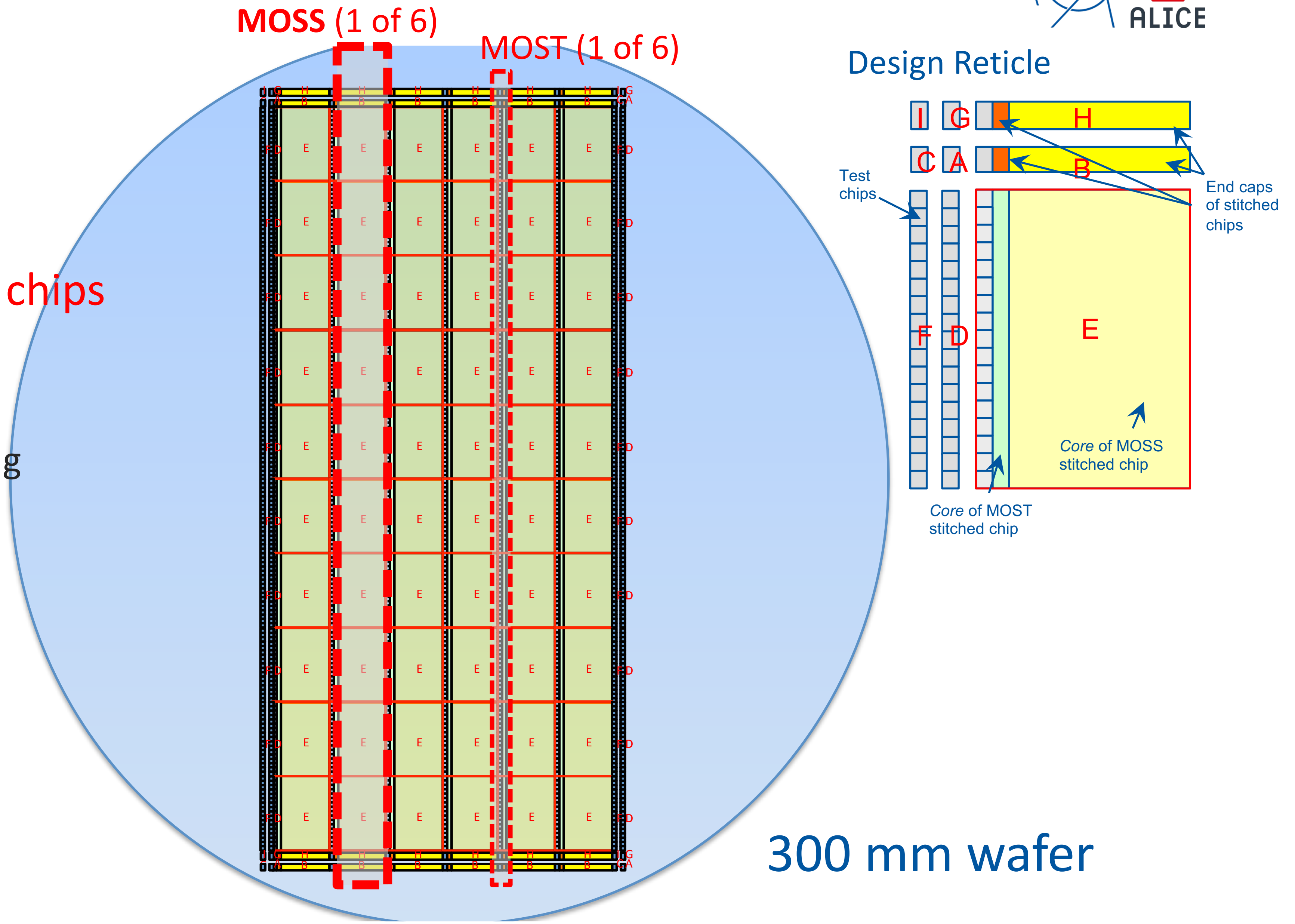
Learn and prove **stitching**

Two large *stitched* sensor chips (MOSS, MOST)

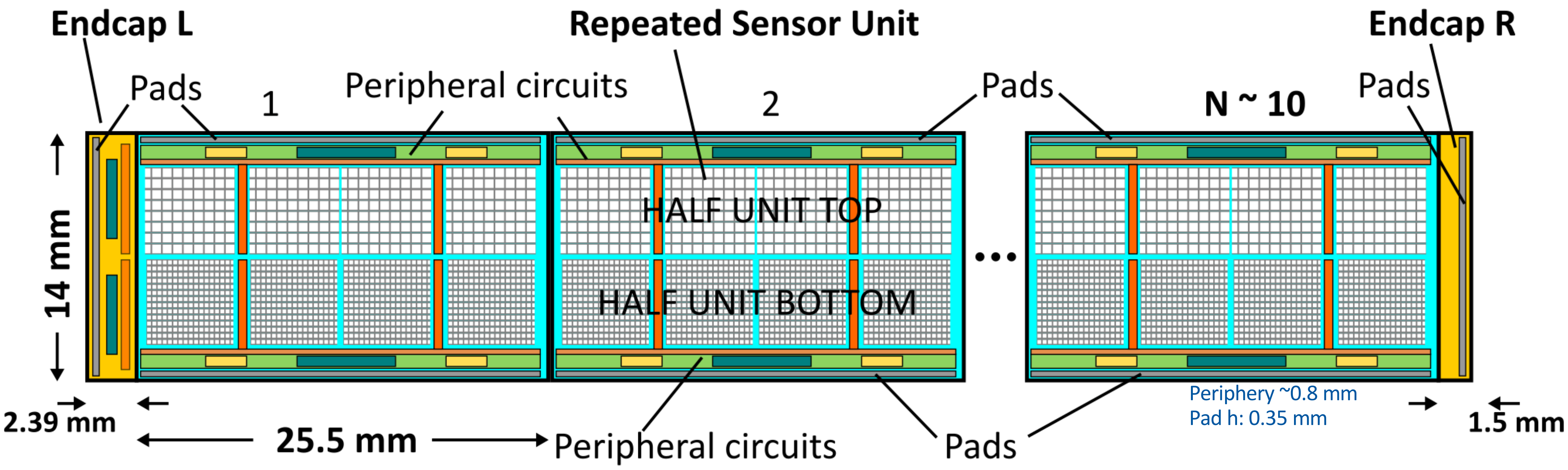
- Different approaches for resilience to manufacturing faults

Small test chips

- Pixel Prototypes
- Fast Serial Links



MOSS Monolithic Stitched Sensor Prototype



Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

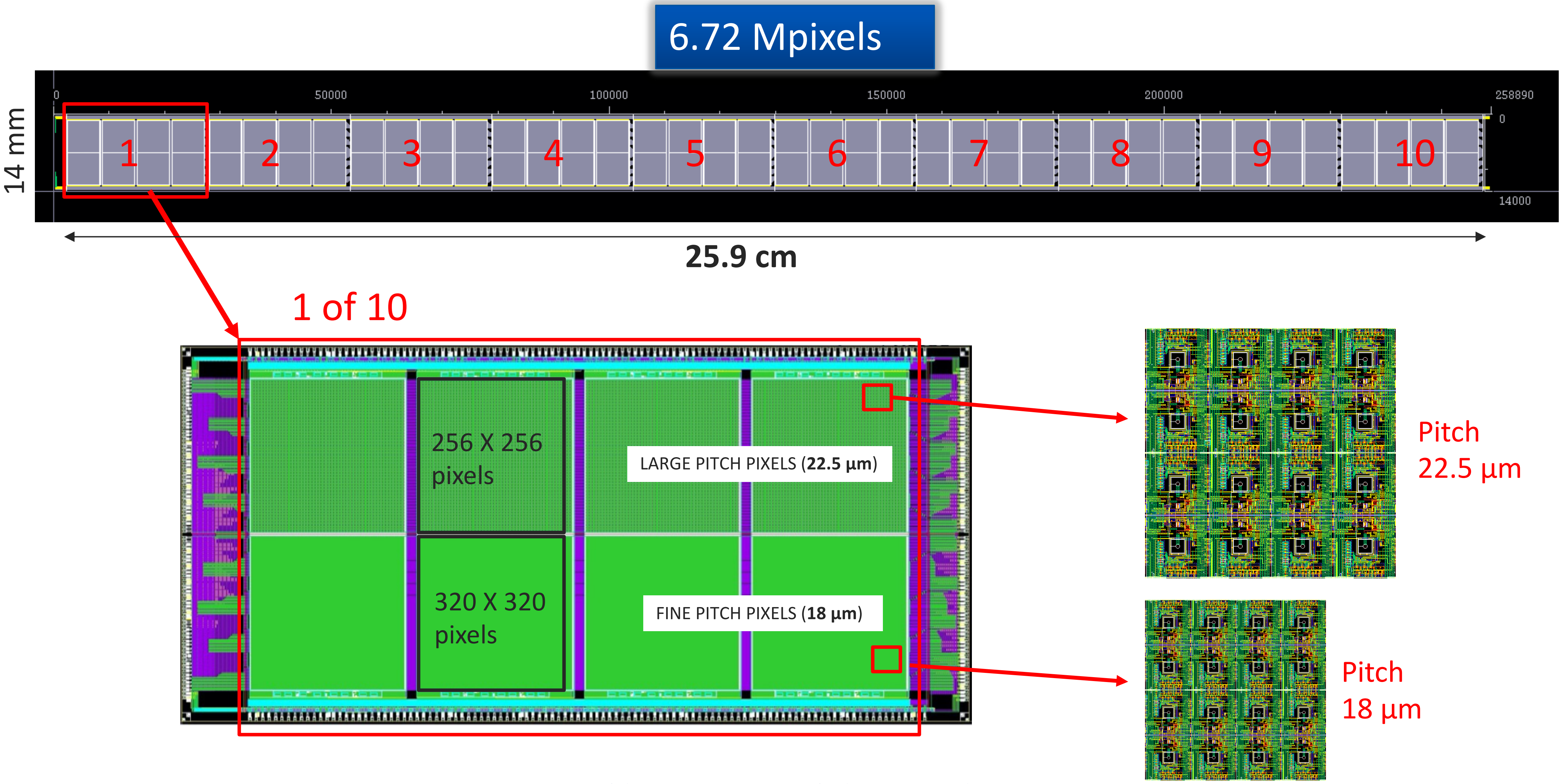
Repeated units abutting on short edges

Repeated Sensor Unit, Endcap Left, Endcap Right

Functionally independent

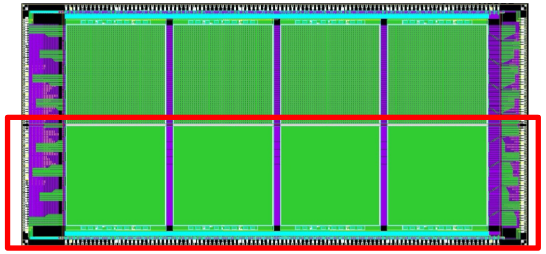
Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

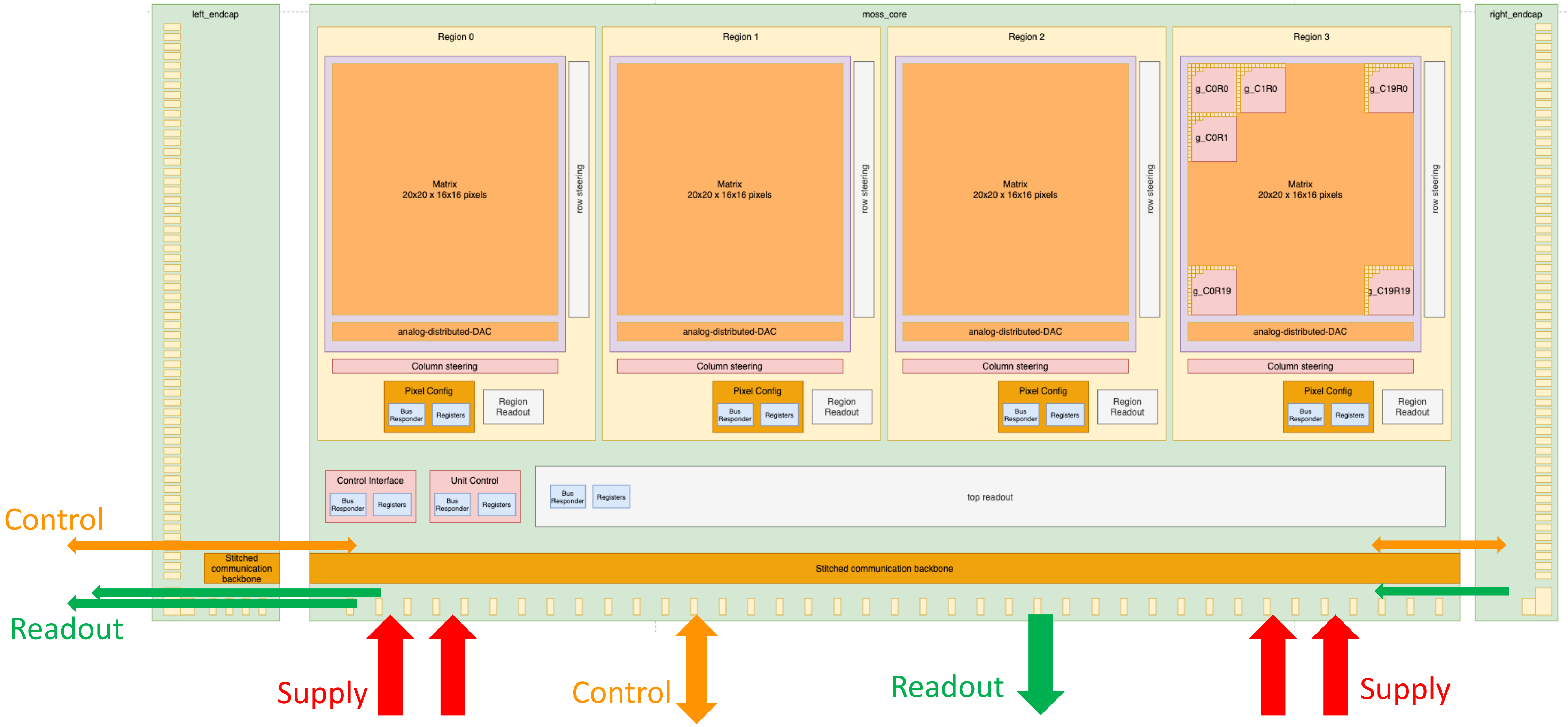
MOSS Layout



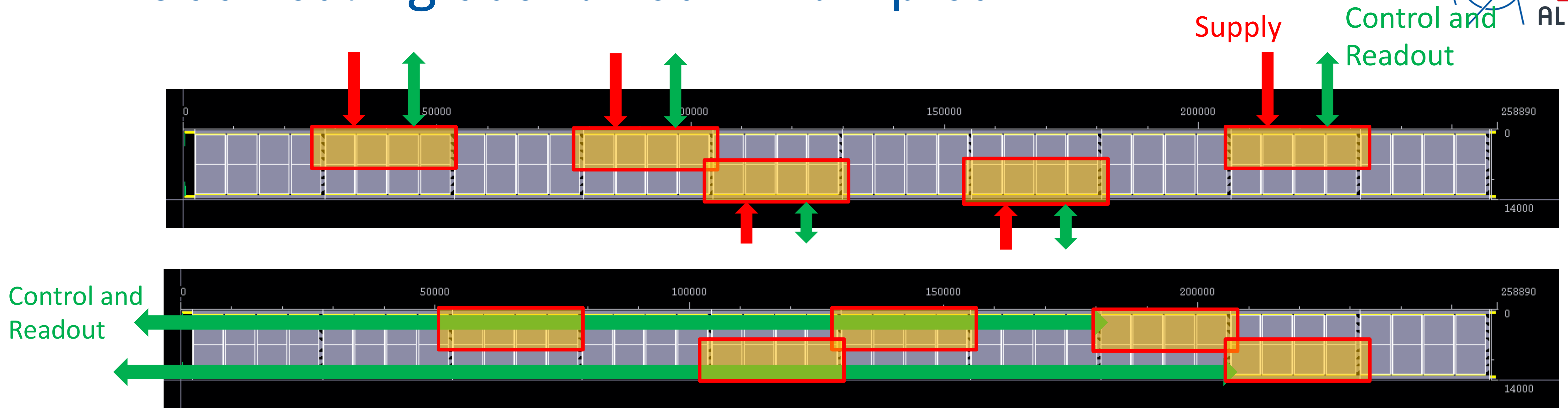
6.72 Mpixels
14 mm
0
50000
100000
150000
200000
258890
0
14000
1
2
3
4
5
6
7
8
9
10
25.9 cm
1 of 10
256 X 256 pixels
320 X 320 pixels
LARGE PITCH PIXELS (**22.5 µm**)
FINE PITCH PIXELS (**18 µm**)
Pitch 22.5 µm
Pitch 18 µm

MOSS - Half Unit





MOSS Testing Scenarios - Examples



Test the sub-units independently

Study manufacturing yield

- Functional yield at half unit, block, column/row/pixel level granularity
- Possible dependence on pixel pitch and layout density?

Study noise, threshold, position resolution vs pixel variants

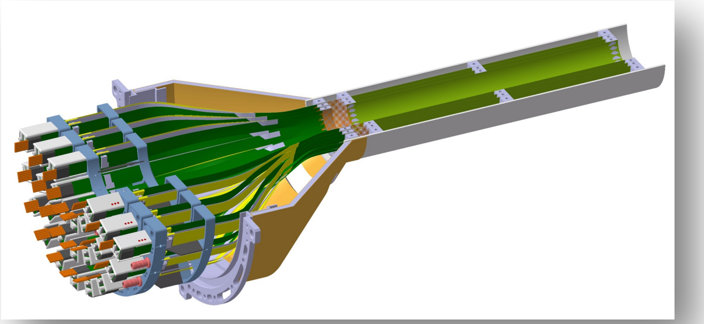
Summary

ALICE ITS3

Replace 3 Inner Layers of ITS2 with **wafer scale bent** monolithic pixel sensors

Proven operation of thinned sensors **bent at 18 mm** radius

Built full scale mechanical prototype



Sensor Developments

TPSCo 65 nm technology validated for particle sensing

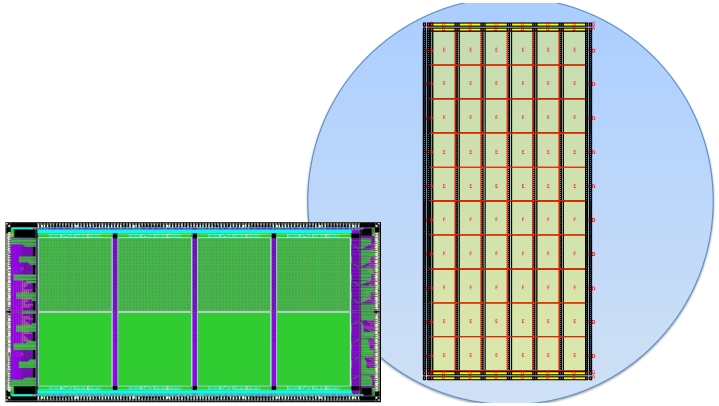
Detailed characterization of MLR1 prototypes ongoing

Next: learn stitching with ER1 submission

MOSS chip prototype

14 mm × 25.9 cm stitched sensor chip

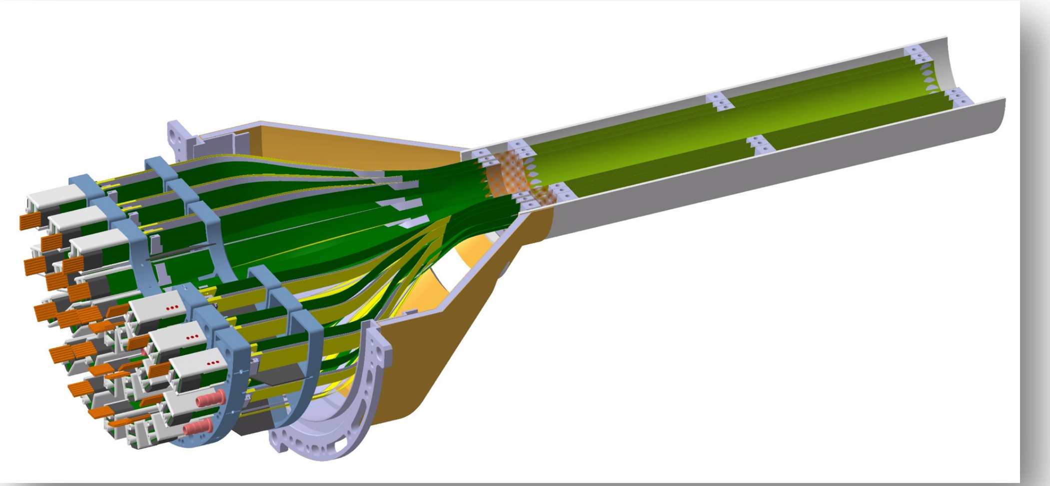
Study yield, power and signal distribution, large pixel arrays



ALICE ITS3 is pioneering large area MAPS sensors and bending.
This is sparking the interest of many groups for other experiments and applications.

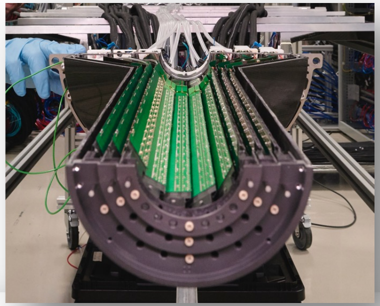
SPARE SLIDES

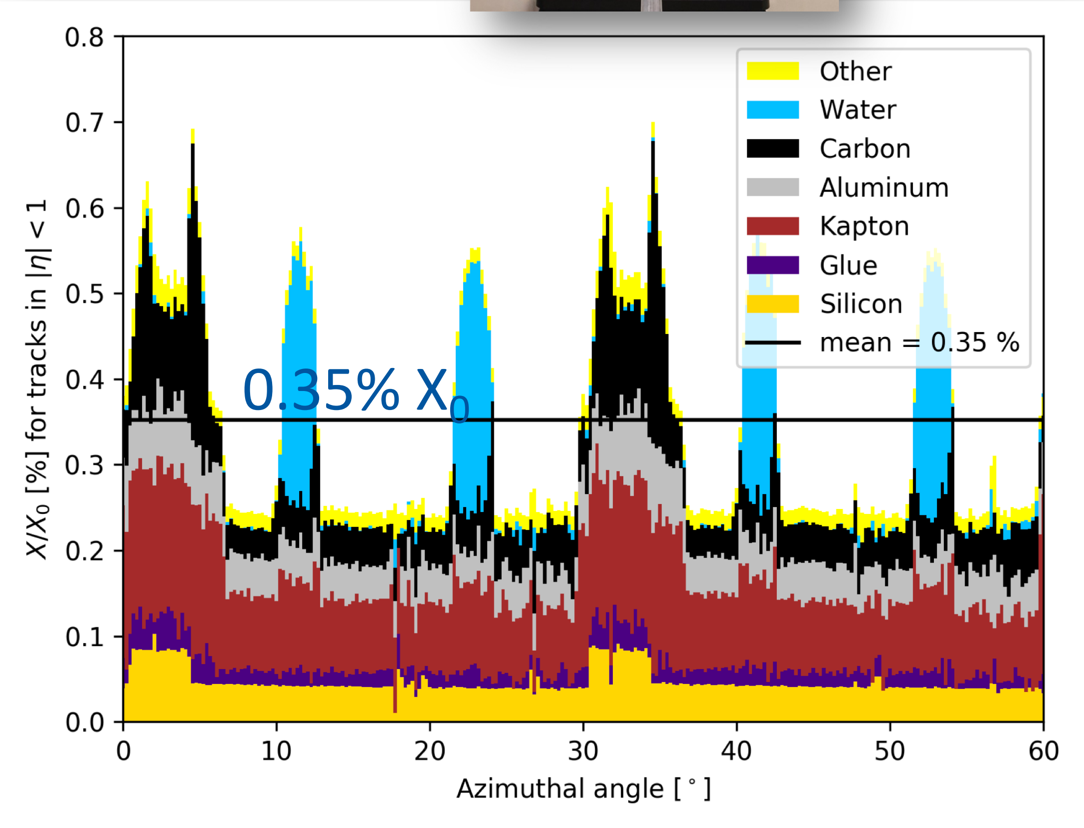
Pb-Pb Interaction Rate	50 kHz
Particle Flux	2.2 MHz/cm^2
TID	<10 kGy
NIEL	1×10^{13} 1 MeV n_{eq} cm^{-2}



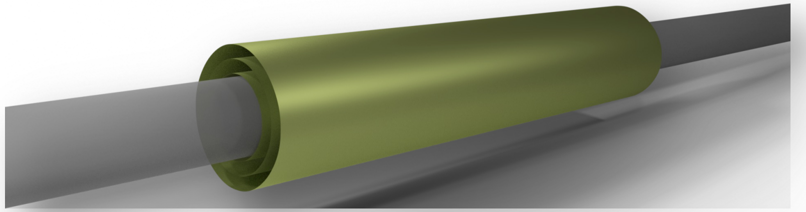
Reduce Material Budget

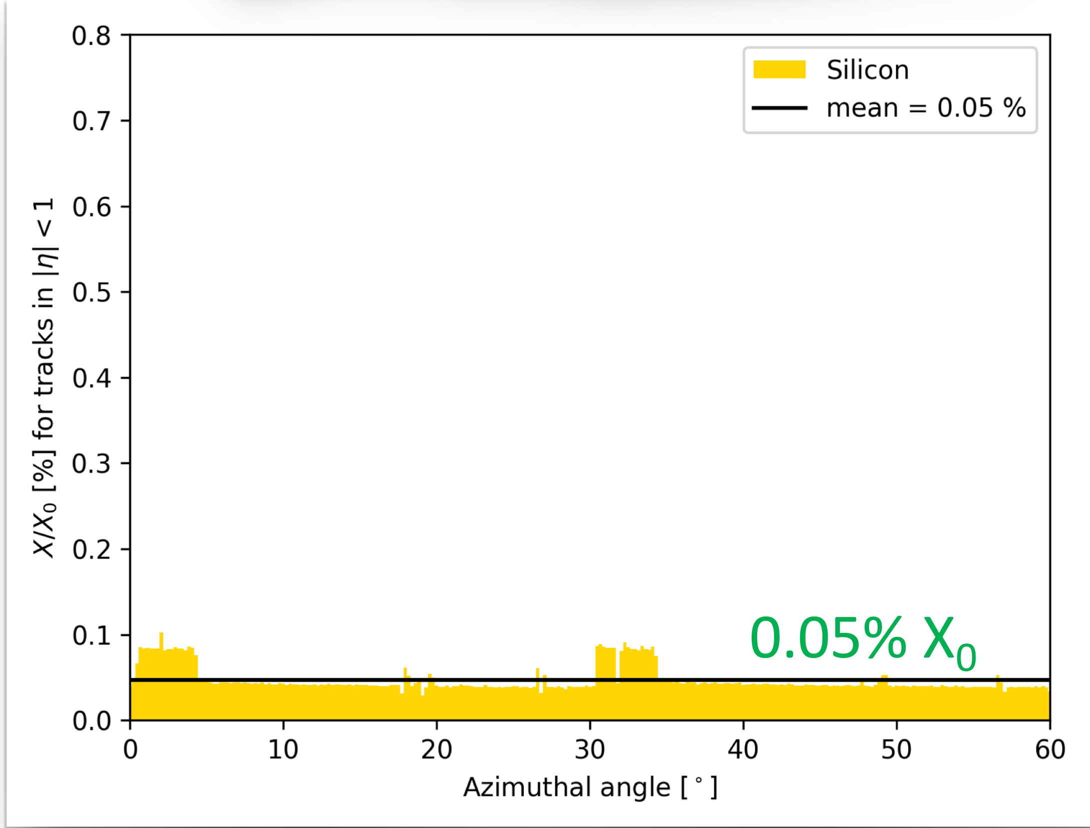
ITS2 Inner Barrel





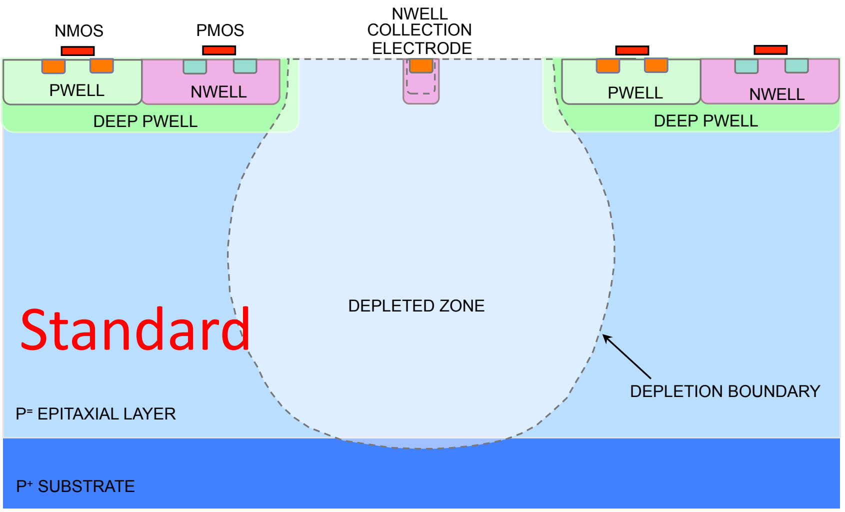
ITS3

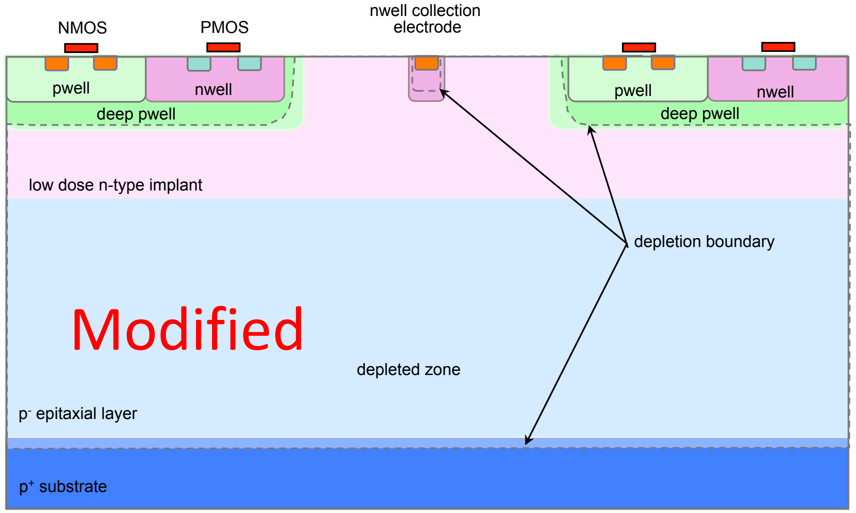


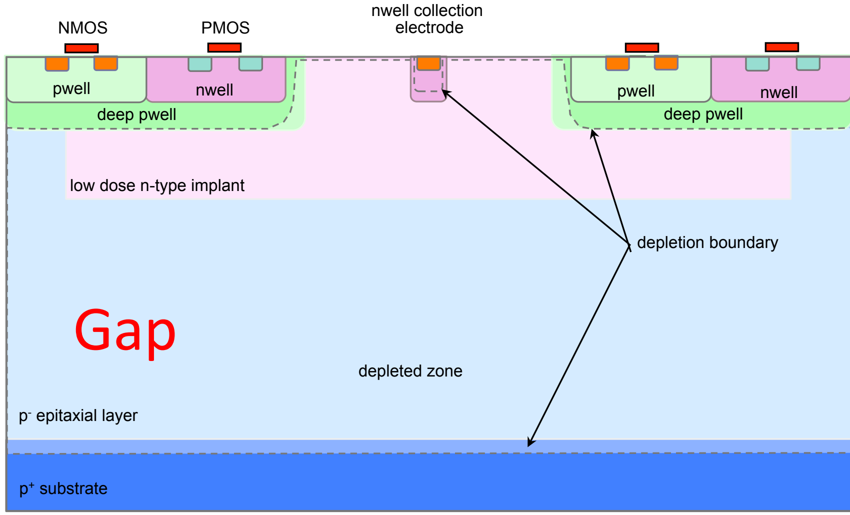


Process modifications

Similar optimization as in 180nm, but modifications needed even more in 65 nm for good charge collection.







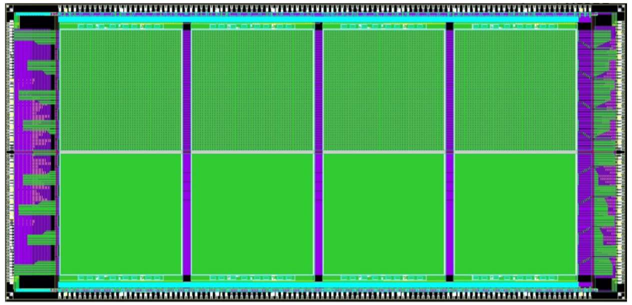
https://doi.org/10.1016/j.nima.2017.07.046 (180nm)

https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed →

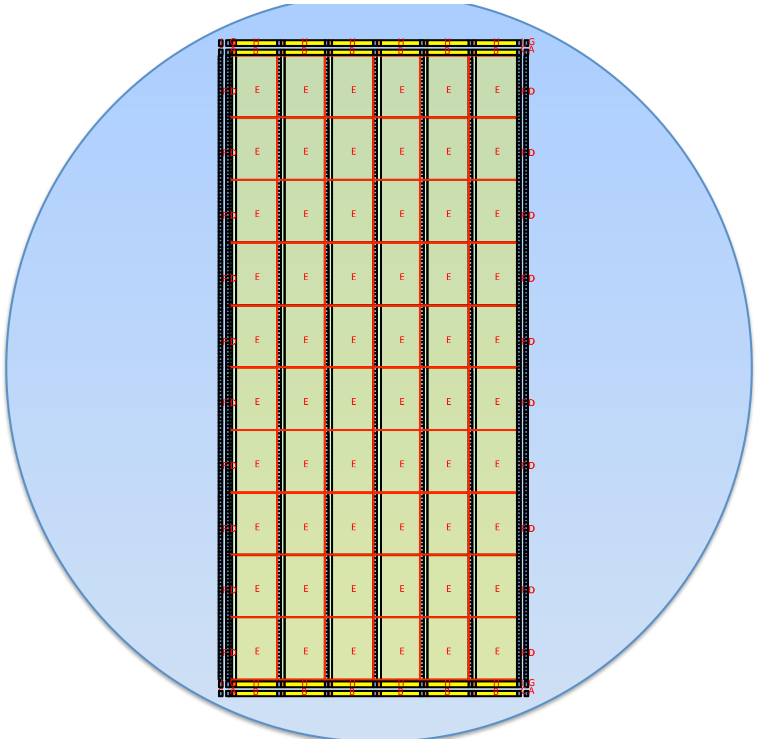
← Charge sharing

MOSS Design Challenges



Stitching

Significant reduction of circuit density



Long-range power distribution and signals transmission

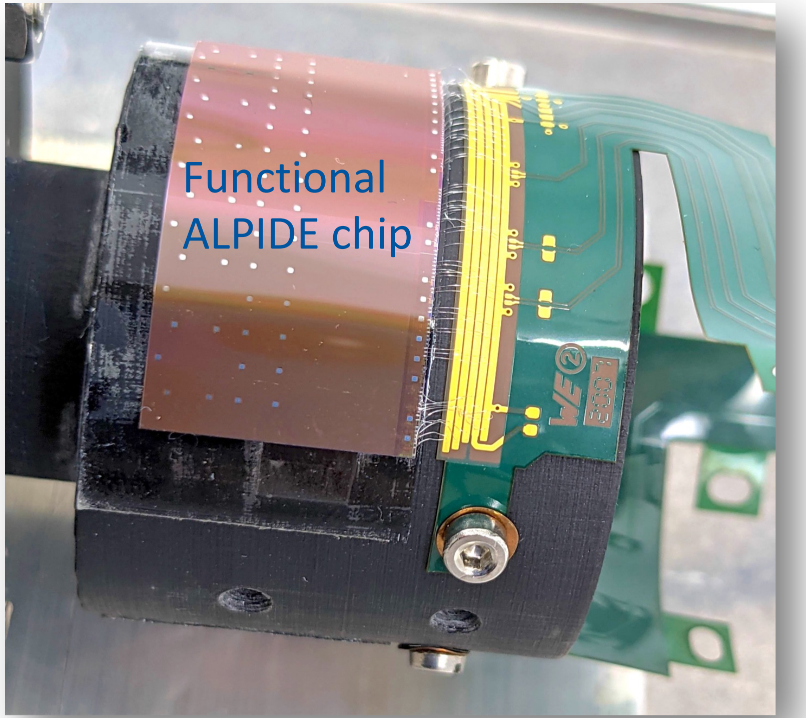
Large number of independent power domains

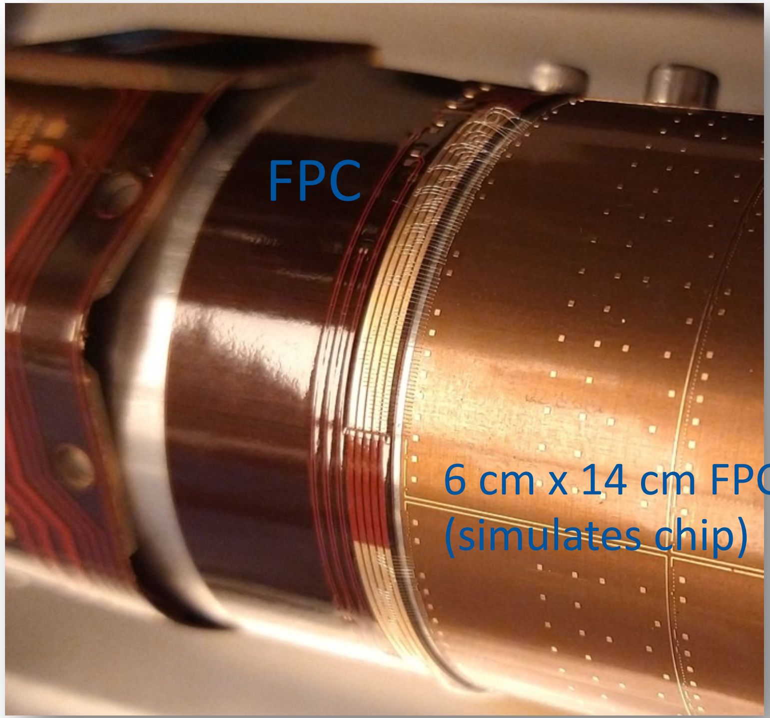
Leakage currents

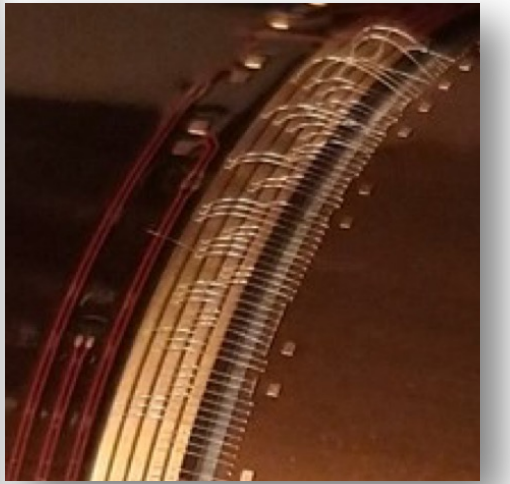
Development of Interconnects

Bonding on curved chips and circuits

Procedures, jigs, mandrels, integration
with bonding machine







ITS2 Inner Barrel Stave