A SIPM MULTICHANNEL ASIC FOR HIGH RESOLUTION CHERENKOV TELESCOPES (SMART) DEVELOPED FOR THE PSCT CAMERA TELESCOPE

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Frontier Detectors for Frontier Physics
15th Pisa meeting on advanced detectors
La Biodola, Isola d'Elba

INFN BARI
Istituto Nazionale di Fisica Nucleare
Sezione di Bari

The pSCT design

The Schwarzschild Couder Telescope for CTA

Dual-mirror medium size telescope:

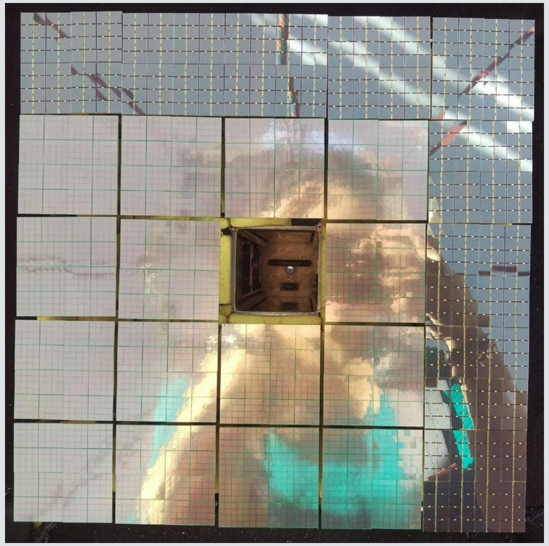
- Compensation of optical aberrations & de-magnification of images
- Compact (80 cm) and high-resolution camera with >11k 6x6 mm^2 SiPM pixels (8° FoV)

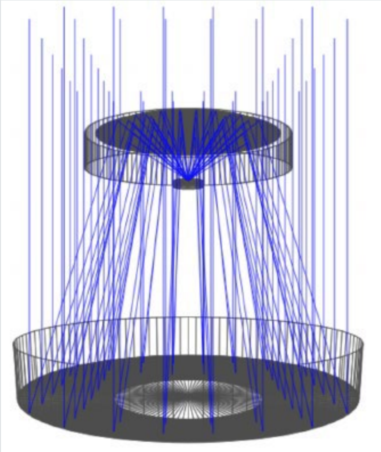
Current camera:

- 1.5k pixels only (2.7° FoV)
- FEE based on discrete pre-amplifier + TARGET-7

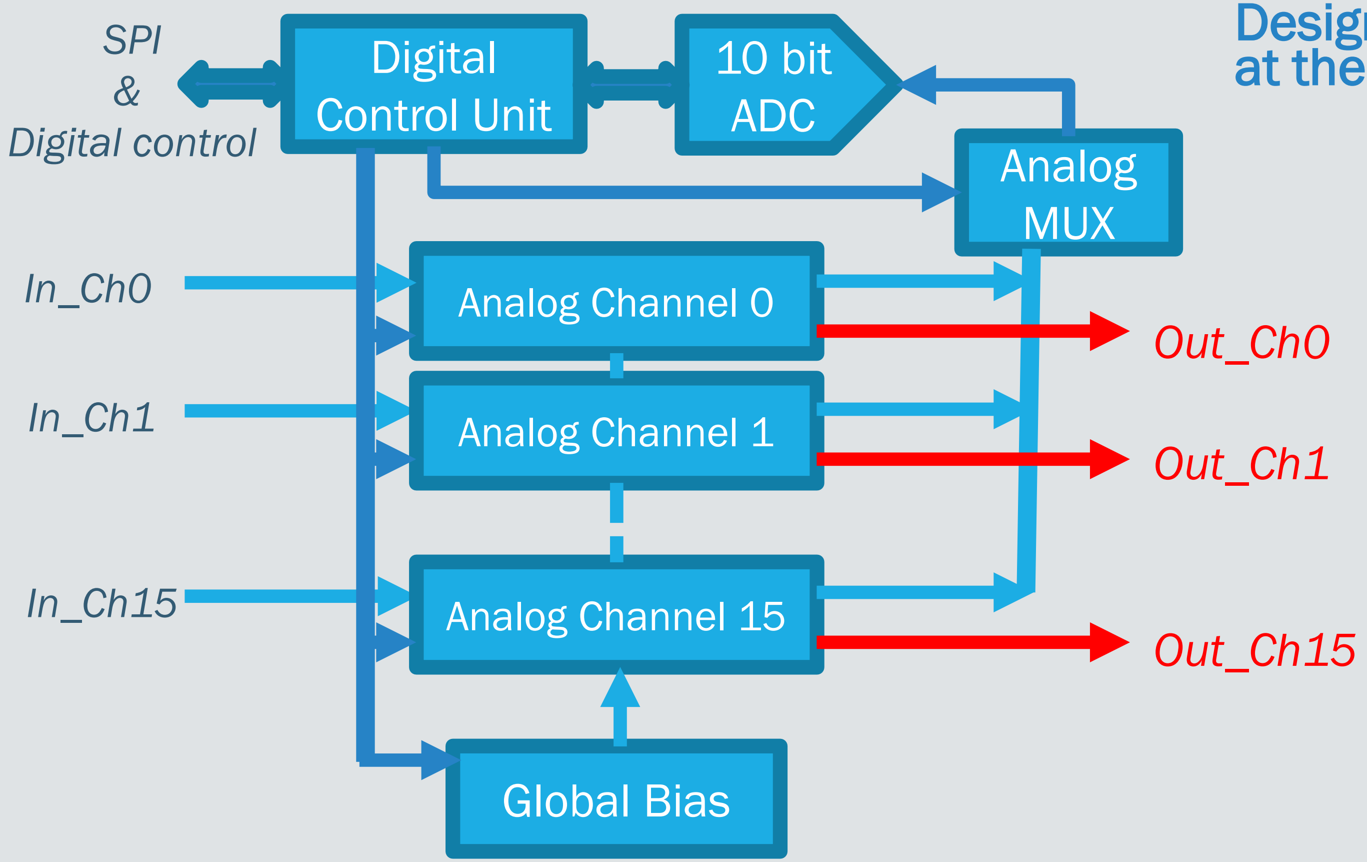
Upgraded camera (ongoing)

- Full camera (>11k pixels) with FBK NUV-HD SiPMs
- FEE based on SMART pre-amplifier +TARGET-C + T5TEA





a SiPM Multichannel Asic for high Resolution Cherenkov Telescopes

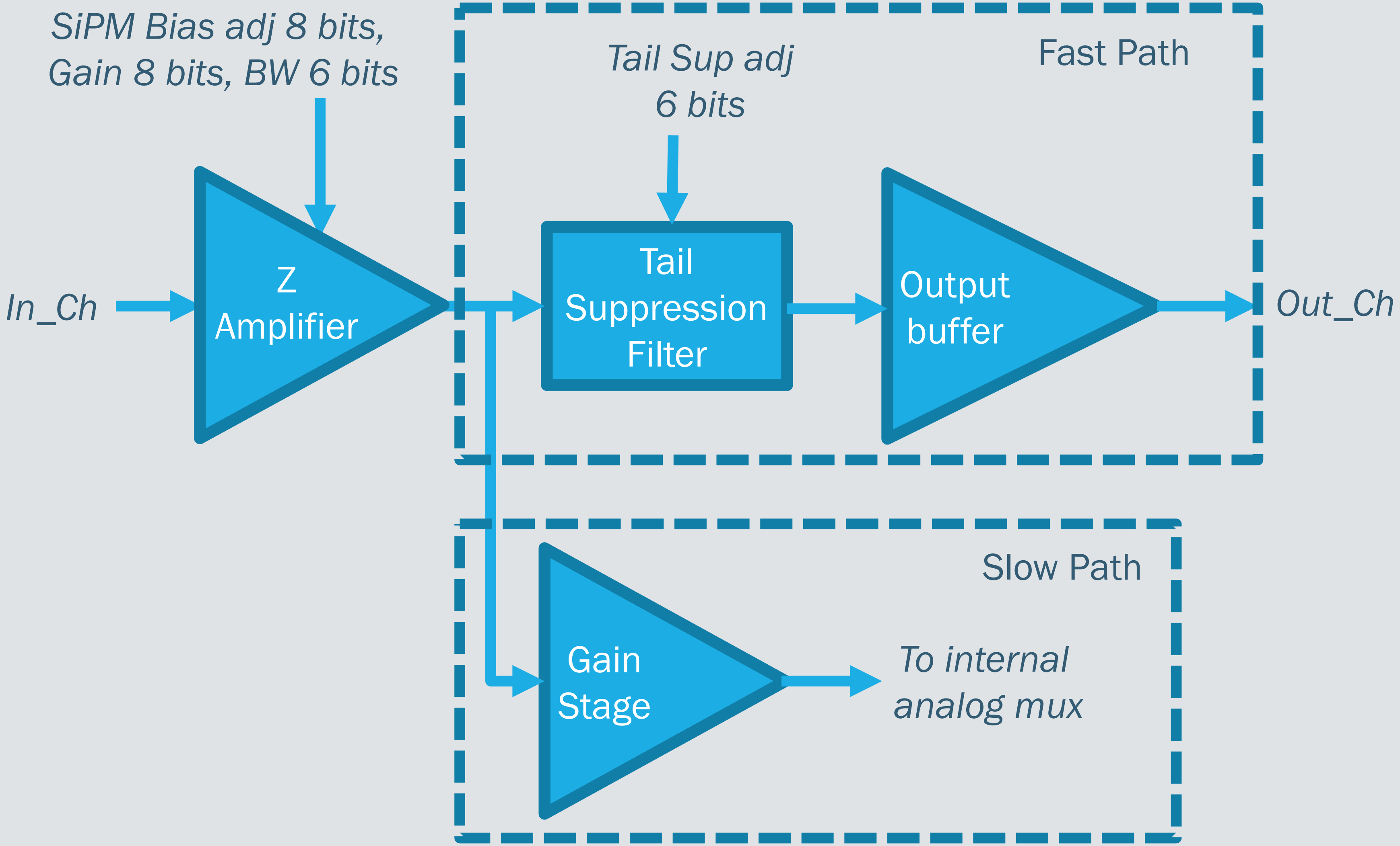


Designed by F. Licciulli & G. De Robertis at the Electronics CAD INFN Bari

Pre-amplifier designed for photon counting

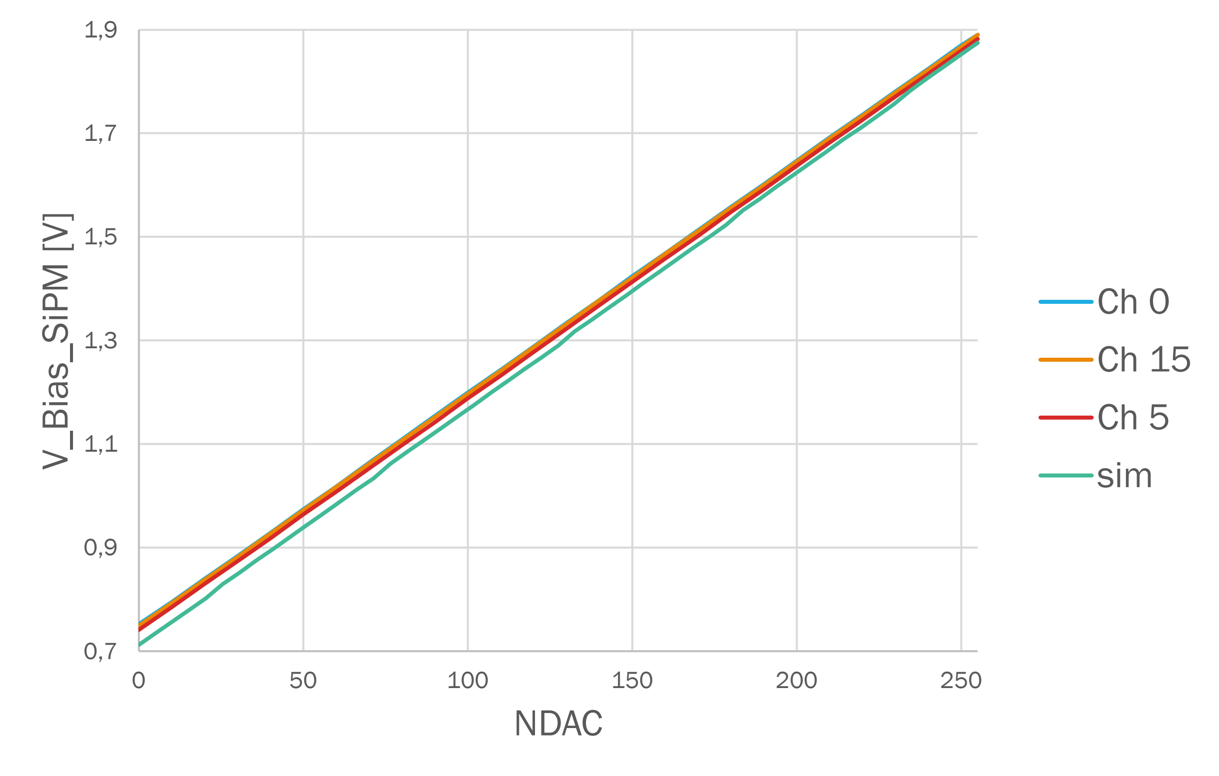
- 16-channel trans-impedance amplifier
- 20-bit global adjustment: gain (8 bits), bandwidth (6 bits), PZ (6 bits)
- 8-bit DAC for SiPM bias fine tuning (1 DAC/ch)
- Slow monitoring of SiPM current (10-bit ADC)
- 1 MHz LVDS SPI interface
- 600 mV dynamic range

Channel architecture



DAC Bias voltage

- Measurement of the channel input voltage as a function of the DAC configuration



The SiPM bias voltage is:

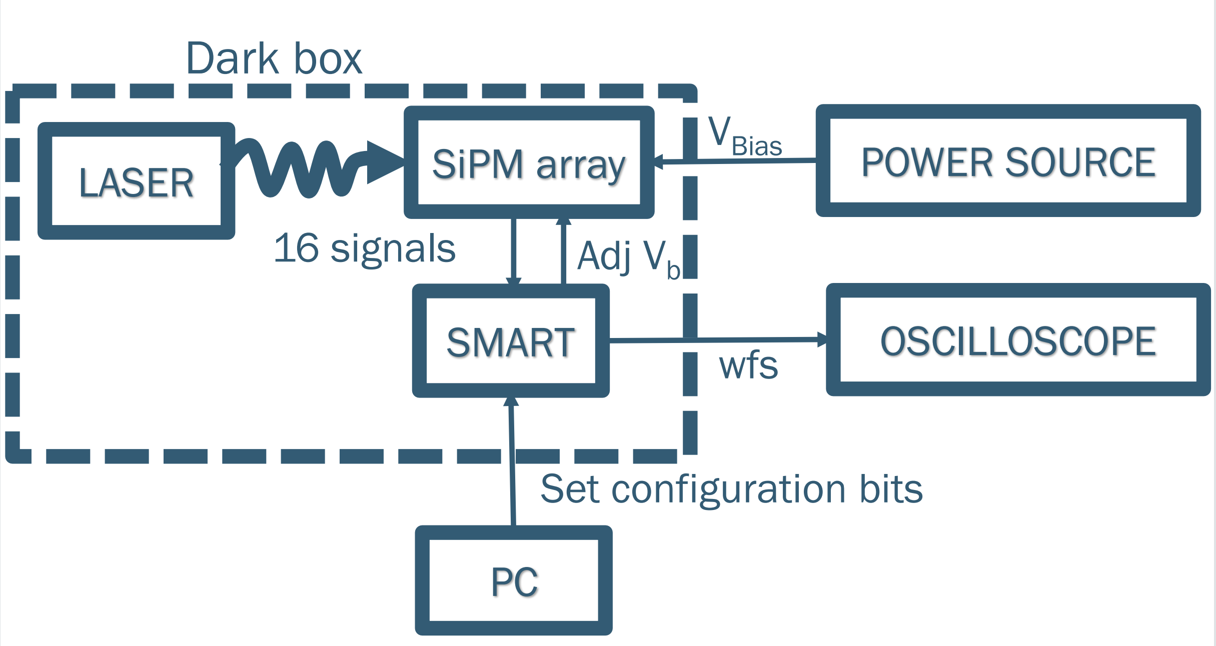
$$V_{bias,\,SiPM} = V_{external} - V_{DAC,\,channel}$$

$$V_{DAC} \in [0.75, 1.9]\ V$$

V_{DAC} range is approximately 1.2 V

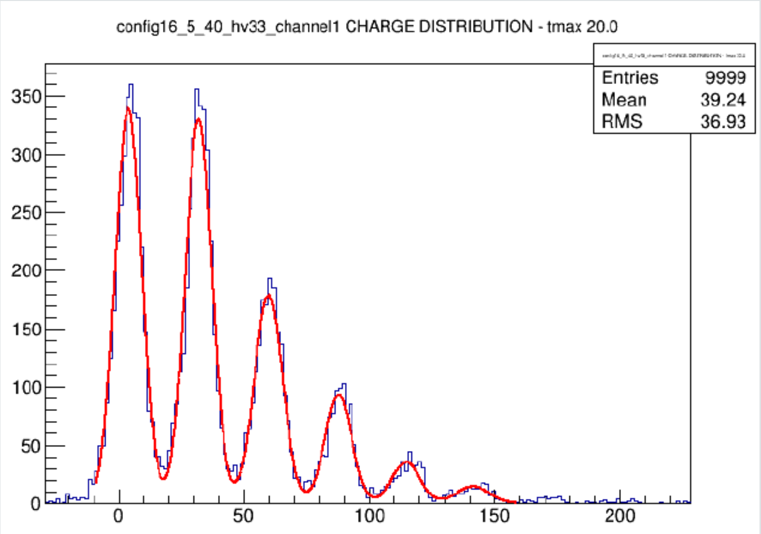
SMART characterization

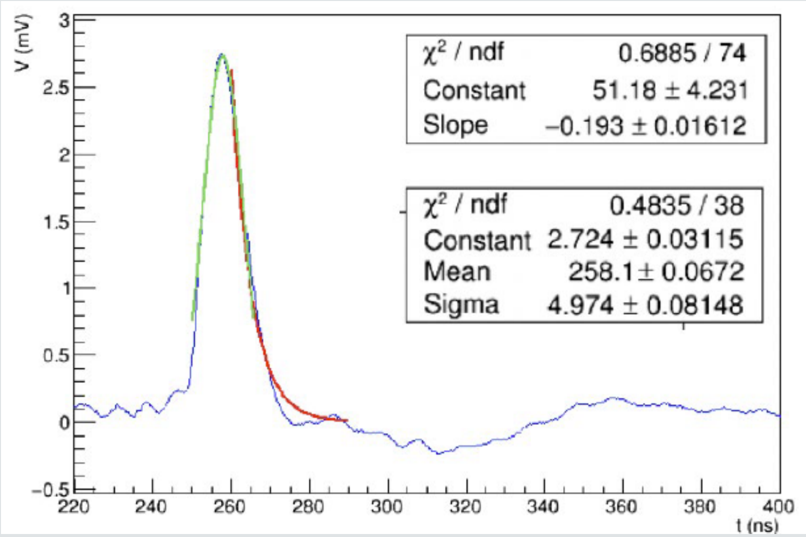
- We measured gain, signal-to-noise ratio and pulse width as a function of configuration bits
- 3 parameters changed
  - *R : gain resistance*
  - *C : filtering capacitance*
  - *PZ: pole zero cancellation*
- External PZ fixed with discrete components
- Tests at different bias voltage (V_{Bias} = 33, 35, 37 V)
- We placed a mask on the SiPM array in order to reduce any cross-talk contribution

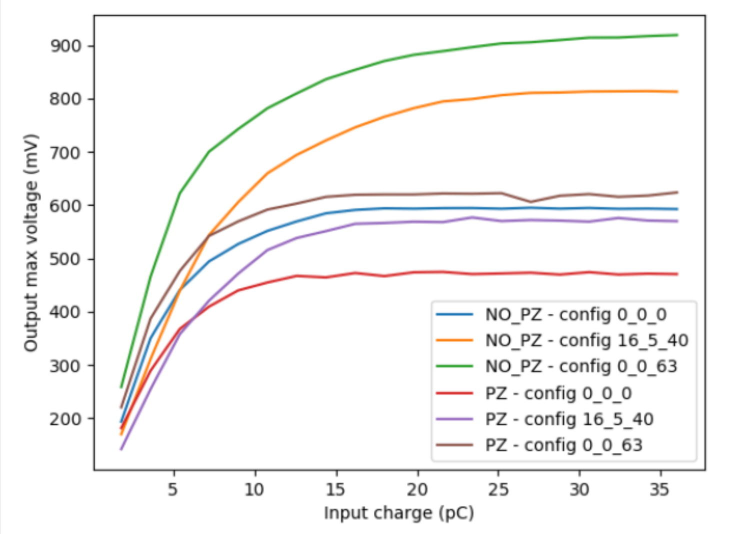


SMART characterization

SMART performances tested with FBK NUV-HD 6x6mm^2 SiPM (HV=33V)







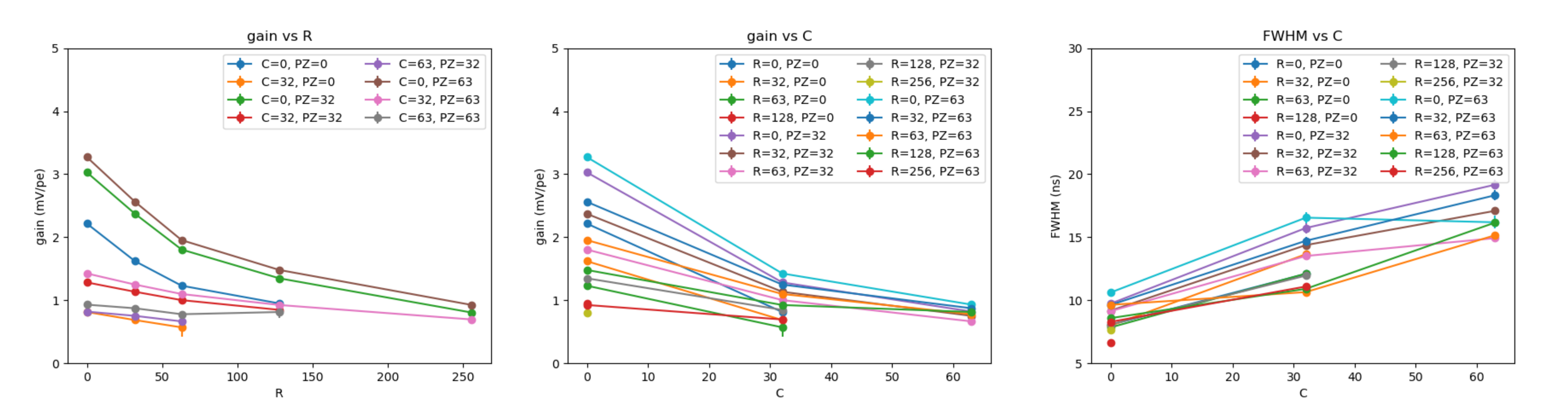
Charge distribution (cfg 16,5,40):
- Gain = 2.41 mV/pe
- SNR_amp = 4.93
- SNR_chg = 5.19

Output pulse (cfg 16,5,40):
- FWHM = 11.69 ns
- Tau_dec = 5.81 ns

Output dynamic range
- 900 mV without ext. PZ
- 600 mV with ext. PZ

Global configuration – Summary

$V_{Bias} = 33$ V

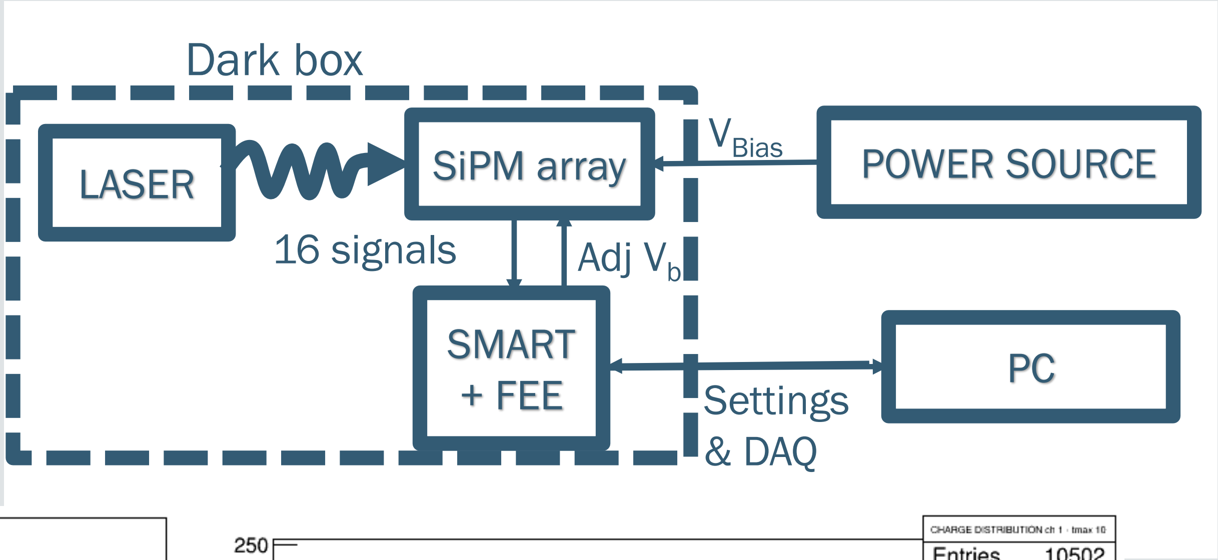


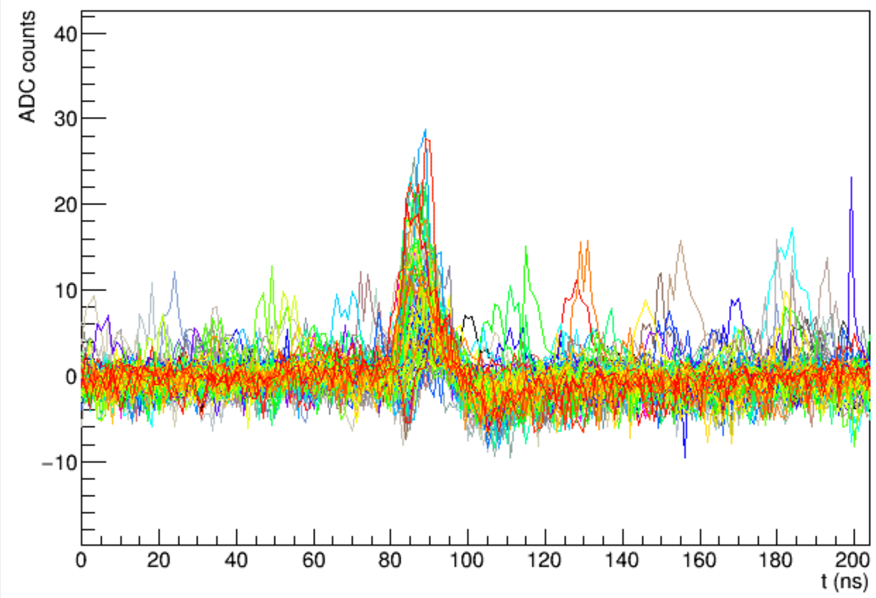
Gain depends mainly on R & C
FWHM depends on C & PZ

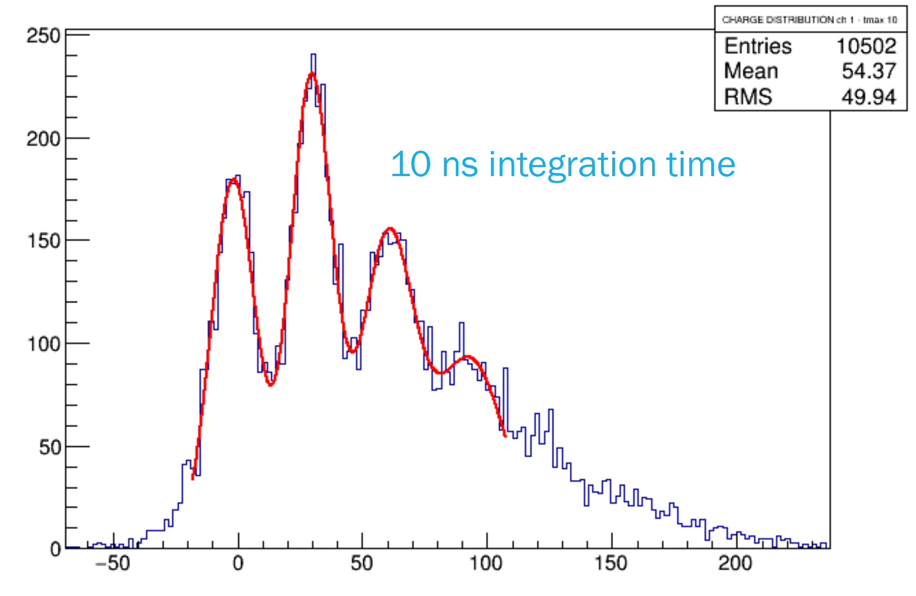
Gain: [0.57 , 3.27] mV/pe
FWHM: [7.68, 19.16] ns
Tau : [3.0, 19.58] ns

Complete FEE measurements

- Laser far away from SiPM arrays, diffusing lens placed in between to achieve uniform illumination
- SiPM arrays + SMART + FEE module
- 10s acquisition time (about 10k wfs)

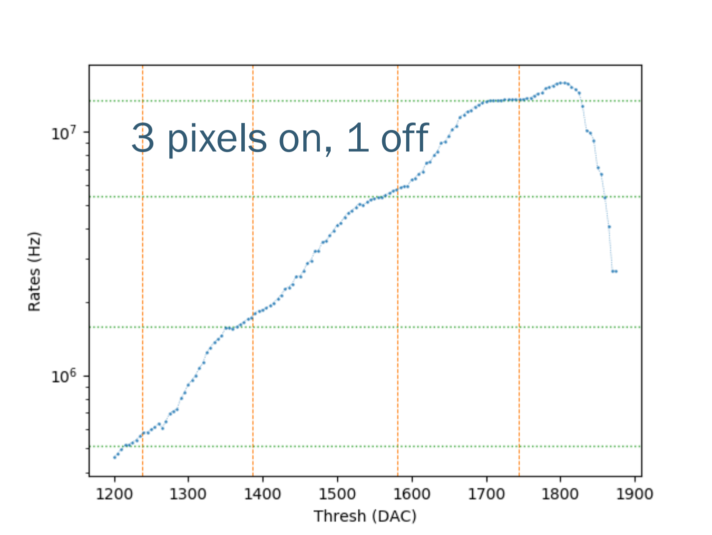


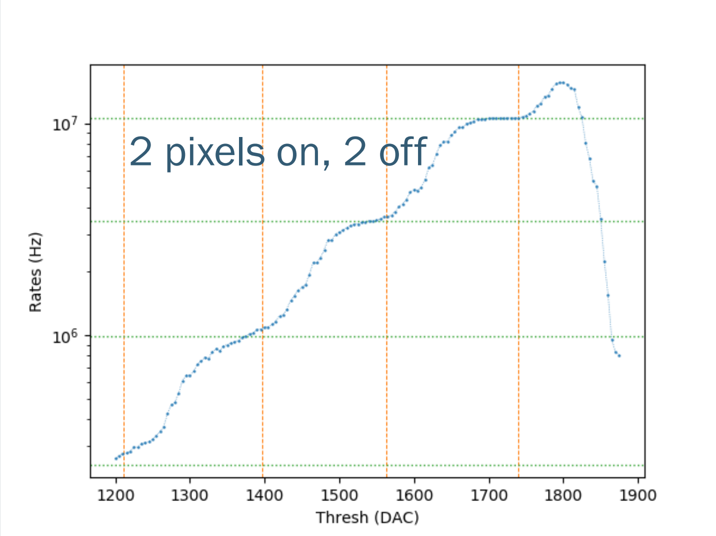


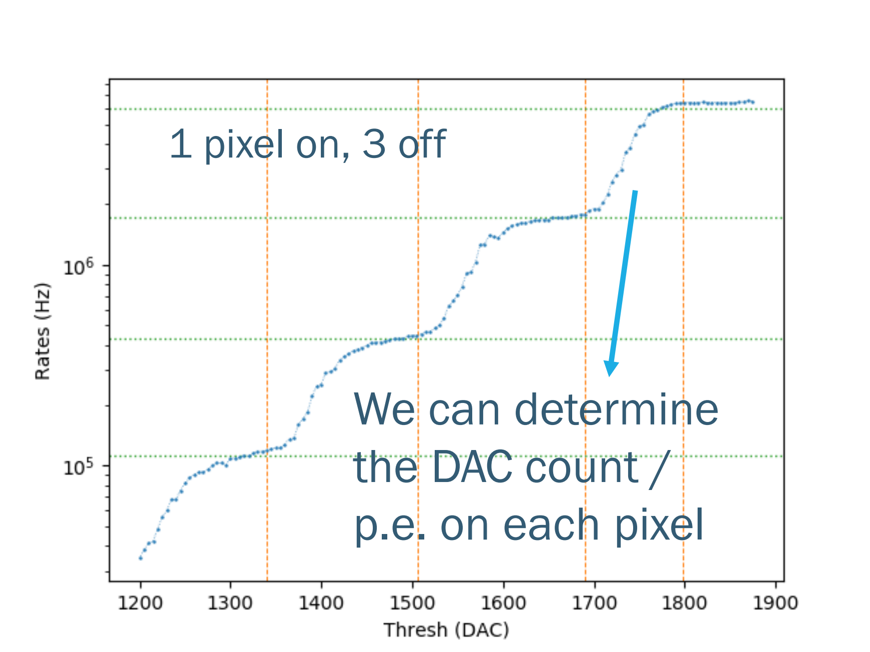


Rate scan

- Auto-trigger of FEE on groups of 4 pixels
- We performed a scan in threshold value trigger on one group
  - *We performed the scan disabling 1, 2 and 3 pixels (i.e., triggering on 3, 2, and 1 pixels) using SMART registers*
- We looked for single p.e. plateaux in the rates

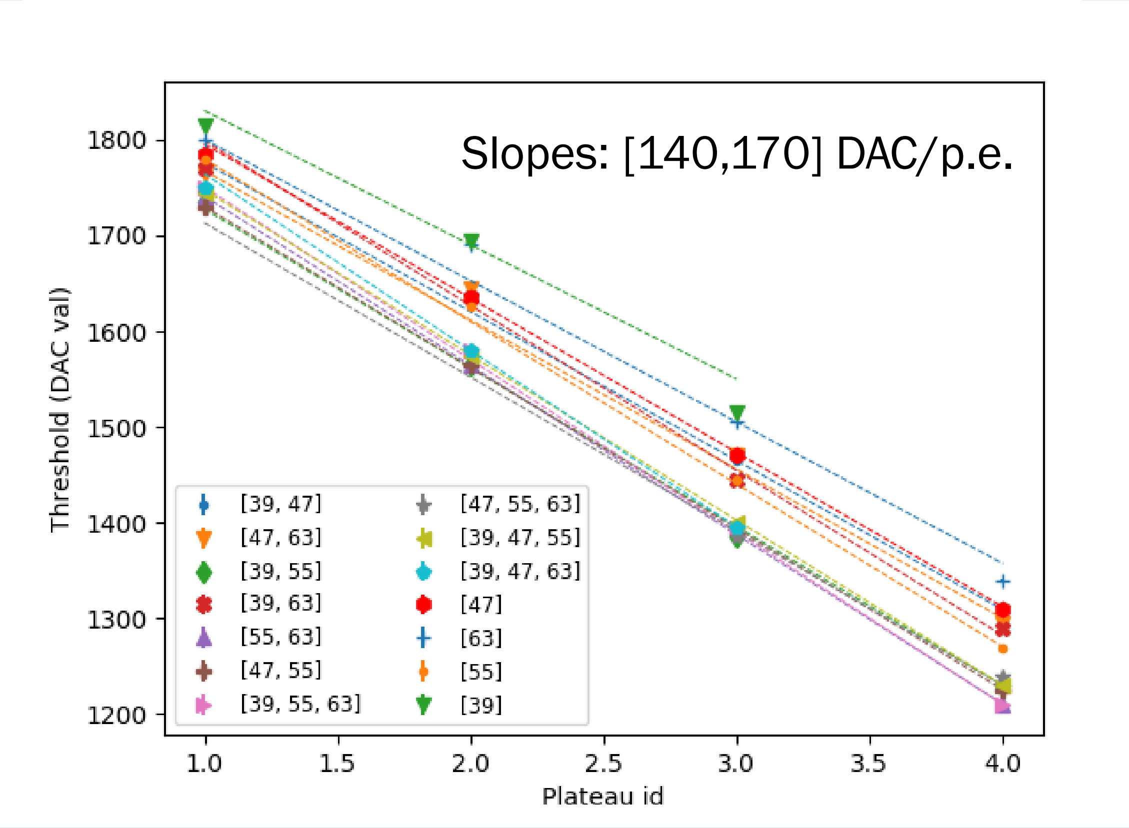


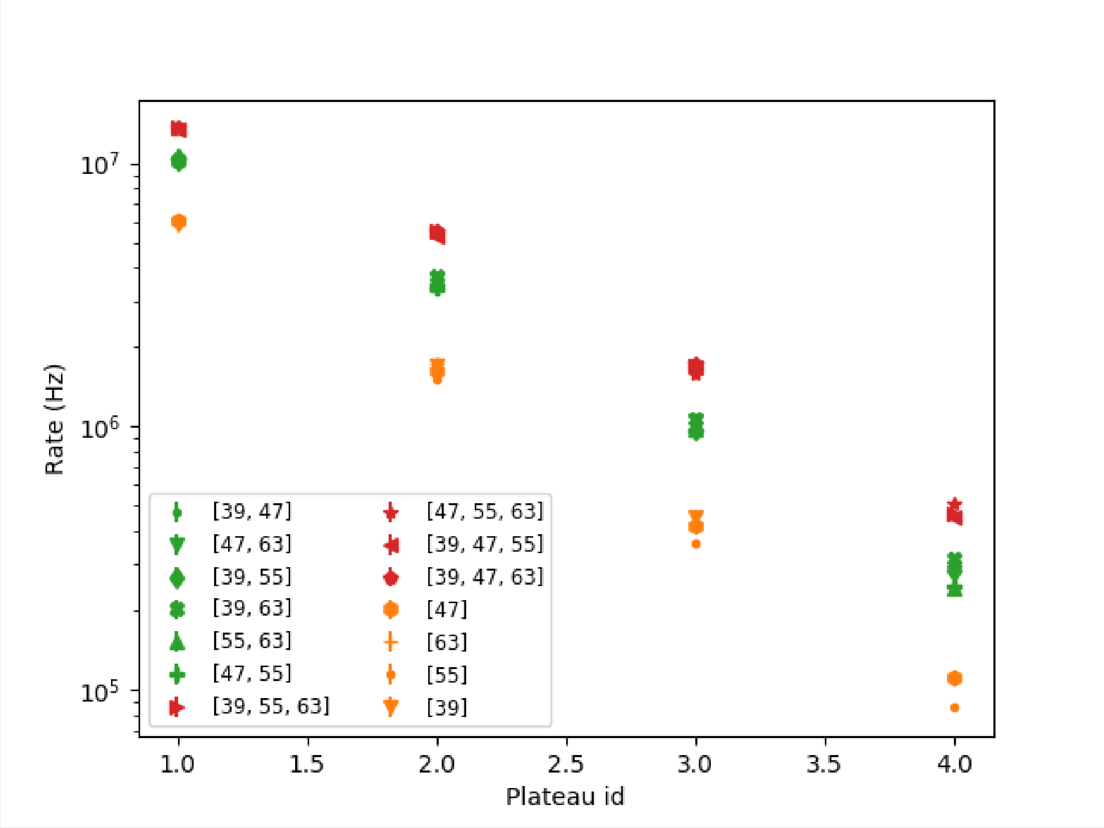




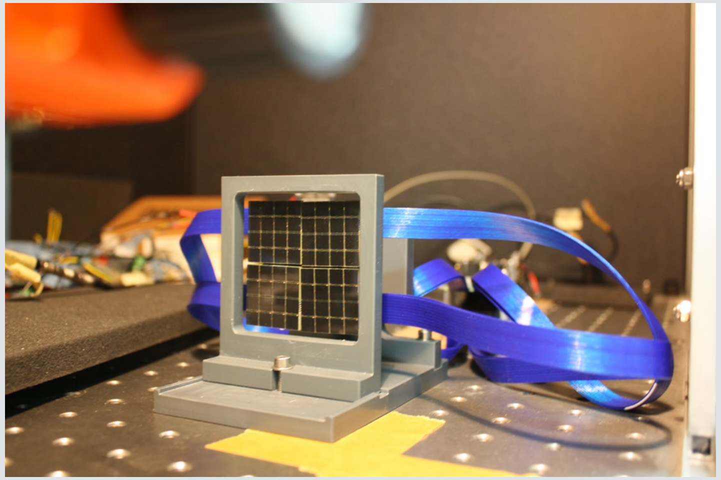
Rate scan results

Rate scan tests are very useful to find single p.e. thresholds for individual pixels





SMART quality control

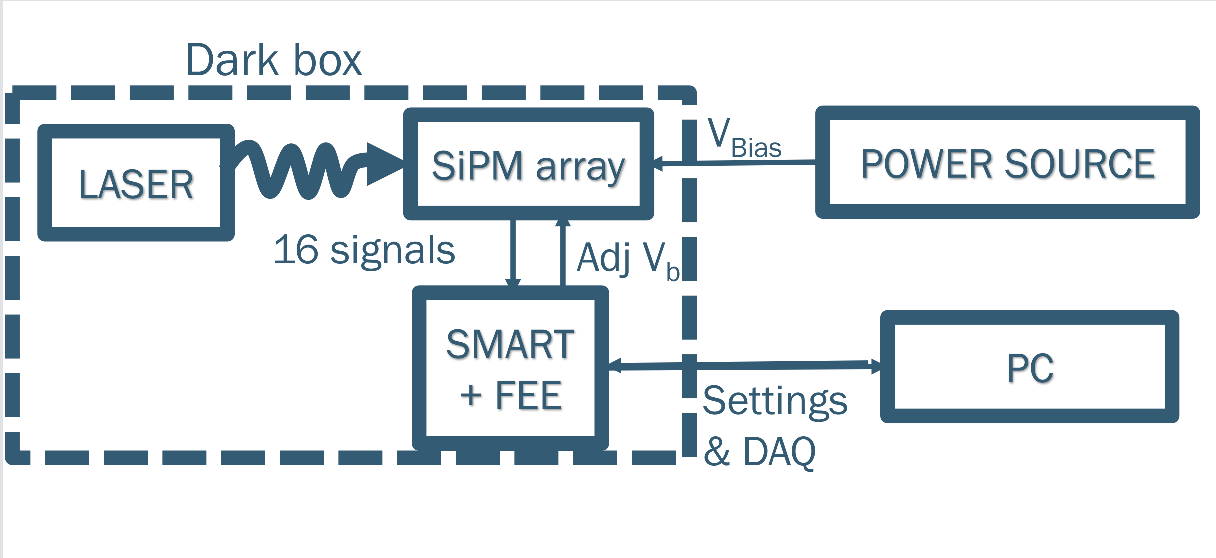


About 750 ASICs produced

We want to test the main features of the SMART to check basic functionalities:

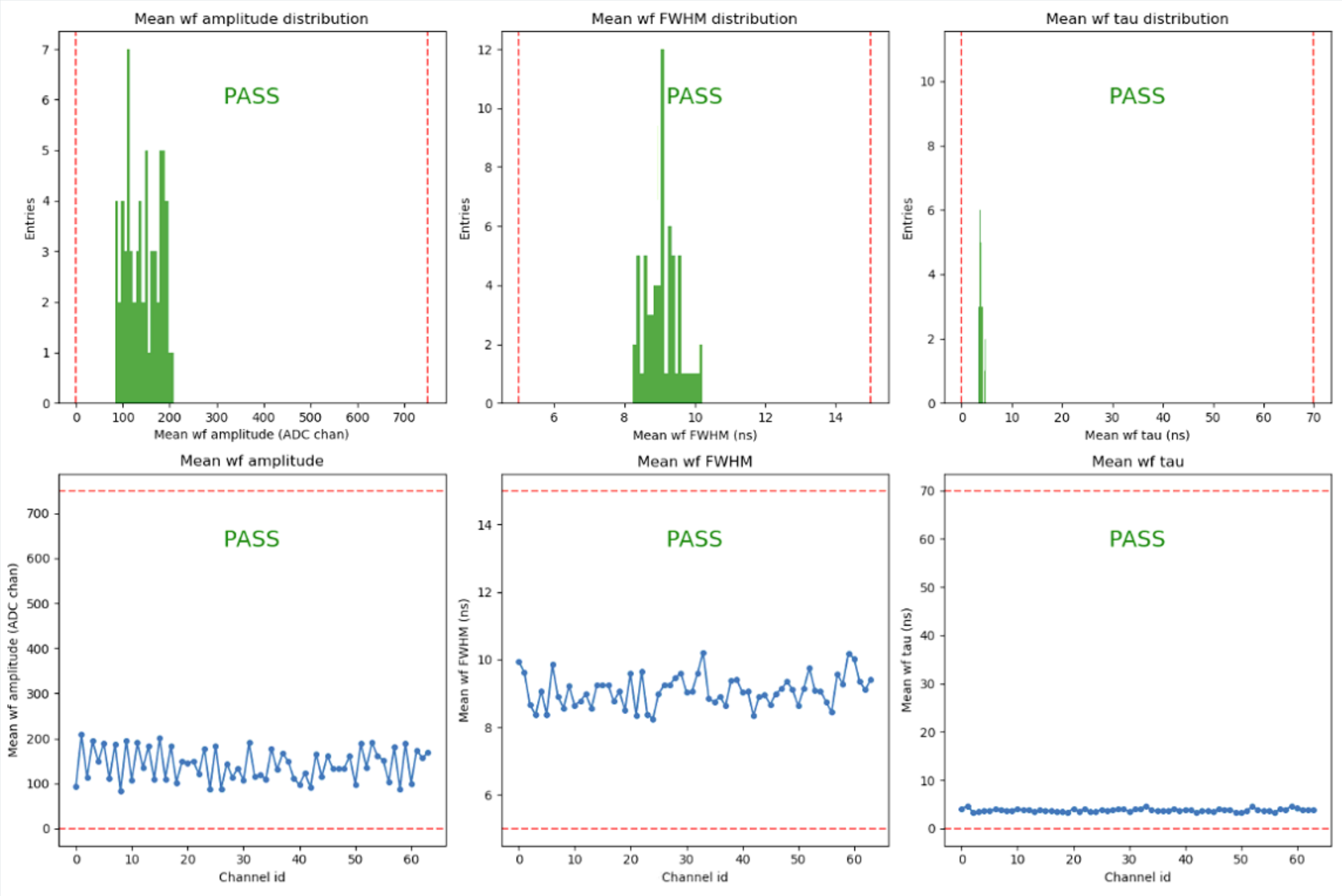
- ADC calibration for current readout
- Response to a laser pulse
- Variation of pulse shape vs SMART configuration
- Pulse amplitude variation vs DAC for fine SiPM bias tuning

See poster by G. Tripodo!



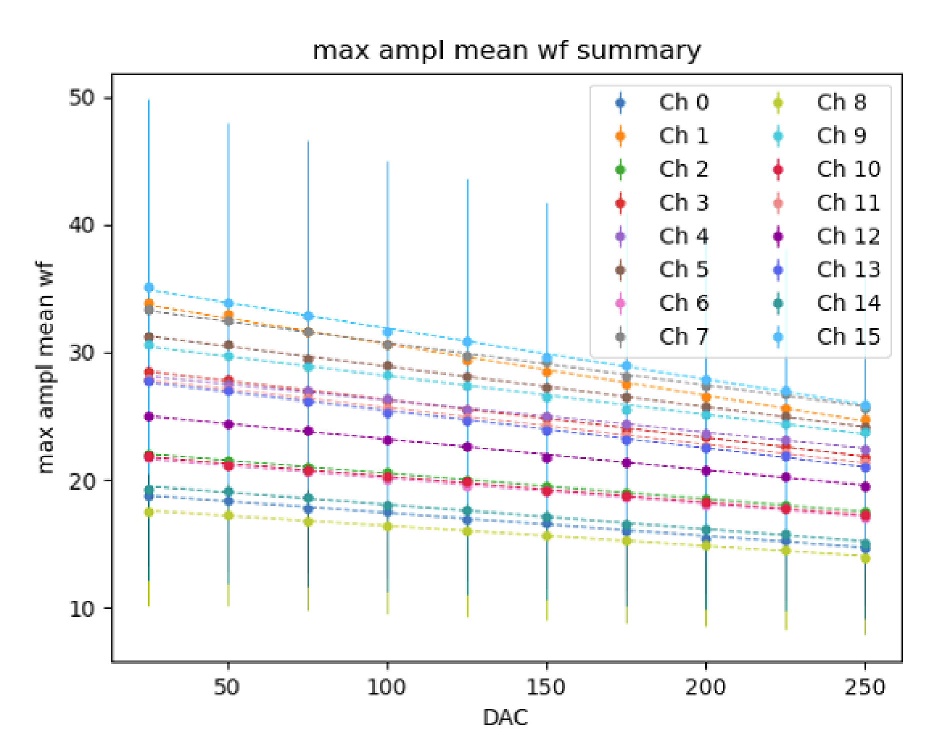
SMART configurations loop

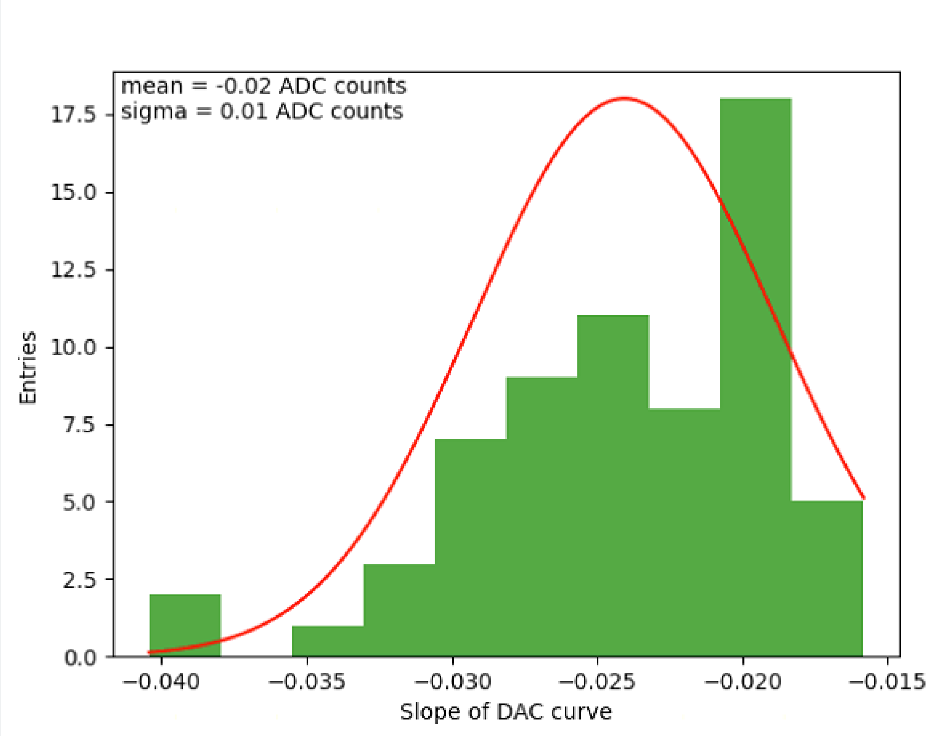
Amplitude, FWHM and tail recovery time of each channel: distribution (top) and scatter plot (bottom)



DAC loop

Amplitude of the mean waveform vs DAC value + linear fit and slope distribution





Flat fielding measurements

- Every SiPM in the array has its own breakdown voltage and a slightly different gain vs overvoltage dependance
- When biased at the same V_{BIAS} the overvoltages and the gains are different
- With the SMART ASIC we can change the DAC (0-255) and regulate the OV on each channel keeping the common bias voltage

DAC – OV relation:

$$OV = V_{BIAS} - V_{BD} - 0.7V - 4.7mV*DAC$$

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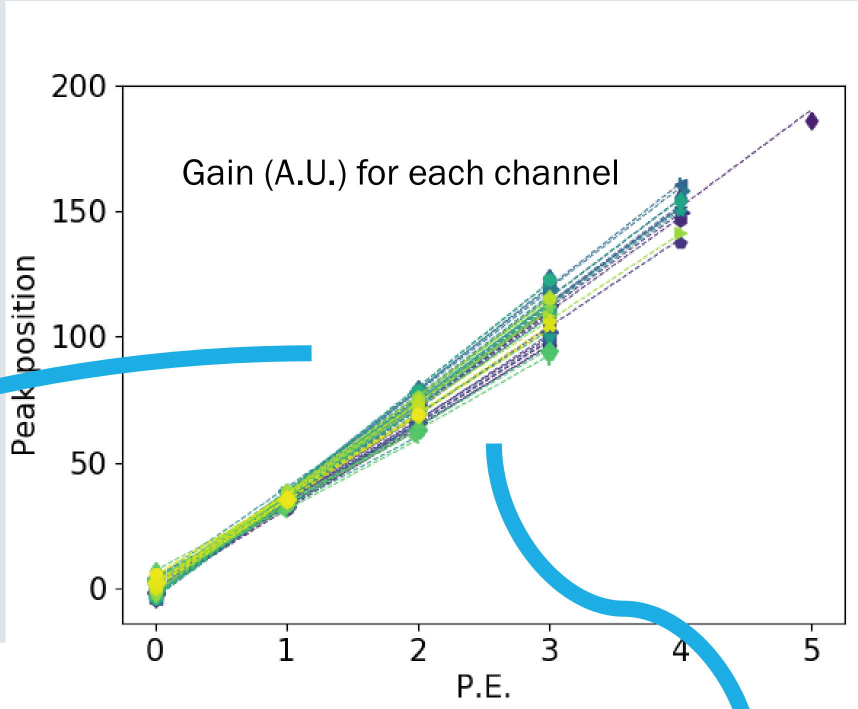
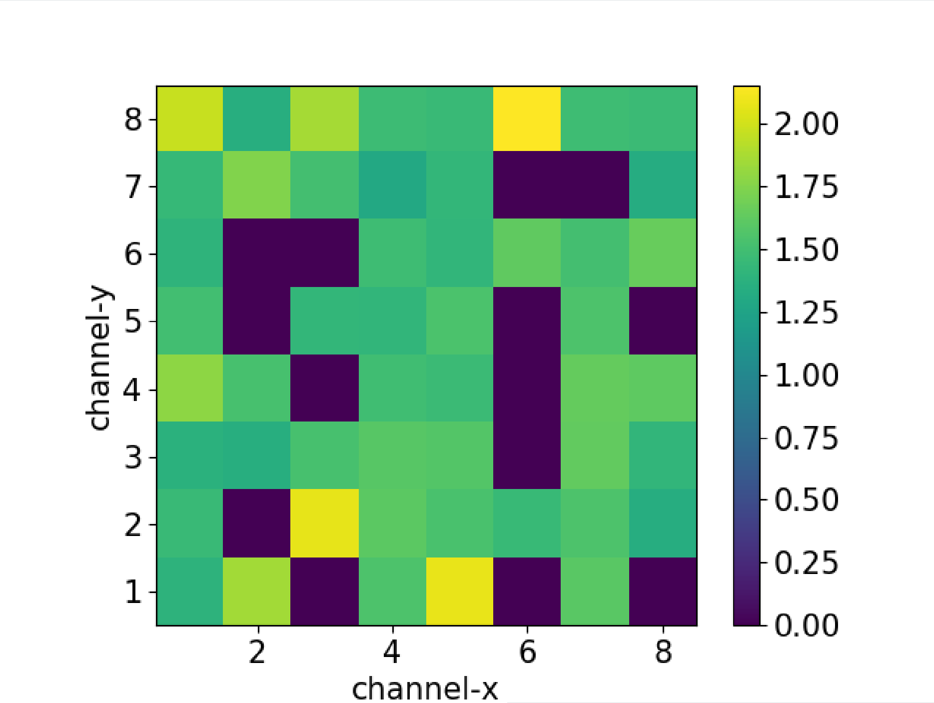
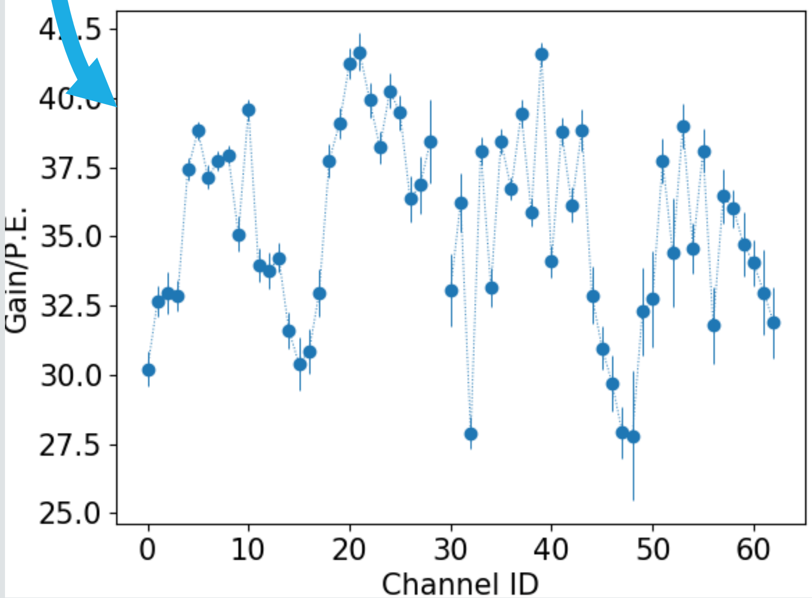
We analyzed all the 64 channels
DAC = 100

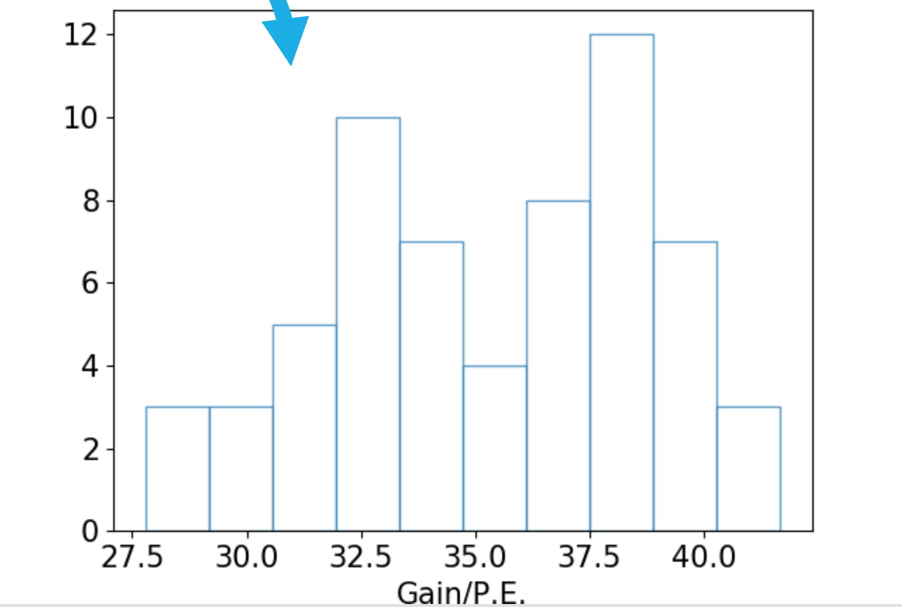


Slope of the best fit line



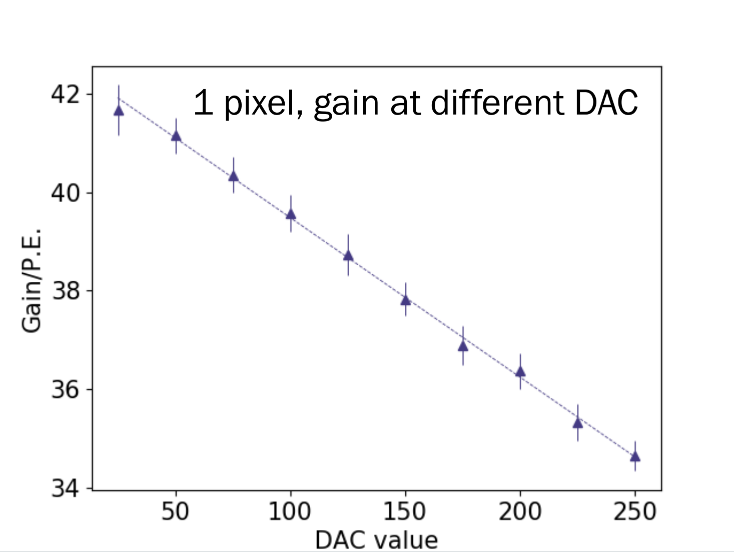
Mean p.e. set to zero for noisy pixels

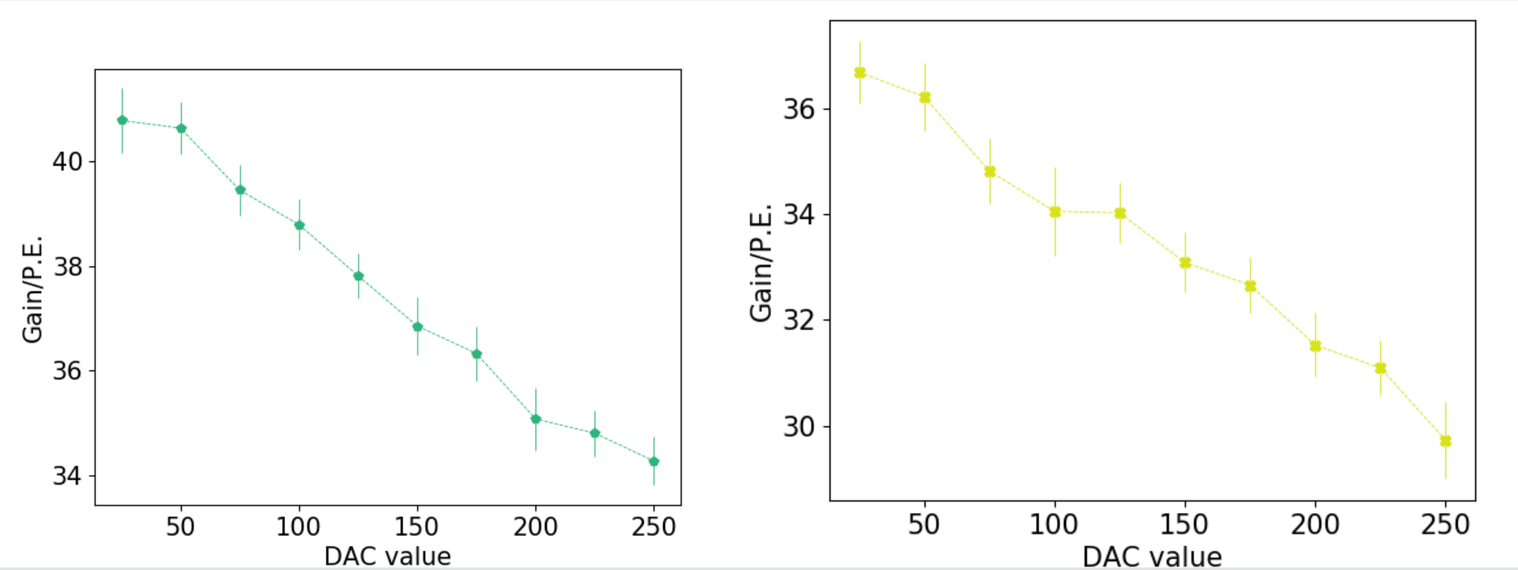


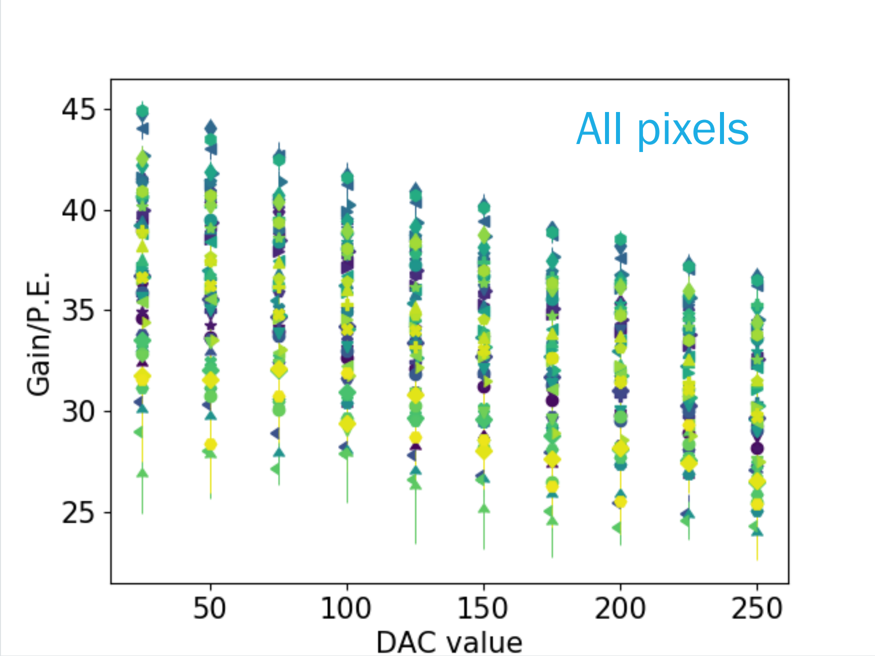


Gain/P.E. for all pixels:
- Scatter plot
- Distribution

Gain vs DAC







We repeated the procedure for all the DACs tested
Each gain vs DAC curve was fitted with a linear function

Conclusions & Outlook

- Performances of the SMART ASIC tested and characterized with FBK NUV HD SiPMs
  - Gain and signal shape dependance on R, C and PZ
- SMART for the full pSCT camera (~750 ASICs) produced and tested in 2021
  - Only 7 ASICs were found to be defective (< 1%)
- Studies on gain versus DAC dependance ongoing
- New design ready to be tested for future upgrades

THANK YOU!

For further information please contact
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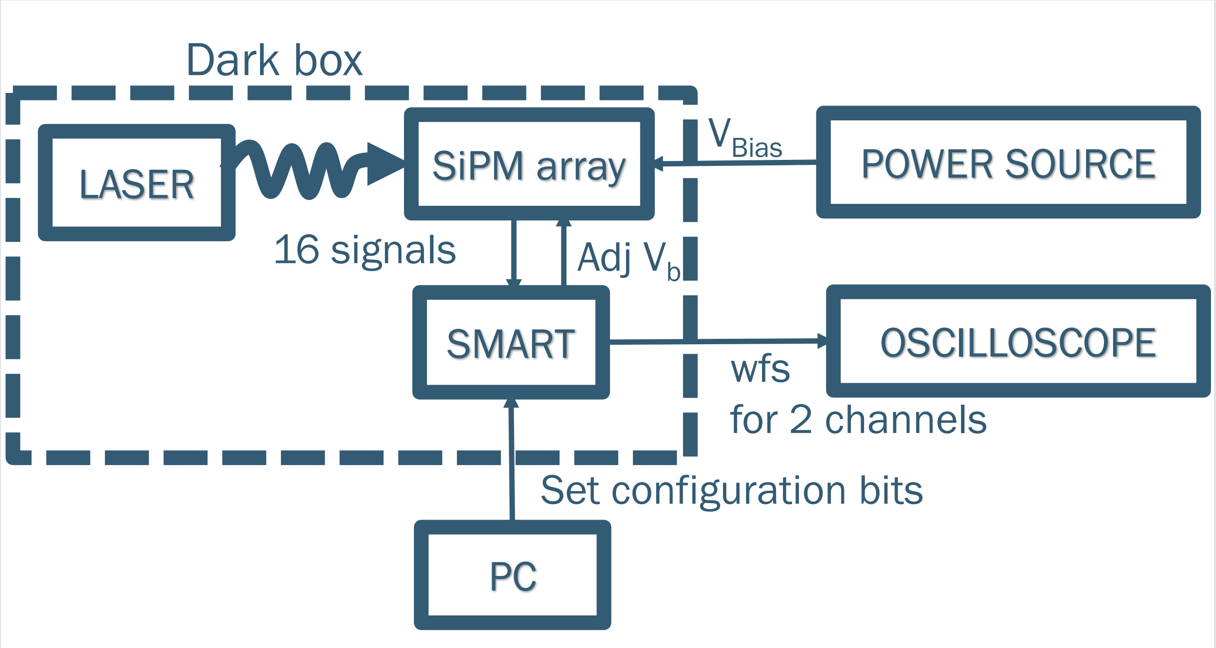
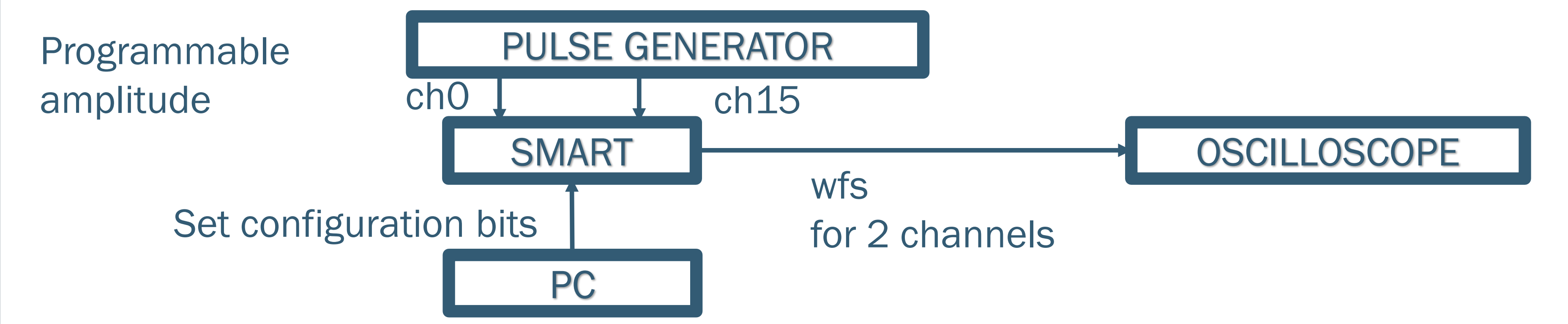
This work was conducted in the context of the CTA Consortium. We gratefully acknowledge financial support from the agencies and organizations listed here:
http://www.cta-observatory.org/consortium_acknowledgments

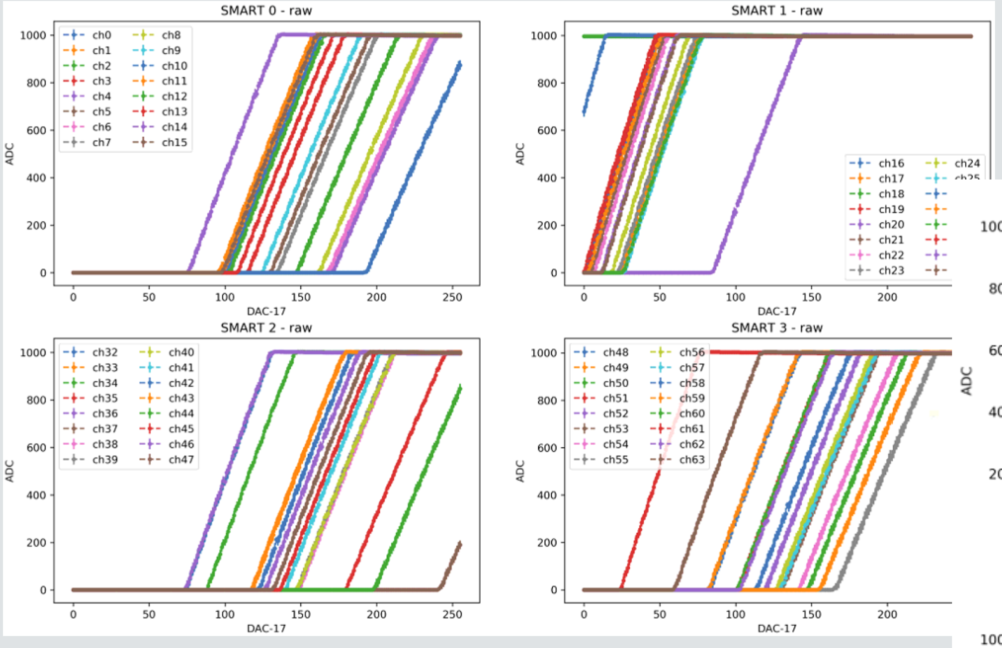
Dynamic range



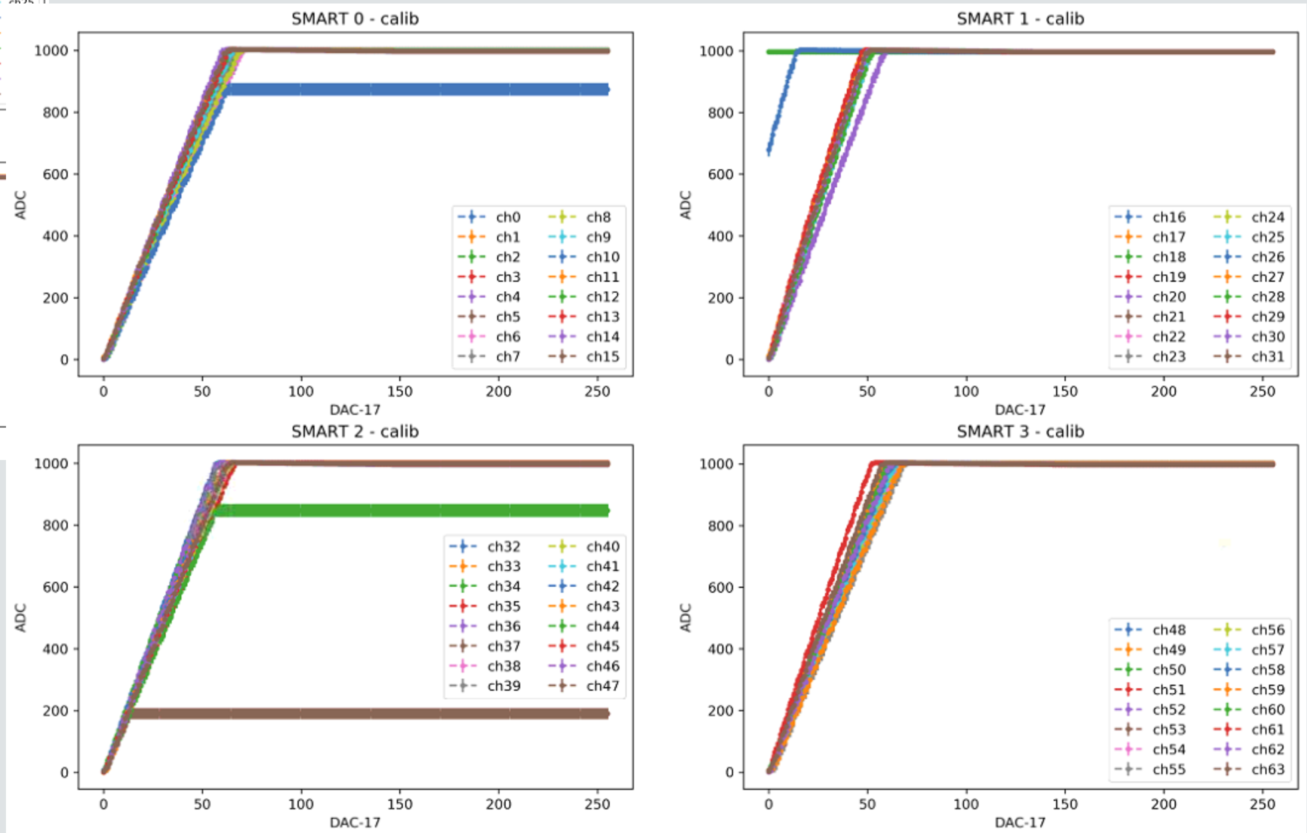
- Two independent measurements:
  1. *We illuminated one SiPM with high intensity pulsed light and measured the max ampl*
  2. *We injected in one channel a charge signal with an external pulse generator*
- We obtained the maximum waveform amplitude for different configuration bits
- We compared two channels w/ and w/o the external PZ



SMART ADC Calibration

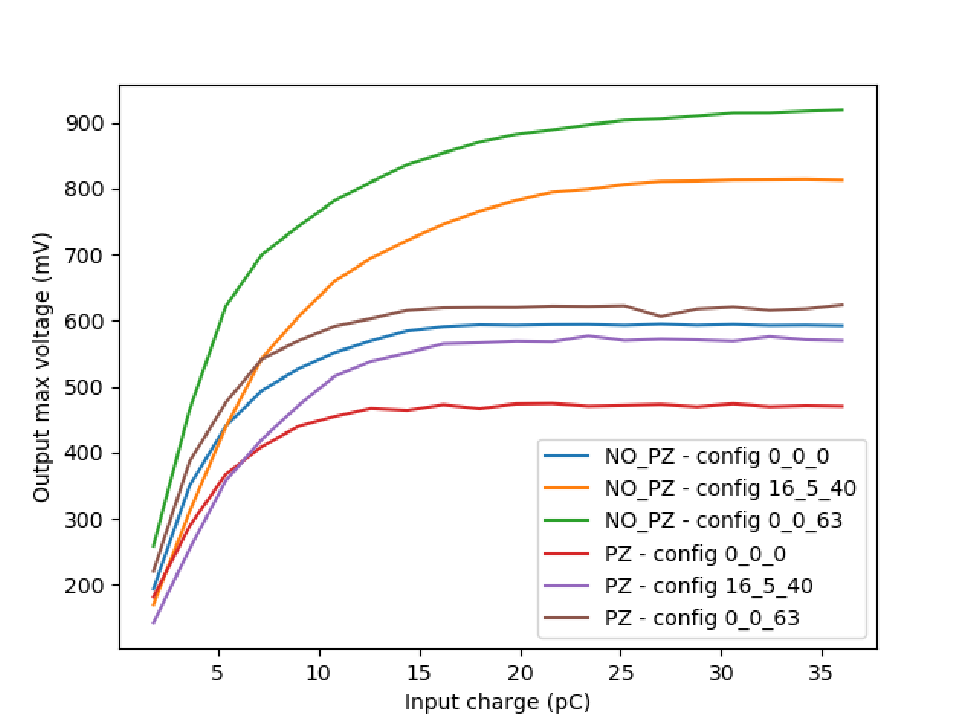


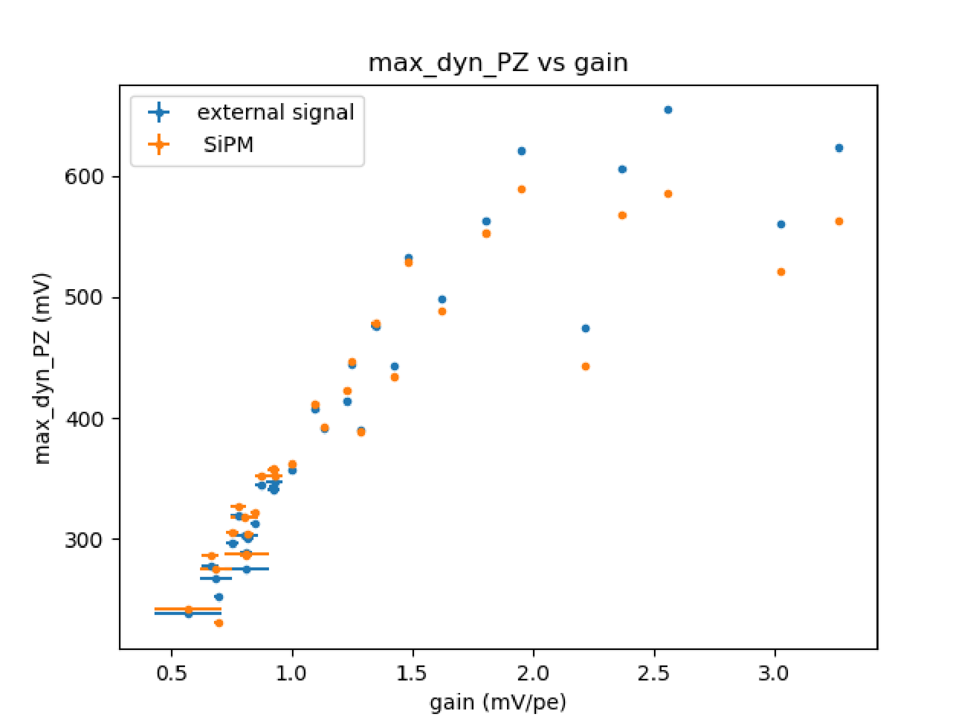
We measure the ADC value on each channel as a function of the reference channel DAC value (DAC-17).



The calibration value is stored and used to measure the Idc on each channel.

Dynamic range



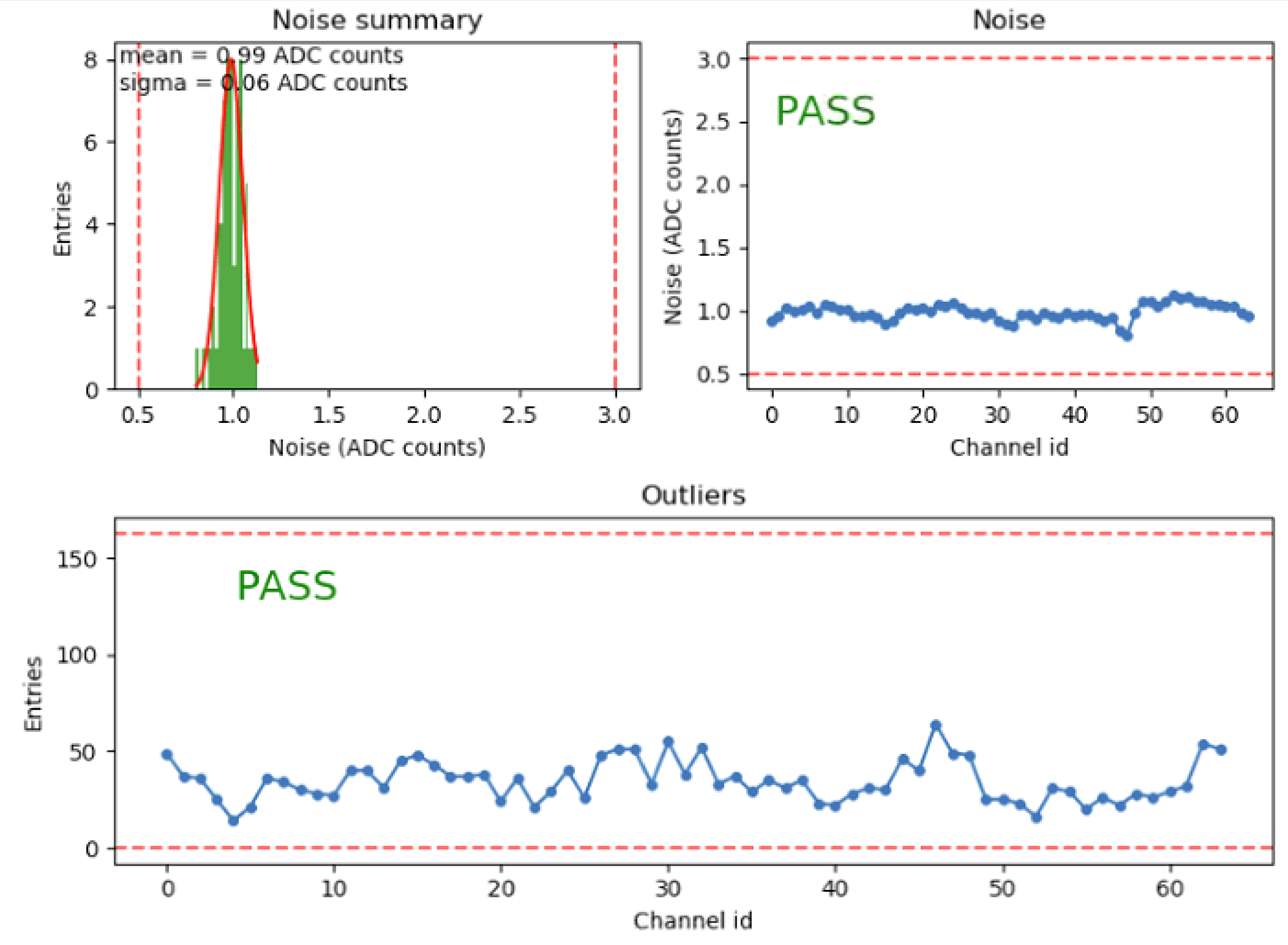


Without external PZ the maximum dynamic range is around 900mV (green).
For an intermediate configuration (R=16,C=5,PZ=40) we reach 800 mV.
The external PZ decreases the maximum dynamics down to 600 mV.
For the intermediate configuration (R=16,C=5,PZ=40) it is 550 mV.

Pedestal acquisition

Setup:

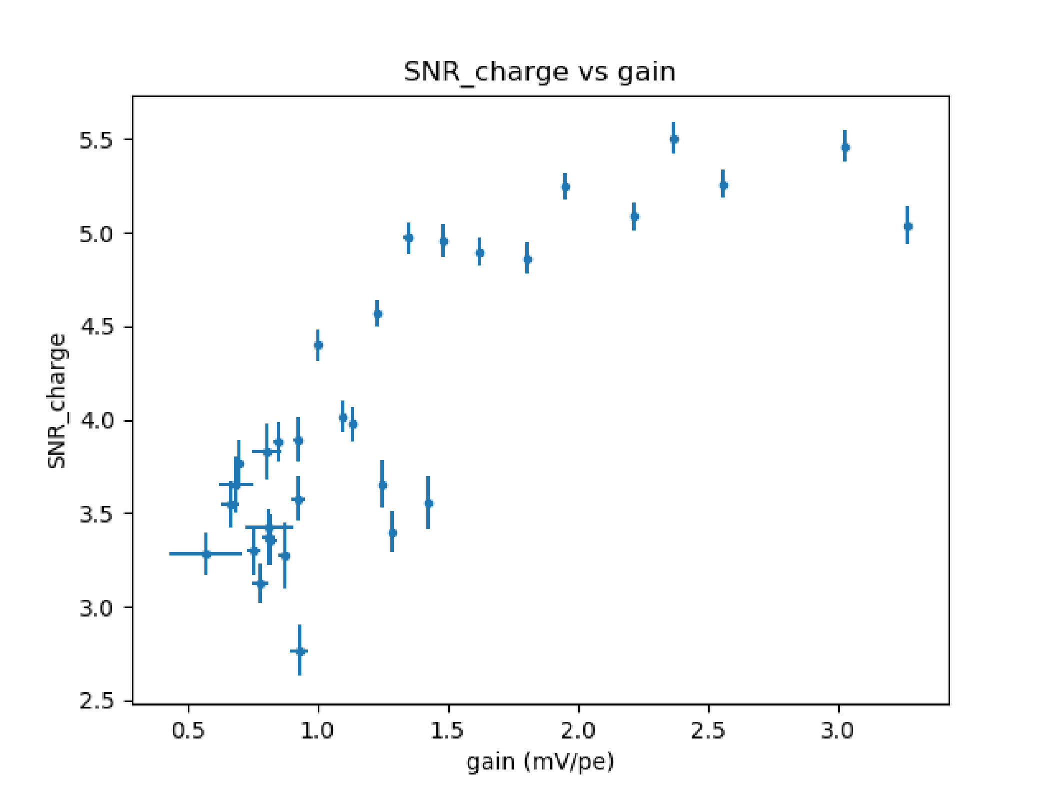
- Trigger: hardsync
- Acquisition time: 60 s
- All buffer is scanned and pedestal is saved → used later with signal run

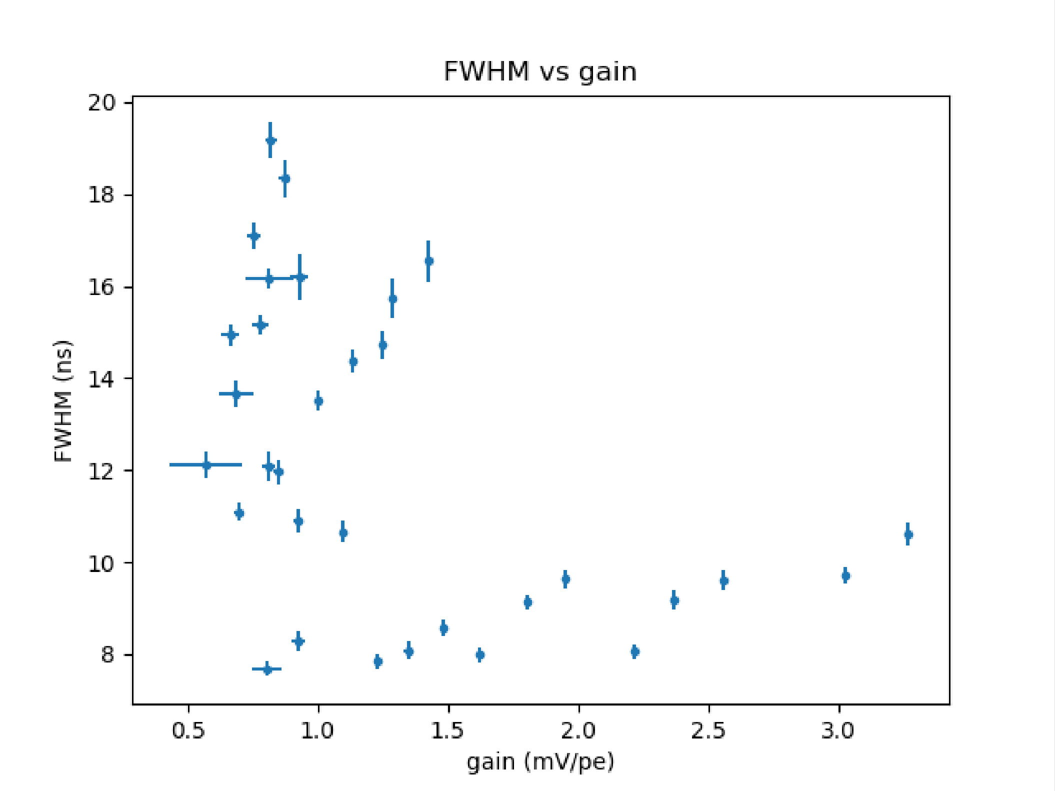


This pedestal is used to calibrate the following runs

Global configuration – Summary

$V_{Bias} = 33$ V

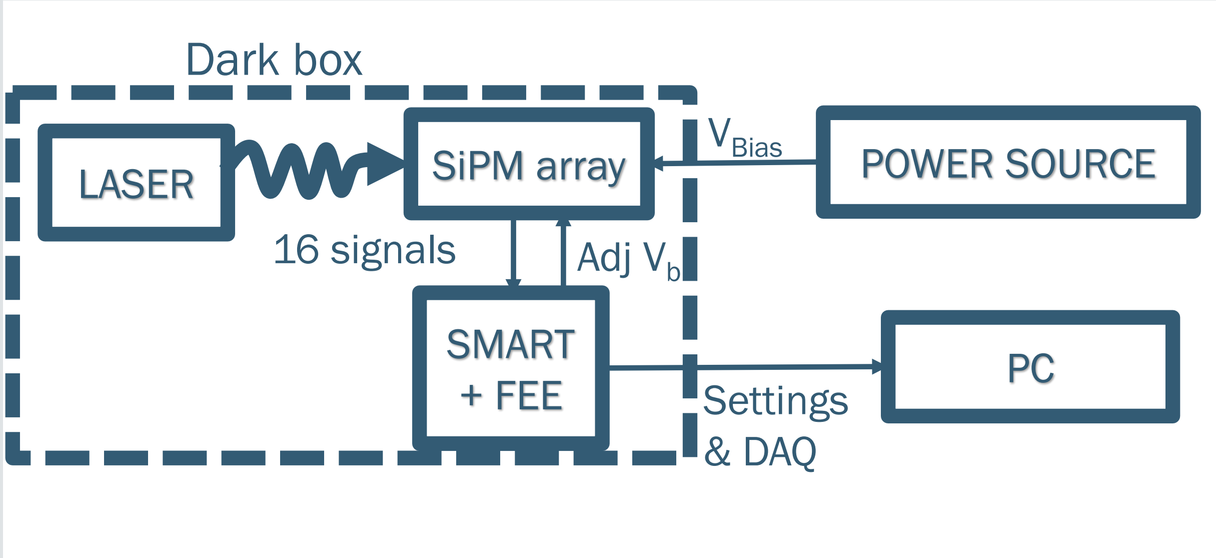




Experimental setup

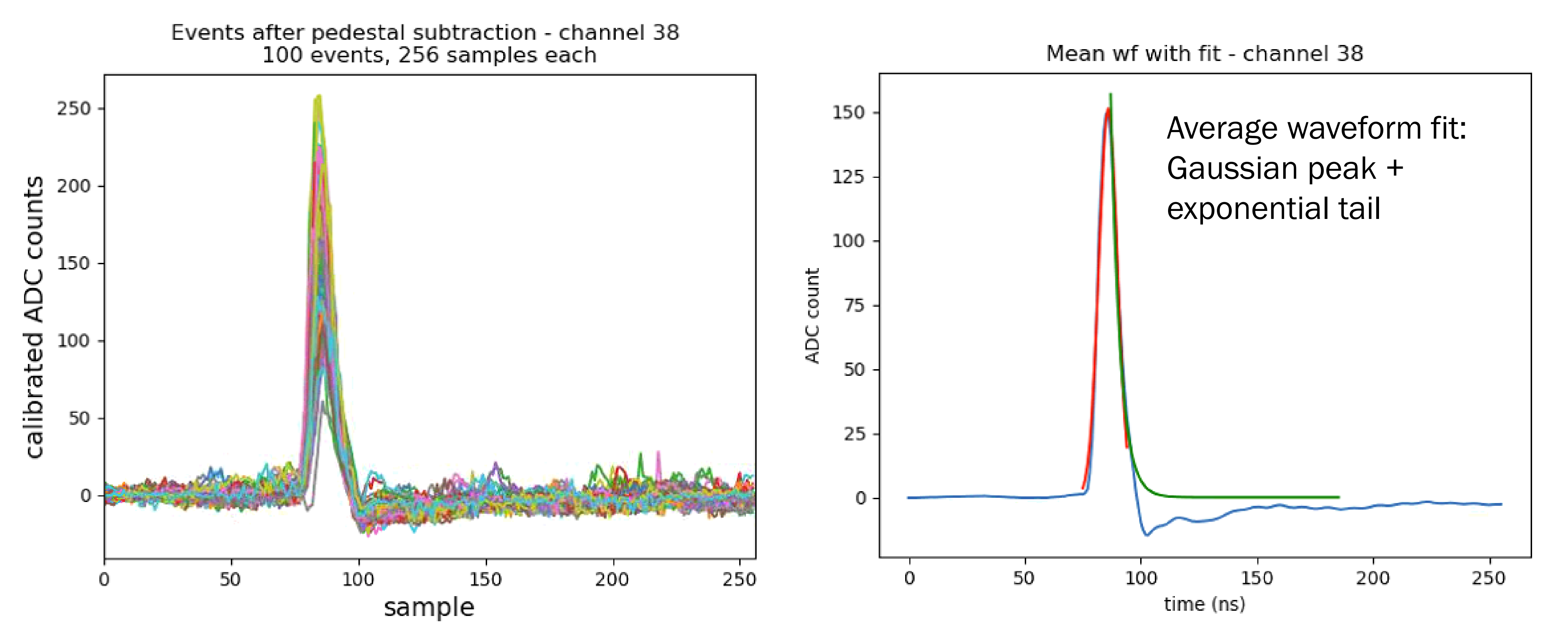
- Laser far away from SiPM arrays, diffusing lens placed in between to achieve uniform illumination
- SiPM arrays + SMART + FEE module
- 0 0 63 globals configuration to increase gain
- Low light intensity to be able to perform charge integrated spectrum
- V_{BIAS} fixed to 33.5 V
- 10s acquisition time (about 10k wfs)
- Scan on DAC value to change the OV
  - *At first, DAC is the same on all channels*

- Charge distribution
- Multigaussian fit → gain and mean p.e.



Signal run

10 s acquisition time with external trigger, laser on all pixels (almost uniform)



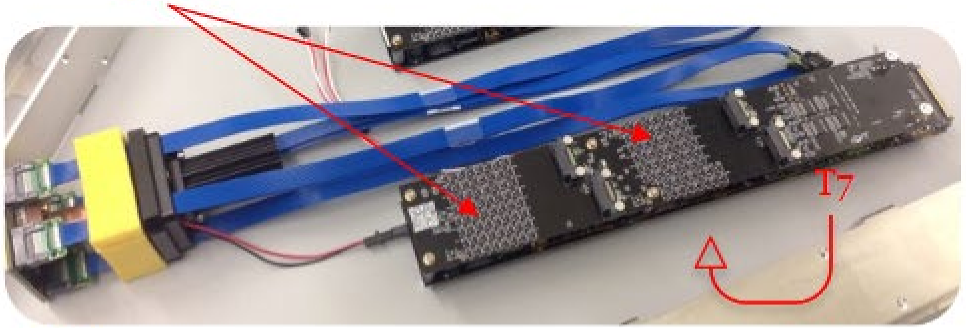
Upgrade of the camera

- Populate all 9 camera sectors → 177 modules – 11328 pixels
- SiPMs produced by FBK with high PDE and low optical CT
- New electronics to reduce noise
  - Separation of the digitizing and trigger ASICs (TARGET-C + T5TEA)
  - Integrated pre-amplifier attached to SiPM boards (SMART)
- New DACQ boards
- New module cage
- New camera frame and redesign of the cooling system

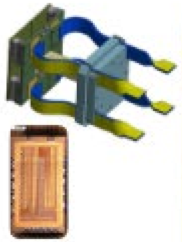
Full-chain testing : current vs. upgrade

M. Capasso's talk @ CTA Consortium Meeting May 2021

Preamps and current sensors

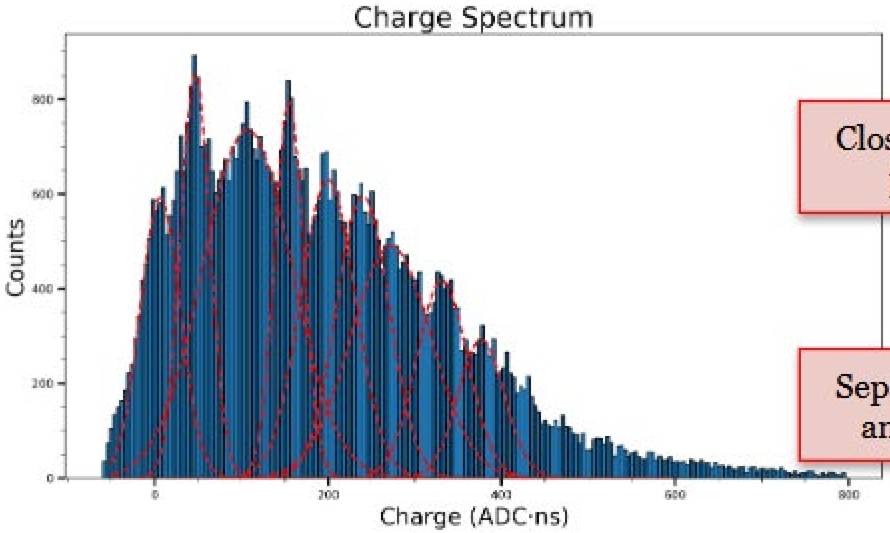


FPM



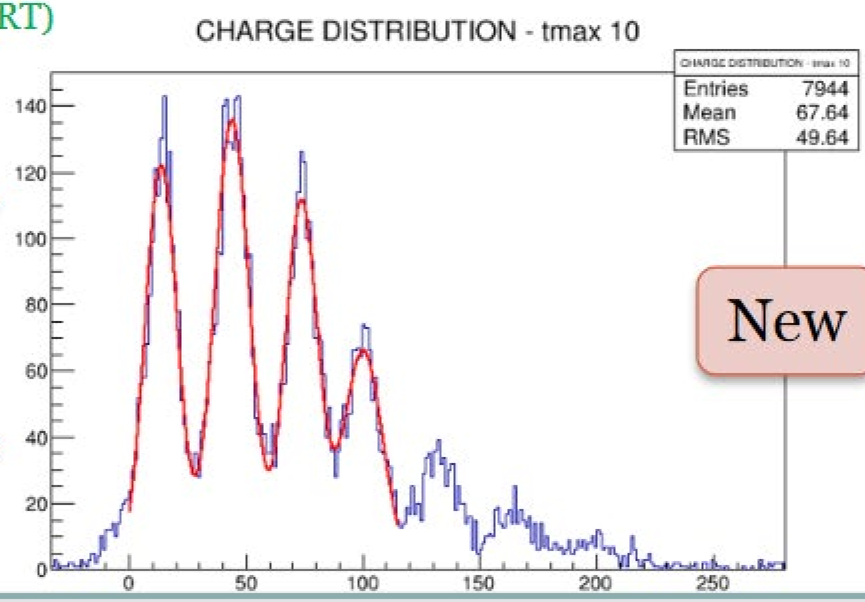
FPM+preamps and current sensors (SMART)

(C)T5TEA + (C)TC



Closer FPM and preamps

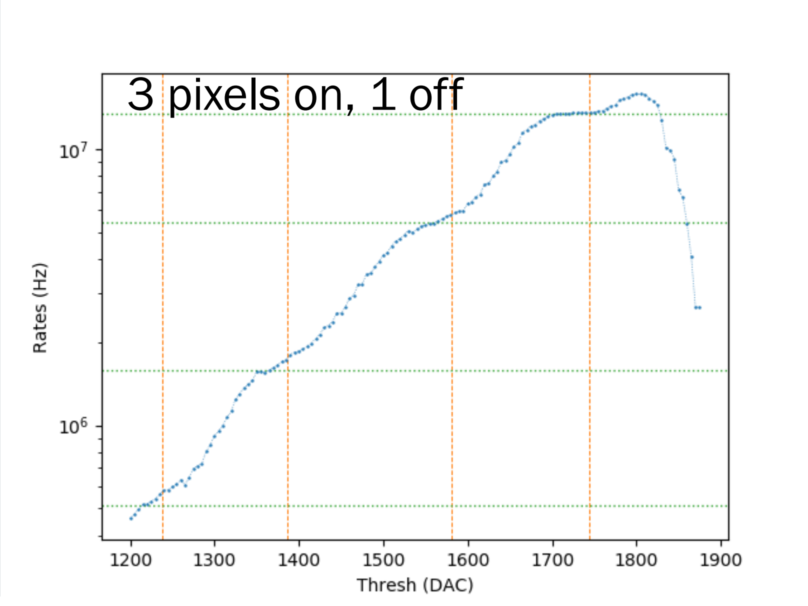
Separate trigger and digitizer

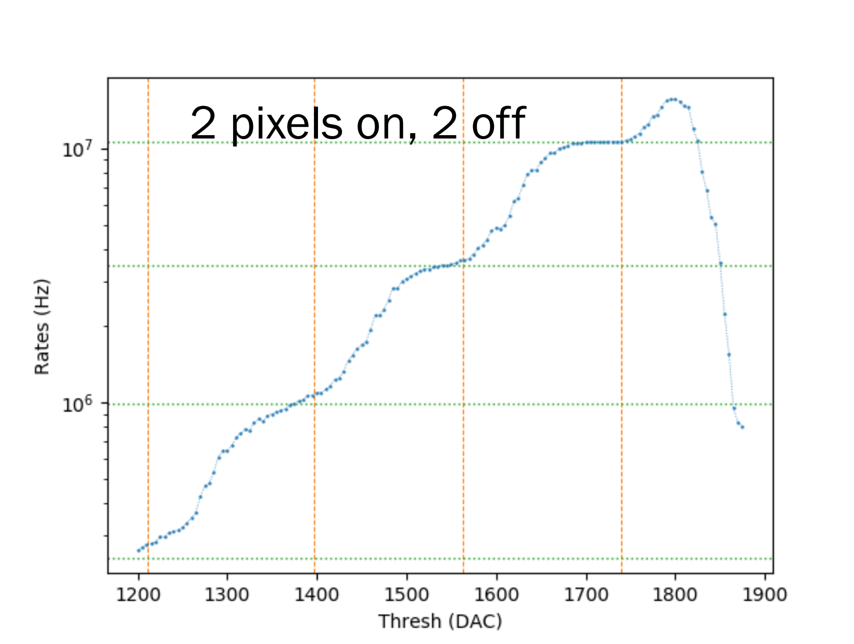


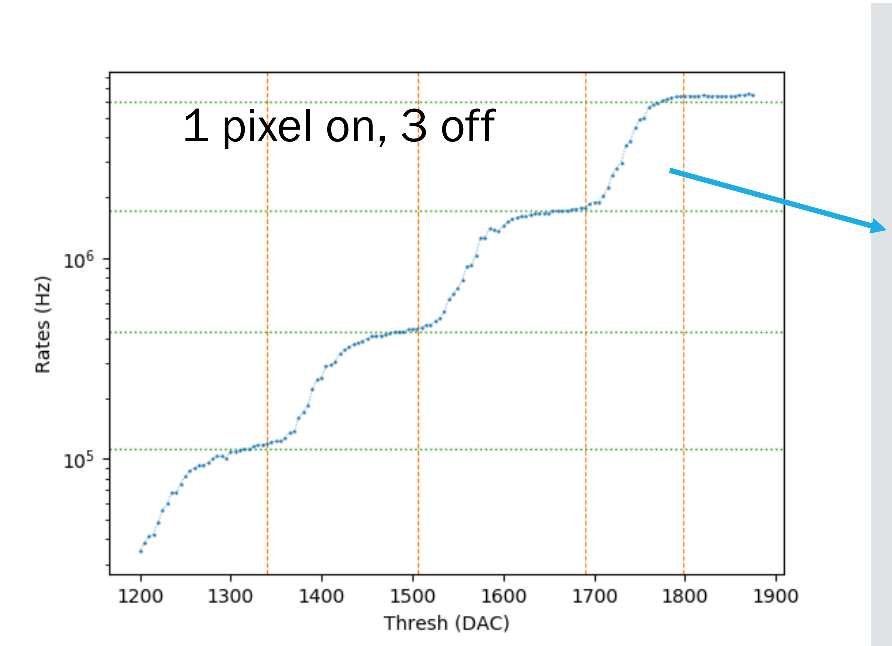
New

Trigger scan

- We performed a scan in threshold value trigger on one trigger group
  - *We performed the scan disabling 1, 2 and 3 pixels (i.e., triggering on 3, 2, and 1 pixels)* ***using the SMART control registers***



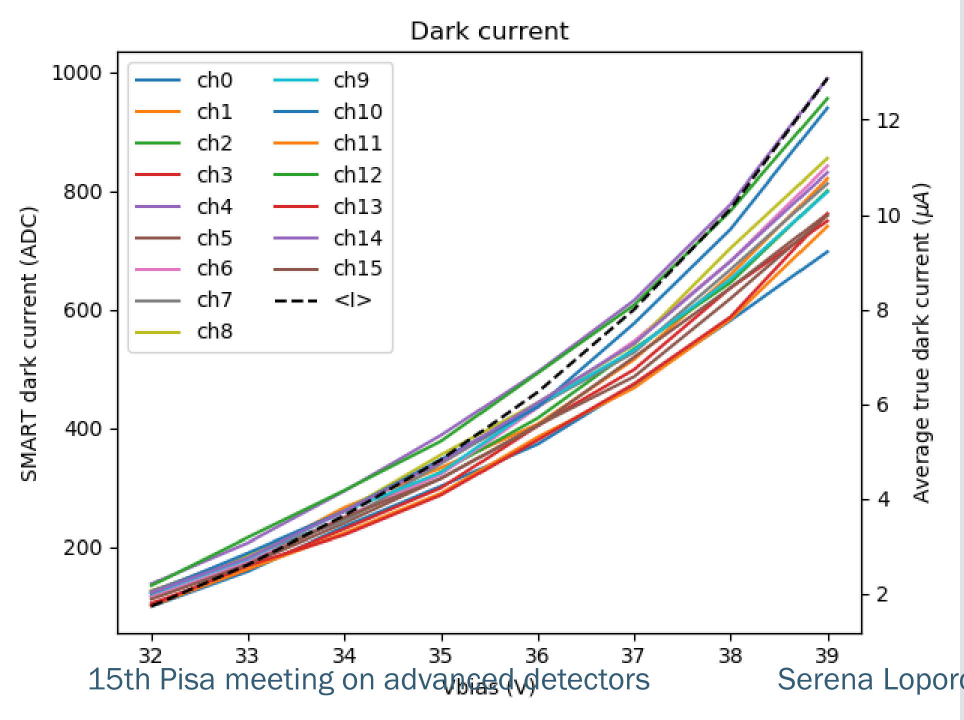


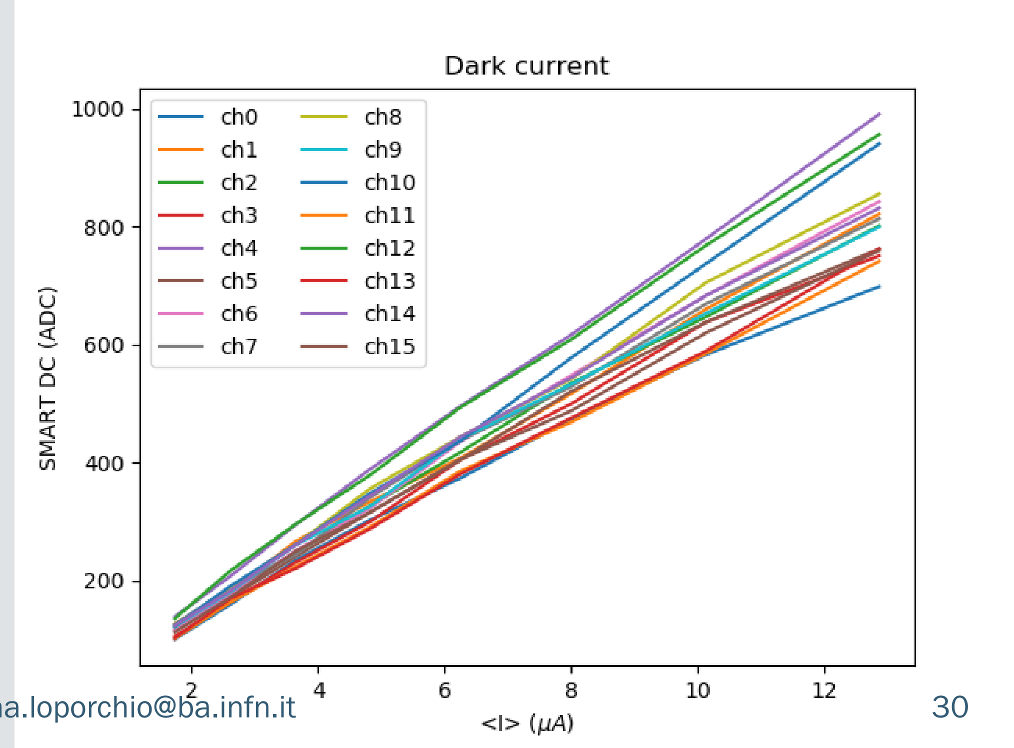


We can determine the DAC count / p.e. on each pixel

Slow control

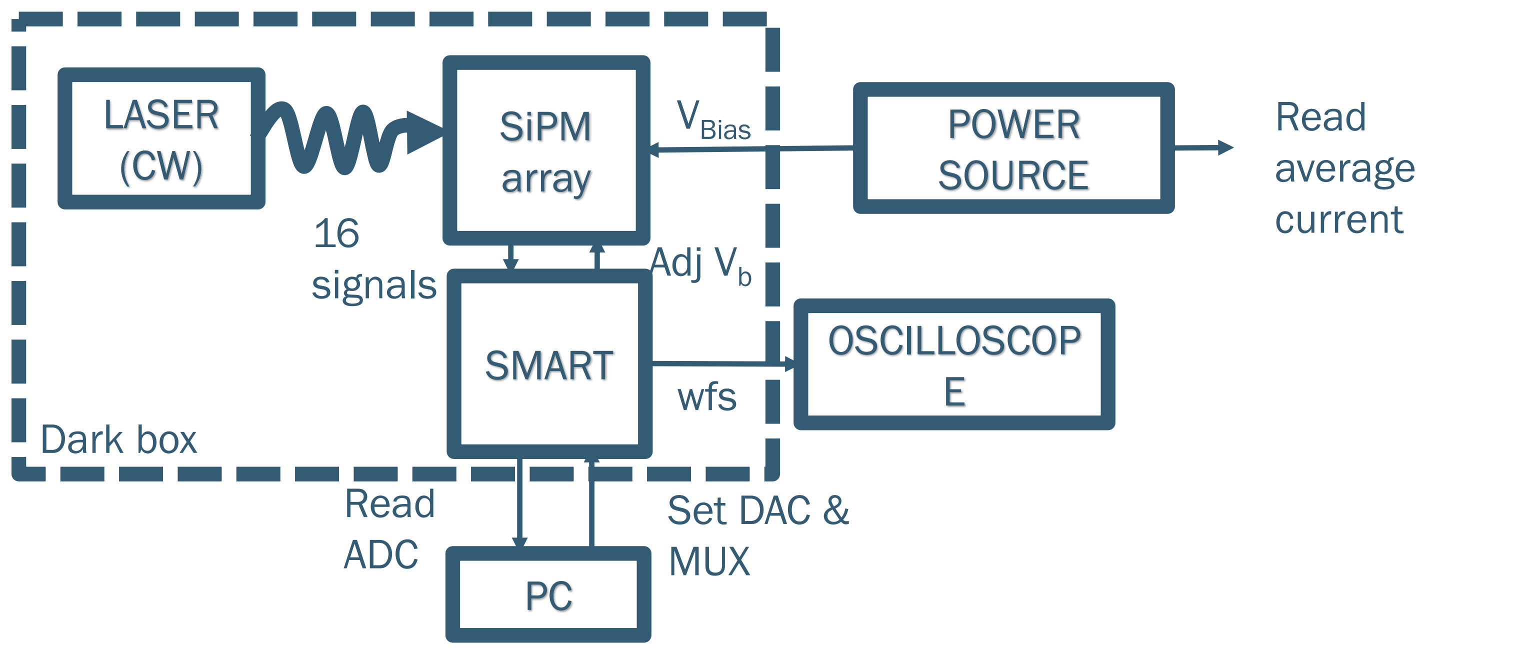
- We measure the DC current on each channel in dark conditions as a function of bias voltage
  - *For each V_{bias} and each channel we set the DAC on ch 17 found from calibration (previous slide) and measure the mean current with the ADC*
  - *We compare the ADC current with the average dark current measured with the power meter*





Slow control - setup

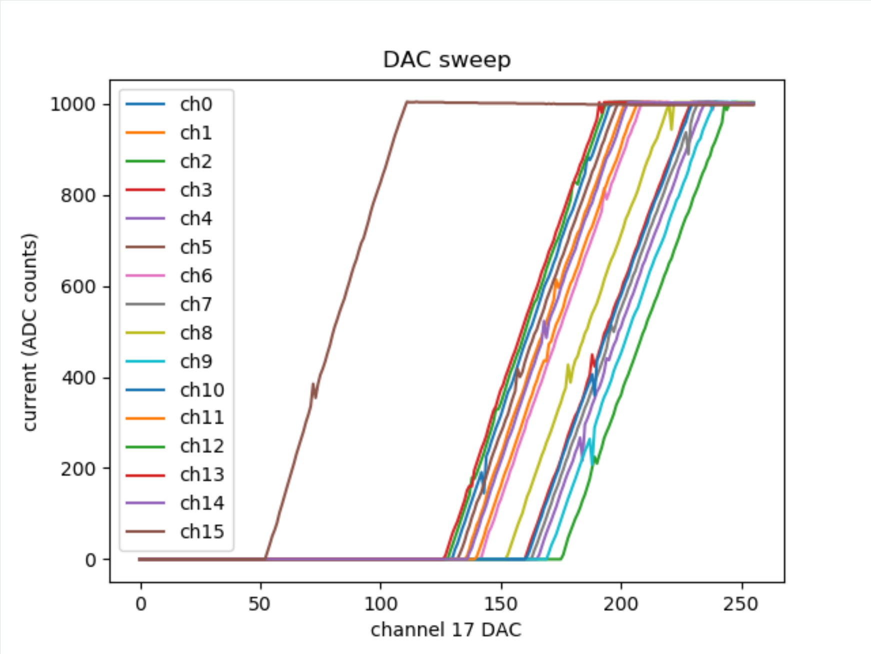
- Configuration is fixed R=16,C=5,PZ=40
- DC current is measured for each channel using a reference channel (ch 17)
- The reference channel has a configurable DAC which should be set accordingly for each channel



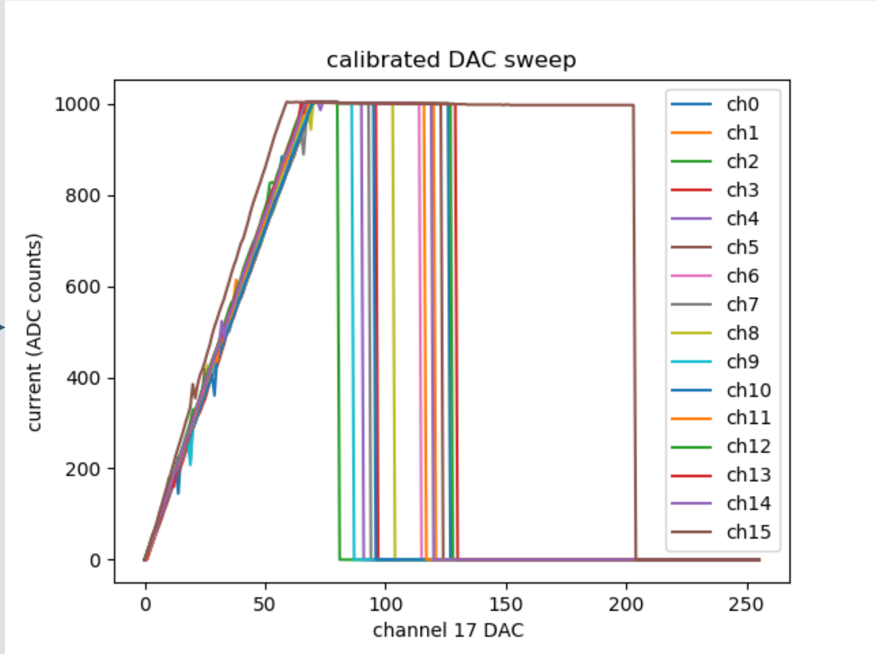
- DC current measured for different bias voltages in dark conditions and for fixed bias voltage with increasing light illumination

Slow control

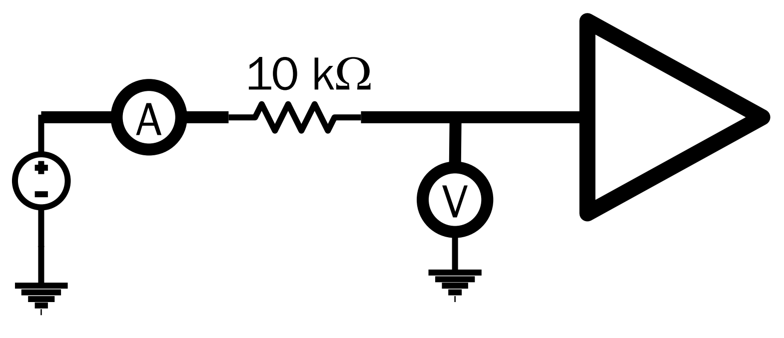
- We connect the SiPMs to the SMART and keep $V_{bias} < V_{breakdown}$
- For each channel (ch0-ch15) we loop over DAC value for ch17
  - *The optimal value ('calibration' value) is obtained when the ADC value becomes larger than 0*



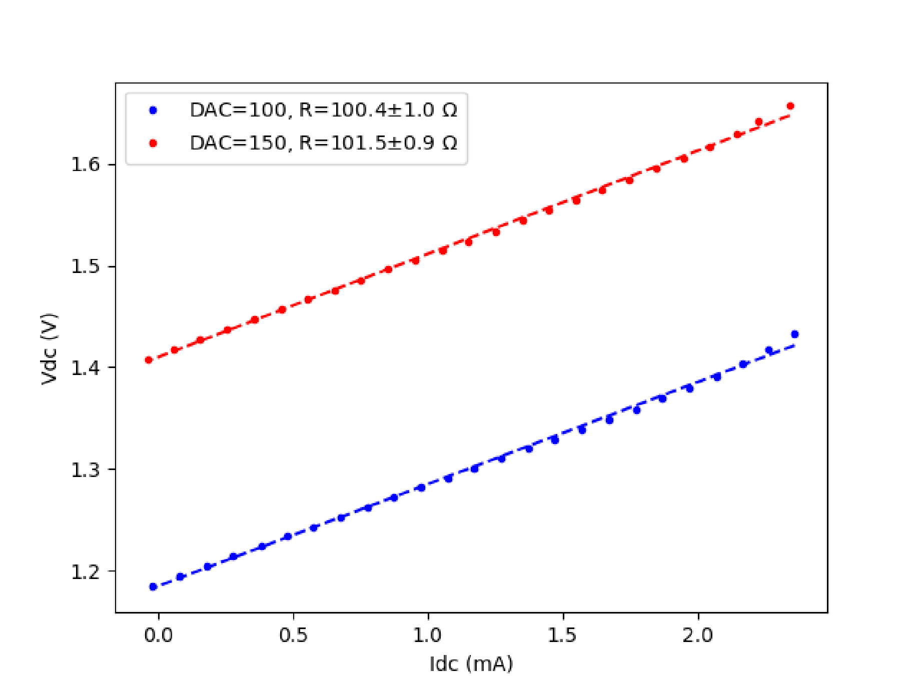
DAC 'calibration'



Internal resistance



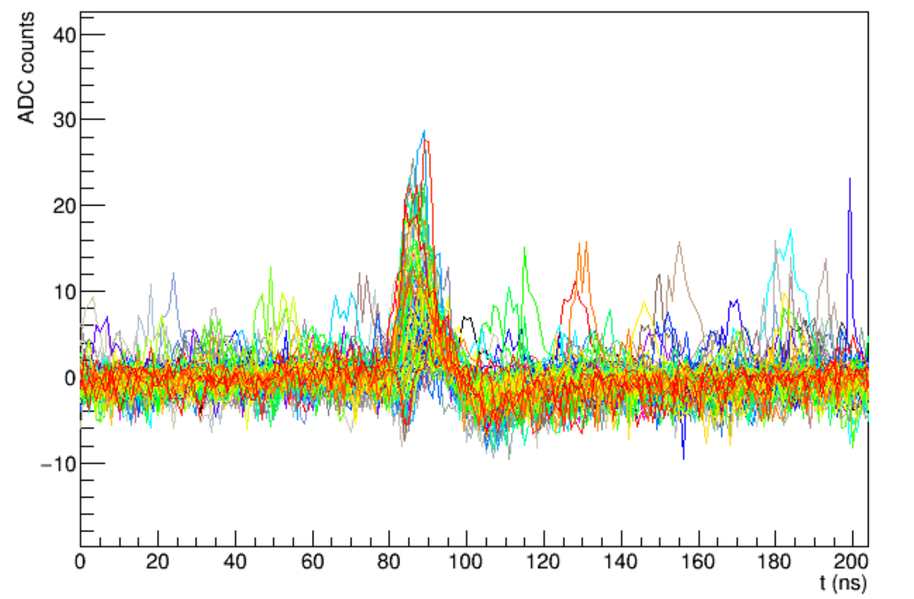
- We connected the input of channel 0 to a voltage source with a series resistance
- We changed the input voltage and measured the injected current and the voltage at the input of the SMART channel

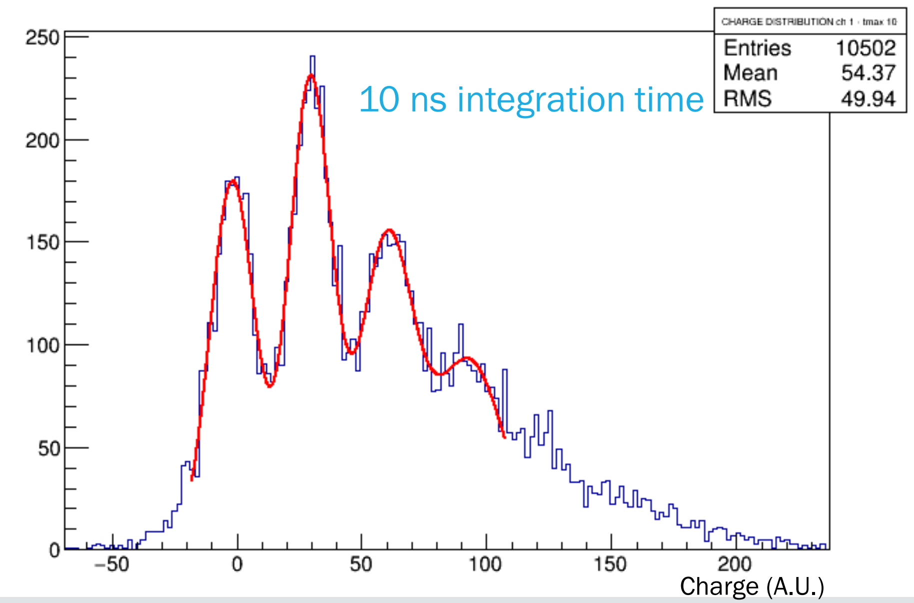


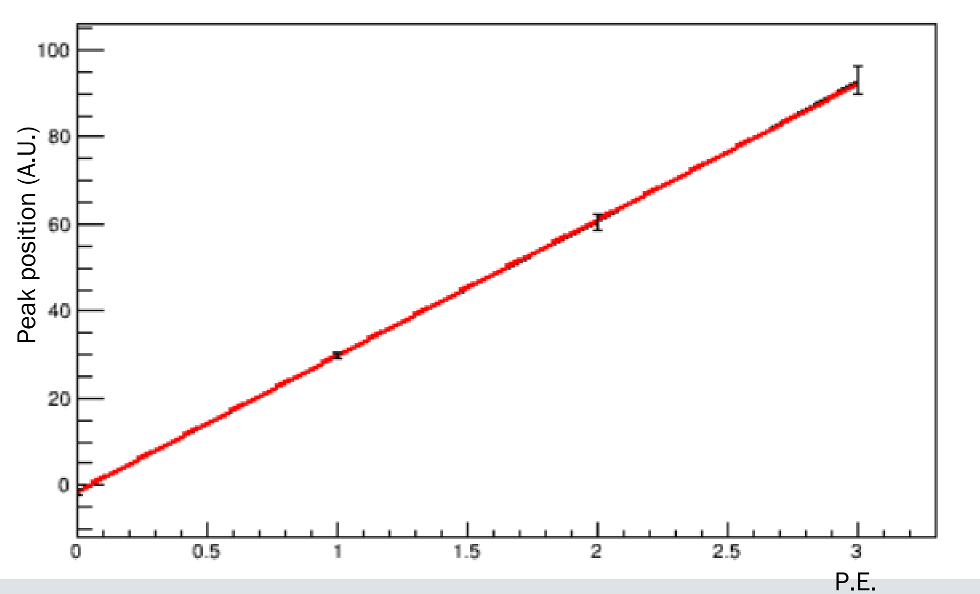
Resistance is approximately 100 Ω
The different DAC settings change the absolute voltage values but not the slope

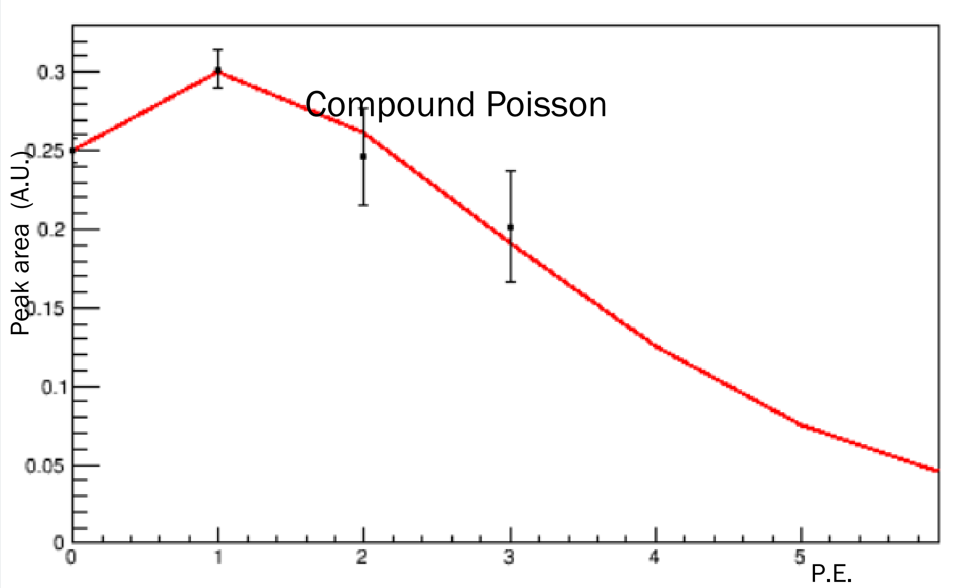
The channel was tested injecting a current up to 2.35mA without any damage

1 pixel
DAC = 100









SMART configurations loop

Amplitude, FWHM and tail recovery time of each channel reported for 4/10 configurations

Good uniformity among channels for a fixed configuration