ATLAS toward the High Luminosity era: challenges on electronic systems

F. Tartarelli (INFN – Milano)
On behalf of the ATLAS Collaboration

15th Pisa Meeting on Advanced Detectors, La Biodola, Isola d'Elba, May 22-28, 2022

ATLAS PHASE-II UPGRADE

A large upgrade program (Phase-II upgrade) has been started by the ATLAS detector to cope with operational conditions at the planned high luminosity upgrade of LHC (HL-LHC)

- Center-of-mass energy: 14 TeV
- Instantaneous luminosity: 7.5×10^{34} cm^{-2} s^{-1} (cf. $\sim 2 \times 10^{34}$ cm^{-2} s^{-1} in Run 2)
- Integrated luminosity: 4000 fb^{-1}
- **Pile-up (average interactions/bunch crossing): 200 ($\times$ 5 higher than today)**

Phase-I upgrades done for current data taking (Run 3)

- LAr digital trigger electronics
- L1calo trigger
- New Small Wheel (sTGC + Micromegas) and sMDT + small-gap RPC in some regions (BIS78) of the Muon System

Phase-II upgrades(*)

- Completely new inner tracker (ITk) (**)
- New endcap timing layers (HGTD)
- Additional muon chambers will be installed,…

Moreover, significant changes in the existing front-end, off-detector and trigger electronics are foreseen for all the other systems

(*) H. Pernegger, 'General overview of ATLAS Upgrades projects for HL-LHC,' talk

(**) L. Gonella, 'The ATLAS ITk Detector System for the Phase-II LHC Upgrade,' talk

ELECTRONICS UPGRADE: DRIVING FACTORS

Performance

Aim to maintain (or improve) existing performance in terms of acceptance, efficiency, resolution, and background rejection for all the physics objects

Radiation resistance

Some existing components have limited radiation tolerance and would not withstand the additional expected doses

Ageing

Some components would have more than 20 yr. operation at the start of Run 4. Many components are obsolete and are difficult to maintain and repair

Reliability

Based on past run experience: increase redundancy, ease installation/removal for maintenance, reduce single points of failure

Trigger

Upgraded to handle the expected pile-up levels while keeping thresholds at today level

Will use highest granularity information and resolution to keep efficient and selective triggers

Detector readout electronics needs to be upgraded to be compatible with the future trigger scheme

TRIGGER UPGRADE

Single level hardware-based trigger

Dataflow from Tile, LAr calorimeters and Muon System at 40 MHz

L0 trigger

Feature extractors (FPGA-based) for calo and muons combined in Global Trigger: identify physics objects and calculate event-level physics quantities

Max output 1 MHz, ~5.2 TB/s, 10 μs latency (cf. 100 kHz, 0.29 TB/s, 2.5 μs of today L1)

Event Filter

At L0A will perform ITk tracking in regions based on objects identified by L0

Heterogeneous commercial system: CPU cores and possibly accelerators

Output 10 kHz, ~52 TB/s (cf. 1 kHz, ~2.9 TB/s today)

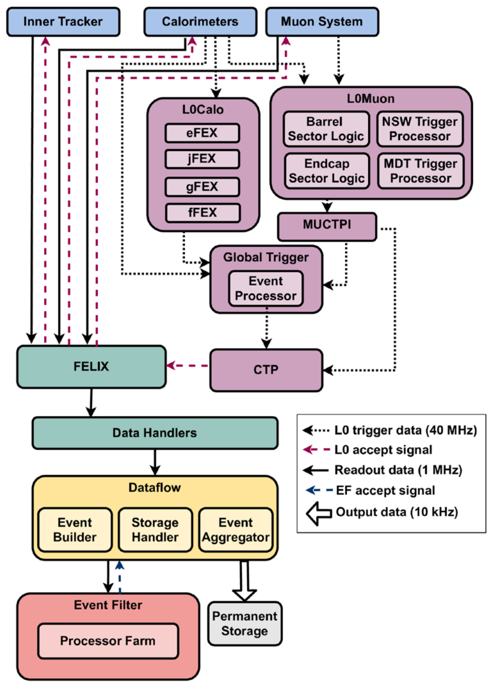
FELIX cards to connect FE serial links and DAQ commercial network

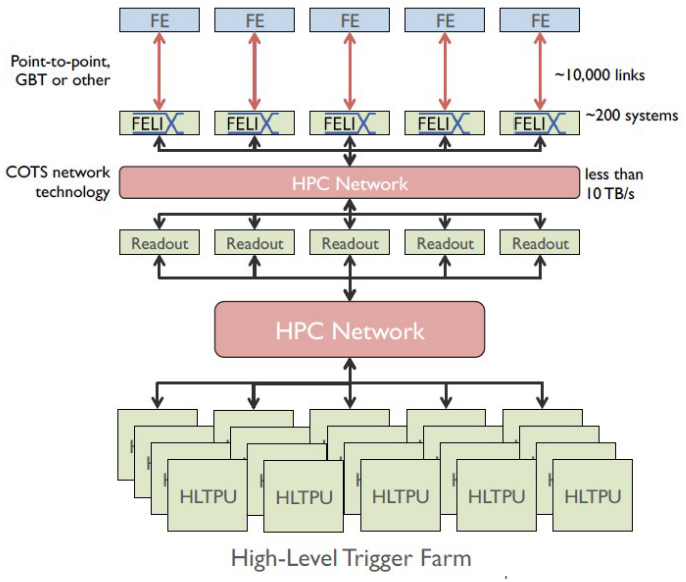
Custom-designed PCIe I/O cards in a commodity server (~ detector agnostic)

Will route all needed signals (readout, configuration, trigger, clock,…)

Phase-II FELIX: evolution of the FELIX being used in Phase-I upgrades

First prototypes of some of the required boards are available and are being tested (FELIX, L0Muon, Global Trigger,…)





ELECTRONICS UPGRADE

The electronics of the calorimeters and of the muon system is not compatible with this architecture

- **Replacement of both front-end and off-detector systems is needed**

Front-end electronics

- **Located on detector and subjected to radiation**
- Amplifies, shapes and digitizes signals coming from the detectors and ships the data off detector
- All on-detector buffers will be removed
- Full granularity data will be streamed off-detector at 40 MHz

Data is sent optically to off-detector electronics

- Large use of CERN GBT, lpGBT, VTRx,…

Off-detector electronics

- Fast pre-processors (FPGA-based) convert raw-data into calibrated information that feed the trigger system
- Buffer data awaiting trigger decision
- **Located in underground counting rooms not exposed to radiation**

RADIATION LEVELS

4000 fb^{-1} , max TID, 1 MeV equivalent neutron fluence, fluence of hadrons above 20 MeV

ITk inner layers (pixels, 2000 fb^{-1}– innermost 2 layers will be replaced after this dose)

14 MGy, 2.0×10^{16} n_{eq}/cm^2, 5.7×10^{16} $h_{>20\ MeV}/cm^2$

HGTD (plan to replace inner/middle rings after 1000/2000 fb^{-1})

1.2 MGy, 2.2×10^{15} n_{eq}/cm^2, 2.5×10^{15} $h_{>20\ MeV}/cm^2$

ITk outer layers (strips)

0.7 MGy, 2.0×10^{15} n_{eq}/cm^2, 2.1×10^{14} $h_{>20\ MeV}/cm^2$

Lar calorimeter (highest values in barrel crates)

1400 Gy, 4.1×10^{13} n_{eq}/cm^2, 1.0×10^{13} $h_{>20\ MeV}/cm^2$

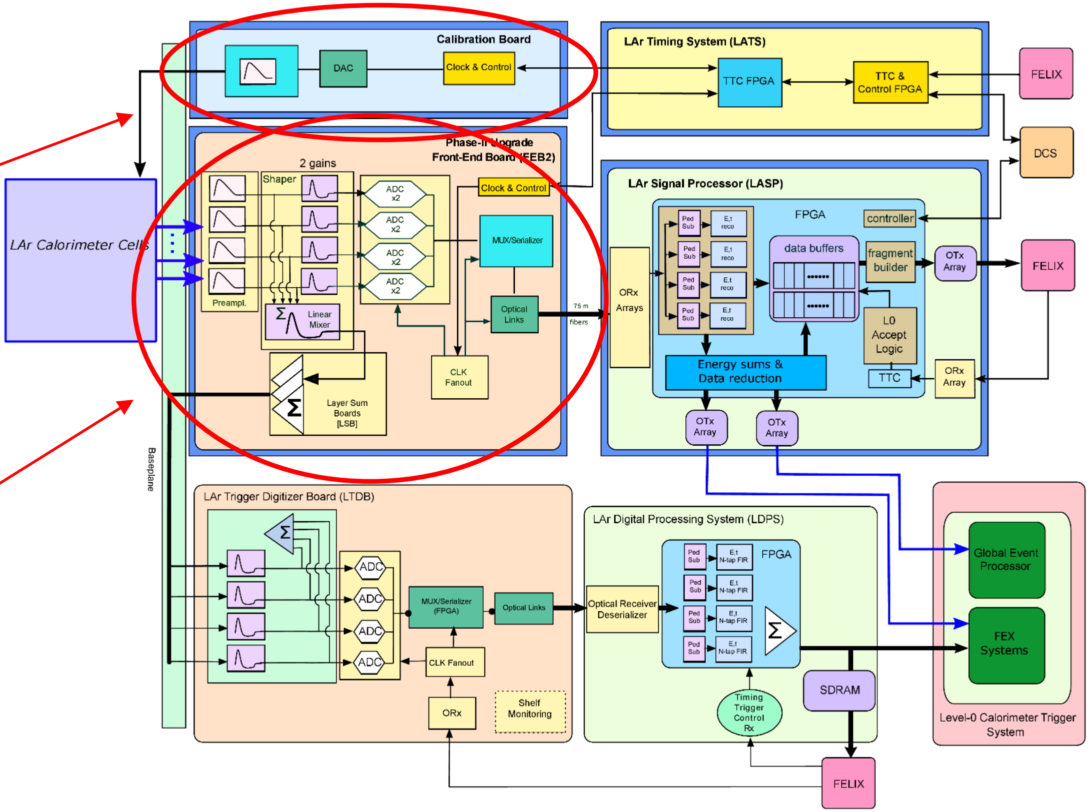
Tile calorimeter (at FE electronics)

110 Gy, 8.6×10^{12} n_{eq}/cm^2, 1.7×10^{12} $h_{>20\ MeV}/cm^2$

Require rad-hard design and qualification for TID and SEE (SEU, bit flips, latch-ups)

ASIC designs, links, DC/DC converters and linear regulators,…

LAr calorimeter (I)



No change to the detector but full replacement of front-end/off-detector electronics

Apart from the hadronic end-cap cold preamps

Calibration board ASICs:

CLAROC: pulser with high frequency switches
LADOC: custom 16b DAC used to command the HF switch

Front-end board (FEB2) ASICs:

PA/SH (ALFE2): 2 overlapping 14b gains to get 16b DR, shaper (CR-RC^2), Noise (ENI < 150nA), non-linearity (< 0.1%), cross-talk (< 20 mV for 50 Ω input). Within specs. TID tests OK
ADC (COLUTAv4): 15 bits (3b MDAC + 12b SAR), sampling at 40 MSPS
Verified low noise (1.2 ADC count on pedestal), cross talk, and ENOB > 11

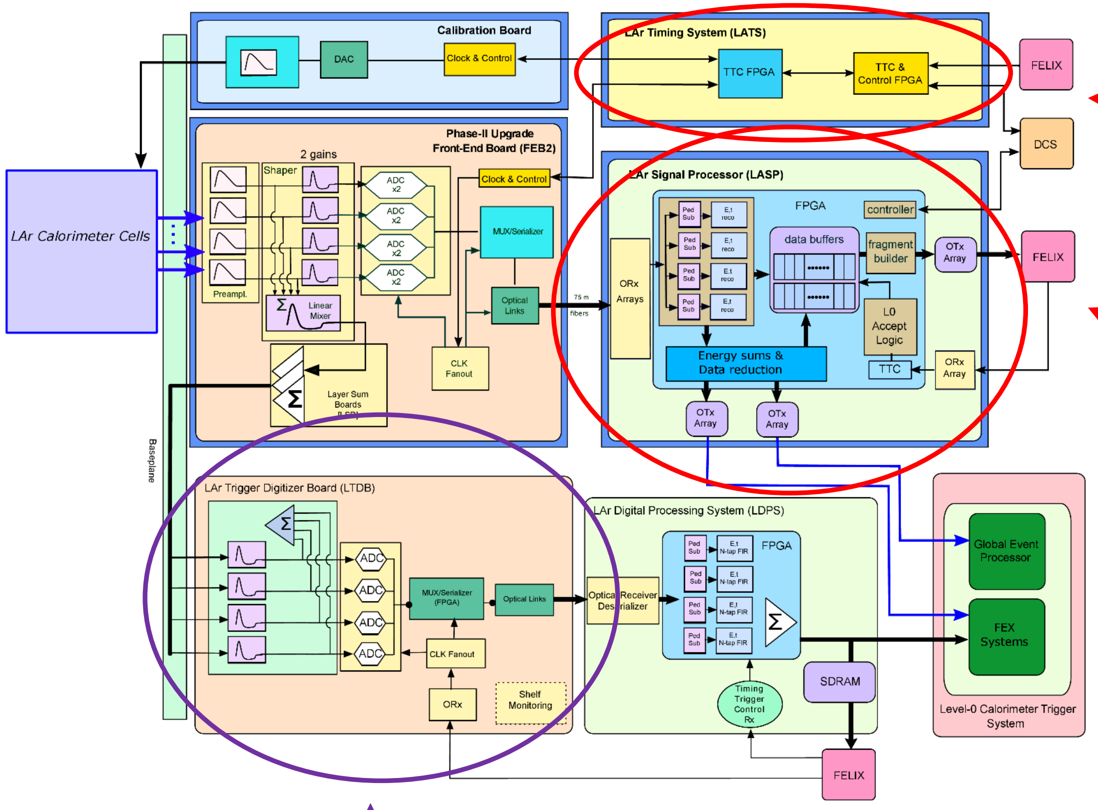
lpGBT + VTRX+ to send data off detector

FEB2 pre-prototype (32/128 ch) successfully built and tested

Demonstrated full readout chain and met analog specs

Calibration board pre-prototype (32/128 ch) also produced

LAr calorimeter (II)



Digital trigger built for RUN3 will also stay in Phase II

LATS

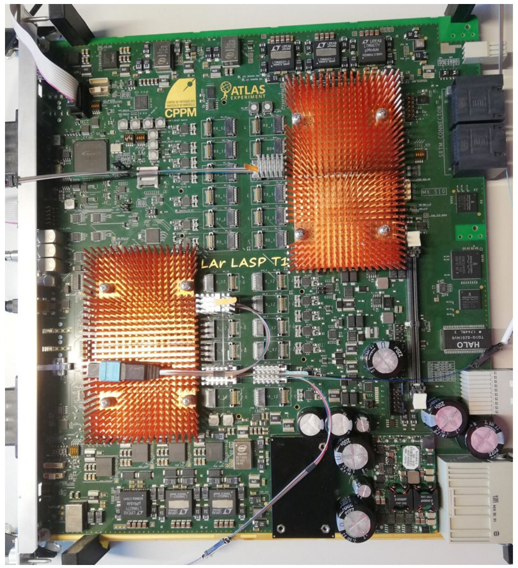
Trigger, Timing and Control (TTC) distribution, and configuration and monitoring of FEB2 and Calibration boards

LASP will receive calo cell data on optical fibers (> 33k links) at 10 Gbps

~345 Tbps data to be processed by the FPGA based boards, need large processing power

Apply digital filtering, calculate energy and time, and transmit to trigger and DAQ

Total number of boards, number of FPGA/board, type of FPGA (Stratix 10 or new Agilex series) still to be decided, balancing resource usage and power requirements



Smart Rear Transition Module (SRTM): provides LASP board interface for monitoring and data transmission to DAQ system

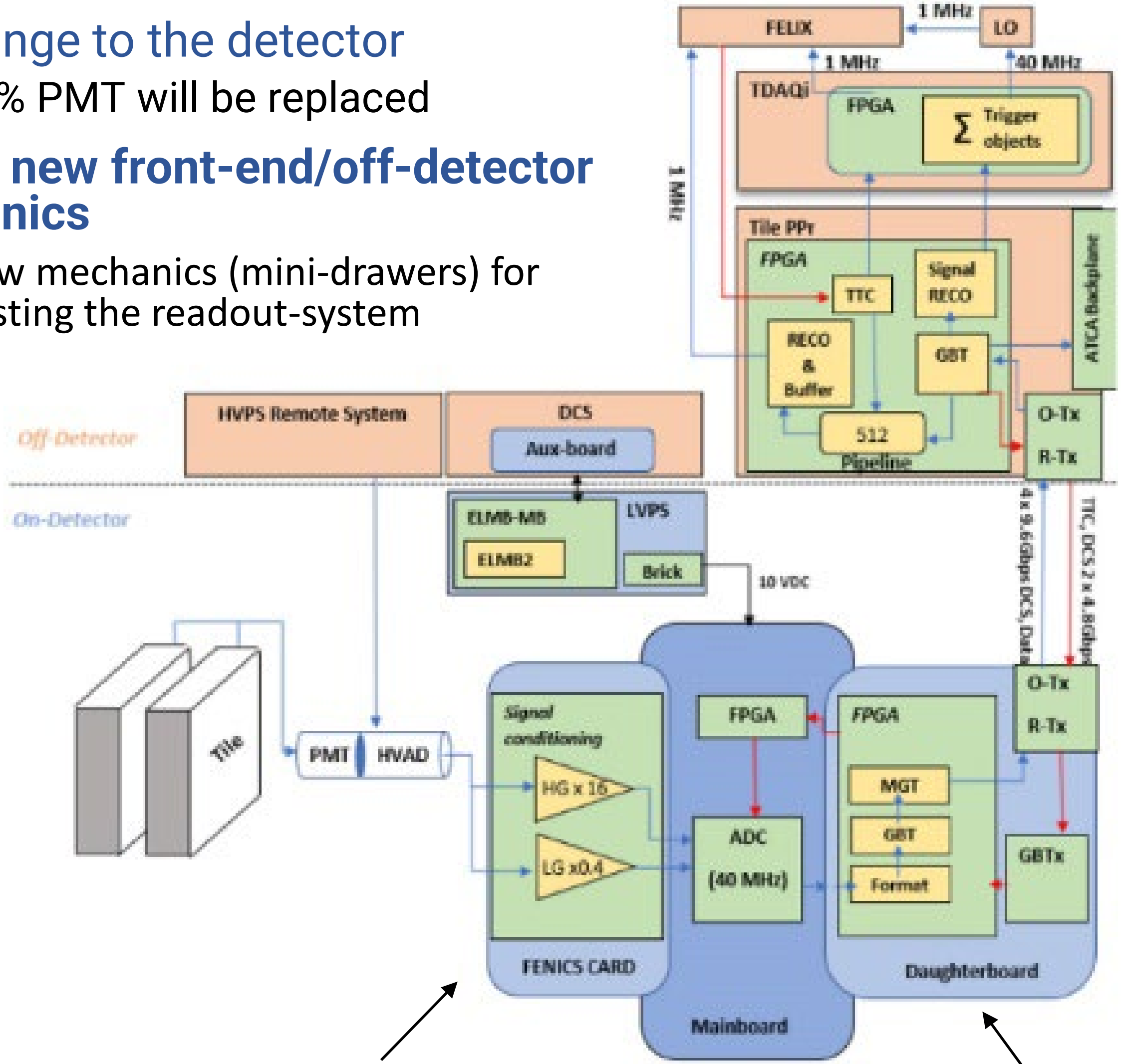
Tile calorimeter

No change to the detector

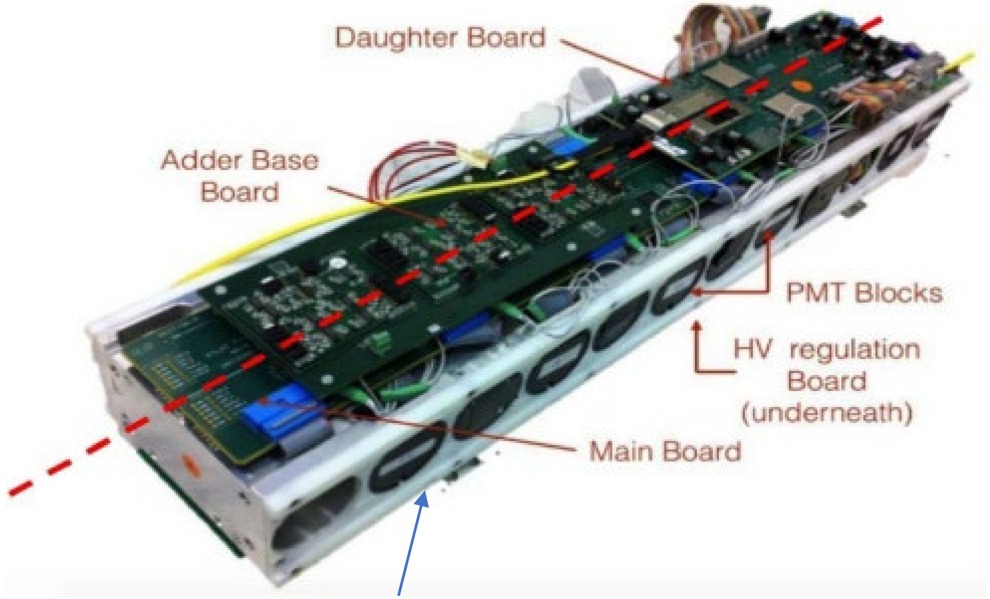
10% PMT will be replaced

Totally new front-end/off-detector electronics

New mechanics (mini-drawers) for hosting the readout-system



Control and readout of modules, propagation of TTC info, cell energy reconstruction, monitoring, trigger interface,...



A hybrid module with some of the new components (compatible with current system) will be kept inside the detector in Run 3

Pre-production done for FENICS and MB
Production of mini-drawers in progress according to the schedule

amplifier and shaper: 2 gains (1/40 ratio) to cover 17 bits DR (~200 fC - 1000 pC)

2x12b ADC at 40 MSPS

synchronize and send the digitized data off detector

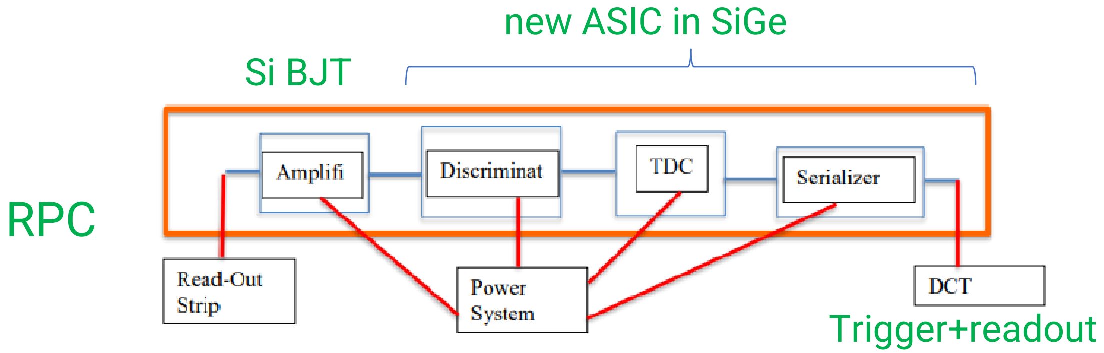
Muon System

Detector upgrade completes Phase-I upgrades already installed

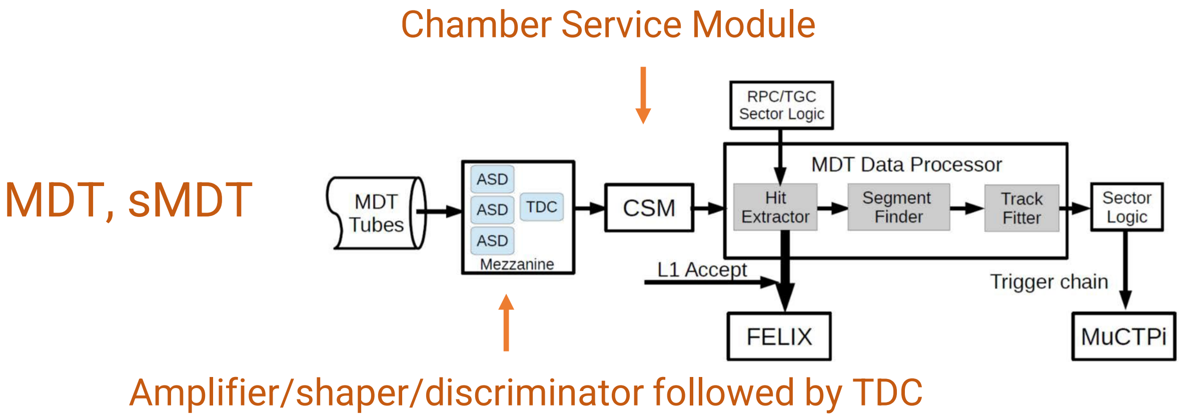
- RPC with thinner gaps, lower voltage, smaller effective signal threshold (barrel)
- New triplet layers of TGC (endcaps)
- New sMDT will replace MDT where space is limited for new RPC layer installation

MDT FE electronics will be replaced

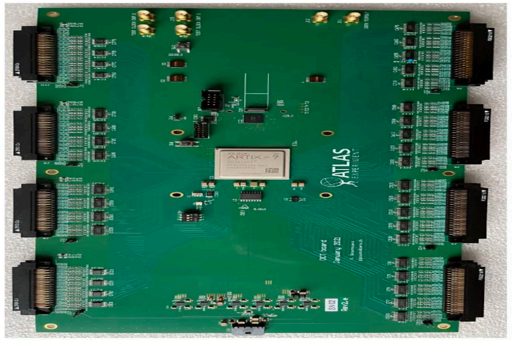
- MDT hits will also be used in trigger logic



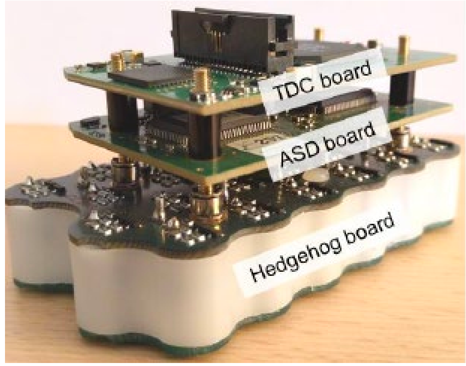
FE ASIC and DCT prototypes available



ASD produced, TDC production to start soon, CSM design progressing



BO-DCT prototype



MDT pre-proto mezzanine

ITk

Full silicon tracker (Pixel + Strip)

Pixel Readout chip prototypes available (ITkPixV1/1.1)

- TSMC 65 nm CMOS technology, successor of the RD53A chip
- 50 µm × 50 µm pixel pitch, 400 × 384 pixels, 20 x 21 mm^2
- Integrates charge generated in the pixel sensor, amplifies, digitizes the signal, and sends information to the DAQ system
- Differential FE, low settable threshold < 1000 e, 1 MHz readout
- **Triple Modular Redundancy (TMR) for critical parts (configuration, state machine, buffer pointers,…)**

Intense testing campaign in the last year, few issues understood and addressed

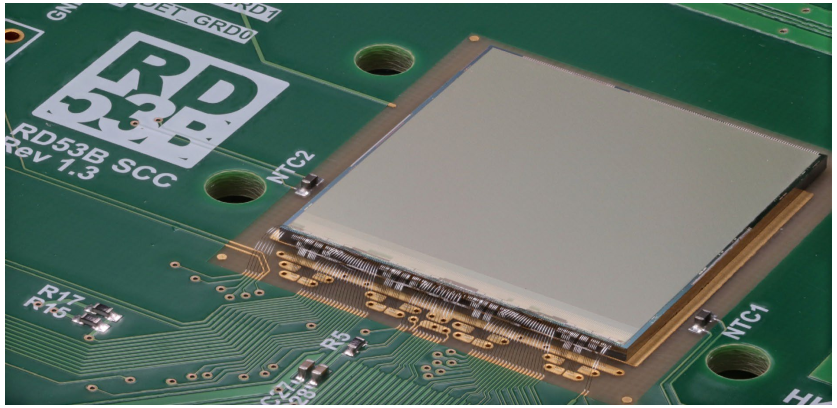
- Design of ITkPixV2 completed and will be soon be submitted

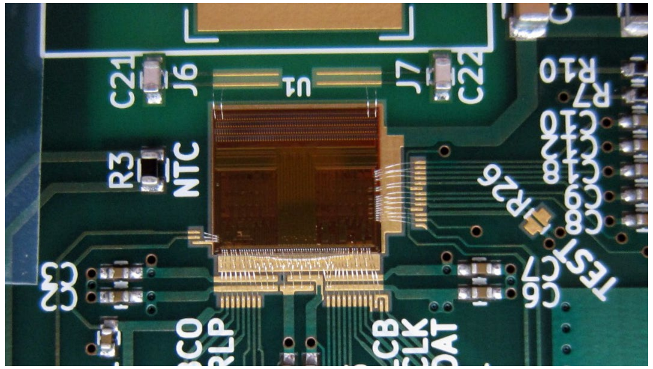
Three ASICs needed for Strip sensors FE

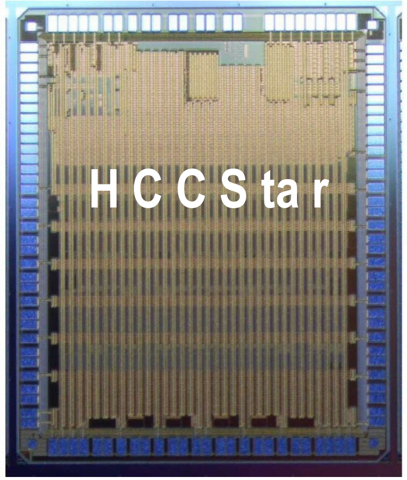
- **ABCStarV1:** 130 nm CMOS, provides analogue amplification, shaping, binary discrimination, buffer pipeline, to read out 256 strips
- **TMR for registers, clocks and reset**
- **HCCStar:** hybrid controller
- **AMACStar:** analog monitor & control of temperature, voltage, current

ABCStarV1: production started, pre-production lots under probing

HCCStar/AMACStar: pre-production tests well advanced and are OK. Need to complete rad campaign







HGTD

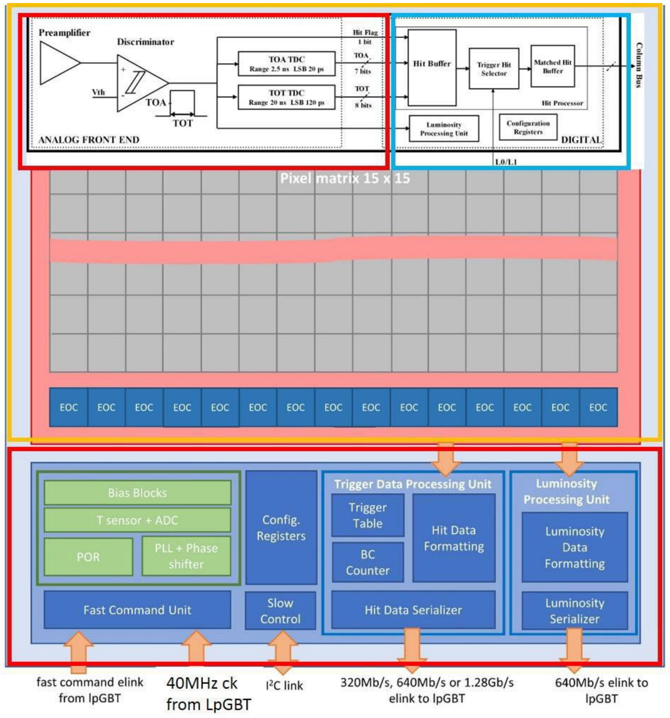
Two LGAD double-sided layers in endcaps ($2.4 < |\eta| < 4.0$)

- Precision timing information with a resolution of 30-50 ps per track
- Bunch by bunch luminosity information

LGAD

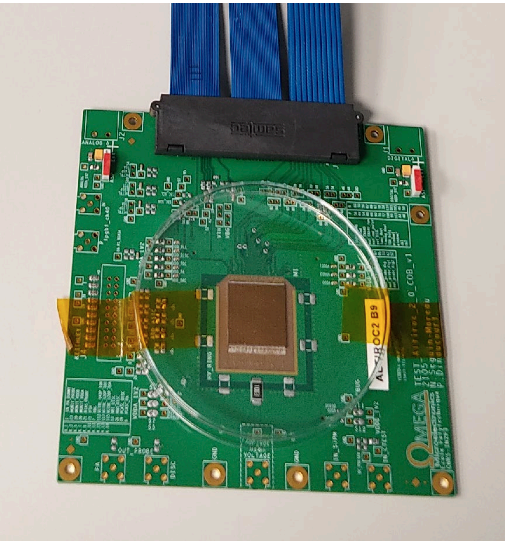
- 15×15 pads of size 1.3×1.3 mm^2, 50 μm thick
- Need 35-70 ps resolution per hit

Readout by ALTIROC chip (TSMC 130 nm CMOS)



- Size 2×2 mm^2 for 15×15 pads
- Preamp, TOA, TOT data per channel
- ALTIROC2 also includes data buffer and transmission
- Requirements: jitter $\sigma_t < 25$ ps, discriminator threshold 2 fC, low power < 300 mW/cm^2

ALTIROC2 being extensively tested right now



- Close to specifications

ALTIROC3 design well advanced but need to wait ALTIROC2 test results

- First rad hard version with triplication

POWER DISTRIBUTION

New electronics brings new requirements for FE power distribution (e.g., lower supply voltages: 1.2 V, 2.5 V,…)

- **Many power supply systems will need to be replaced**
- Increase reliability: ease of installation/removal for maintenance,…

Common strategy is to have a multi step-down conversion

- AC/DC conversion to a System Bus (SB) voltage in rad safe area
- SB is input to LVPS which create an Intermediate Bus (IB) voltage
- IB is brought to the FE: final step-down on-board by POL (DC/DC converters, LDO)

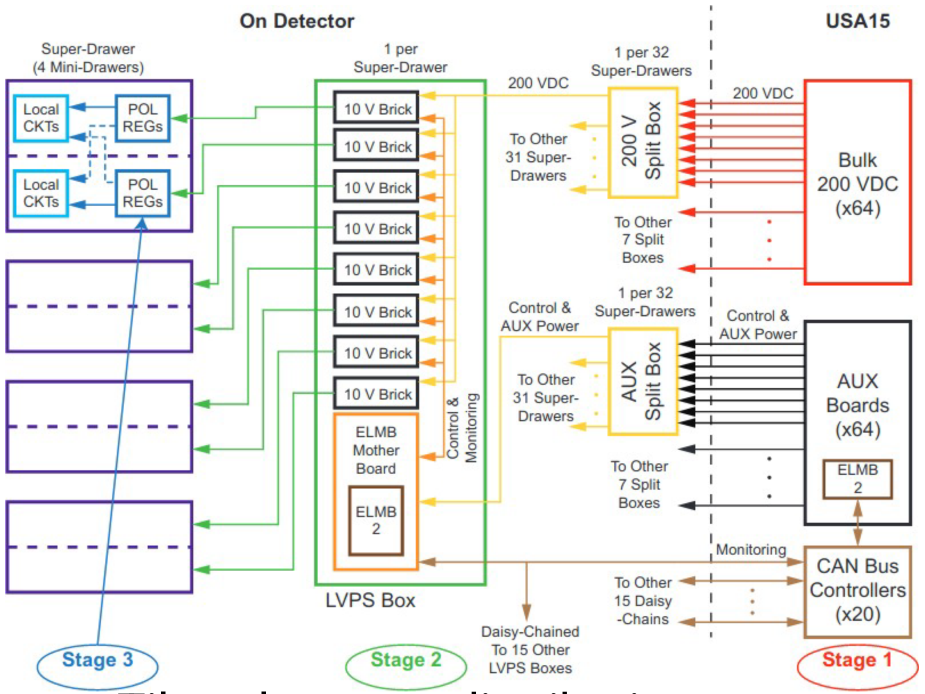
Scheme used by LAr, Tile, HGTD,… Depending on location, LVPS exposed to radiation and B field

E.g., for LAr calorimeter front-end: SB = 280 V, IB = 48 V

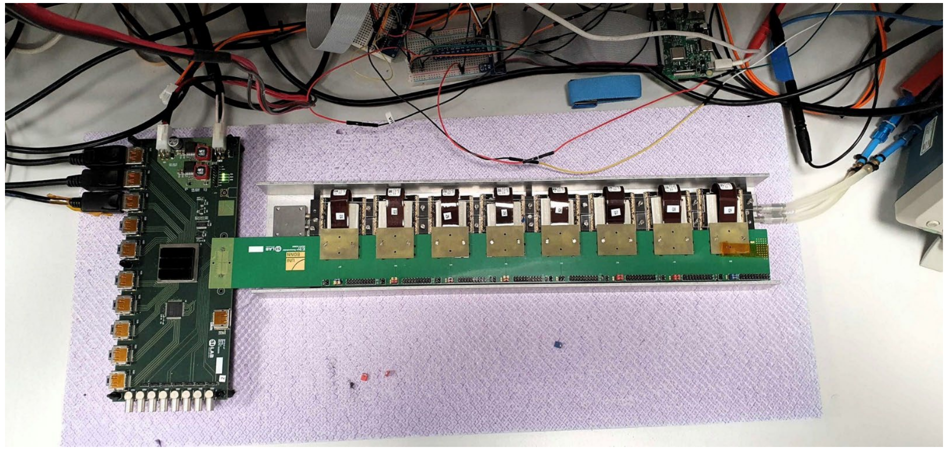
- LVPS (~4 kW) relocated in better accessible locations
- Final step-down: custom solution or new CERN bPOL48V (same family of bPOL12V, linPOL12V,… used e.g., in ITk strips)

ITk pixels will use serial power to reduce cabling and material budget

- On average 10 modules will be connected in series to a constant current source (up to 8 W of power)
- Two shunt-LDOs integrated in the FE chip allow analog and digital voltage regulation



Tile calo power distribution



SP chain of 8 ITkPixV1.1 quad modules

CONCLUSIONS

- ATLAS is making a significant upgrade to its detector to cope with the HL-LHC environment
  - Installation of new systems (ITk, HGTD,…)
  - Replacement of most front-end/off-detector electronics for calorimeters and muon system to allow full detector information in the trigger
- Trigger choice
  - L0-only trigger at 1 MHz and 10 μs latency, and commodity solution for HLT
- Good progress in the electronics of all systems despite the complexity of the upgrades
  - Many systems are completing the pre-production of components and entering series production
- Radiation hardness is a key issue for many systems and requires implementing robust ASIC designs and intense radiation test campaigns
- Foundry crisis is still affecting ASIC production schedules
- Global semiconductor shortage is causing long lead times and is increasing component prices