Contribution ID: **438** Type: **Poster**

Developing a Cluster-Finding Algorithm with Vivado HLS for the CBM-TRD

Friday, 27 May 2022 16:21 (1 minute)

Traditionally FPGA firmware was developed solely with Hardware Description Languages (HDL) such as Verilog or VHDL.
However, with the steady improvements of tools like Vivado HLS (High Level Synthesis) it is now possible to write parts of the firmware with higher level languages like C++.
Using HLS allows faster development cycles, easier code reuse and, most importantly, to efficiently write complex algorithms for the FPGA.

The Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) will investigate the QCD phase diagram at high net-baryon densities.
The experiment employs a free streaming data acquisition with self-triggered front-end electronics (FEE).
At interactions rates of up to 10 MHz the readout hardware has to process very high data loads.
The CBM Transition Radiation Detector (TRD) is equipped with the SPADIC front-end ASIC. The SPADIC allows for an oscilloscope-like sampling of the detector signals.
Additionally, the ASIC has implemented a forced neighbour readout logic which allows to read out pads adjacent to the pad, which fulfilled the trigger logic without lowering the threshold.
In order to do online event selection it is necessary to reduce the incoming data load inside the FPGA by combining the SPADIC trigger messages into clusters.
Achieving this with traditional HDLs is a very complex, time consuming task, which can be sped up significantly by using HLS.
In this contribution I will present how I developed and implemented a cluster-finding algorithm in the FPGA with Vivado HLS.

Collaboration

CBM

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Session Classification: Front End, Trigger, DAQ and Data Mangement - Poster session