Wafer-level testing of the readout chip of the CMS Inner Tracker for HL-LHC

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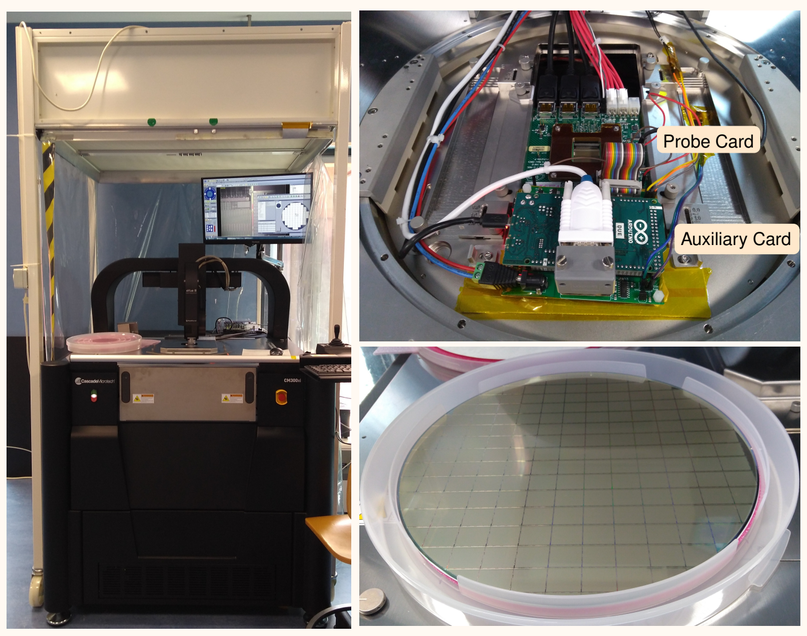
Introduction

- **CMS Inner Tracker** for **High-Luminosity LHC** (HL-LHC): pixel detector instrumented with 10^4 **CMS Readout Chips (CROCs)**
- **CROC characteristics**:
  - **65 nm technology readout chip**
  - Developed by the joint ATLAS-CMS RD53 collaboration
  - 432 × 336 pixels in approximately 4 cm^2
  - Very complex digital architecture for high energy physics
  - **Serial powering**: chips powered via current source
  - **20 wafers** produced for the **prototype chip CROCv1**
- **Wafer-level testing (WLT) activity**
  - Testing CROCs on wafers to **discard chips with manufacturing problems**
  - Critical importance for the detector: 30 % of wafer could be bad!
  - Also important to get calibration data and to characterise the prototype chip

Logos on a CROCv1 chip

Materials and methods

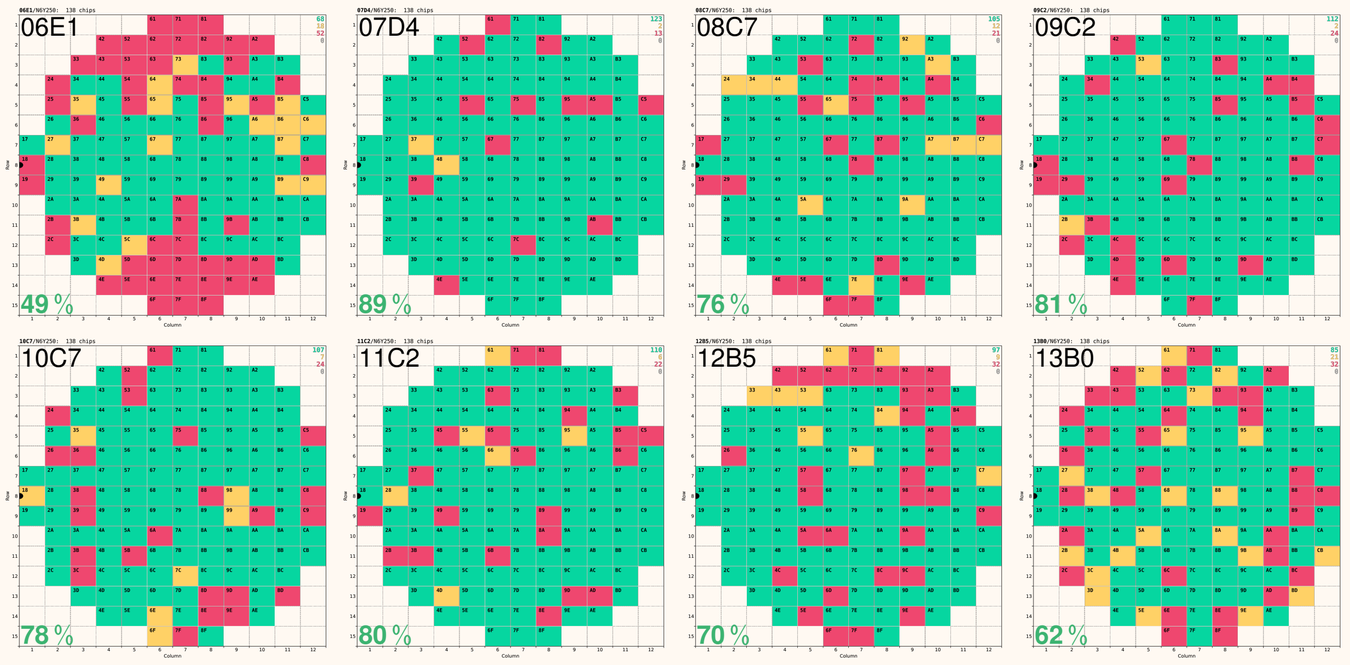
- **Waferprobing facility**: clean room of the INFN-TO Technological Laboratory
- 8 CROCv1 wafers for hybridisation (138 chips / wafer)
- Completely automated testing procedure
- Chip testing requires about 8 min (18 h for each wafer)
- **Wafer-level testing hardware**
  - Probe station: Cascade Microtech CM300xi (semi-automated)
  - Probe card: has 198 micrometric tungsten needles to contact the chip pads on the wafer
  - Auxiliary card: used for probe card control from PC
  - DAQ board: FPGA-based FC7
  - Remotely controllable instruments
- **Wafer-level testing software**
  - WLT software (Python): `croc_wlt`
  - DAQ software (C++): `Ph2_ACF`
- **Chip testing procedures**
  - Chip powering and measurement of power consumption
  - Measurement of chip signals
  - Chip trimming (main reference current and core voltages)
  - Communication testing
  - Registers verification
  - Chip calibrations (ADC, DACs, ring oscillators and *T* sensors)
  - Voltage regulator *IV*
  - Chip front-end testing (occupancy and S-curves)



***Left figure**: CM300xi probe station; **top right figure**: wafer-level testing hardware; **bottom right figure**: CROCv1 wafer (300 mm ⌀)*

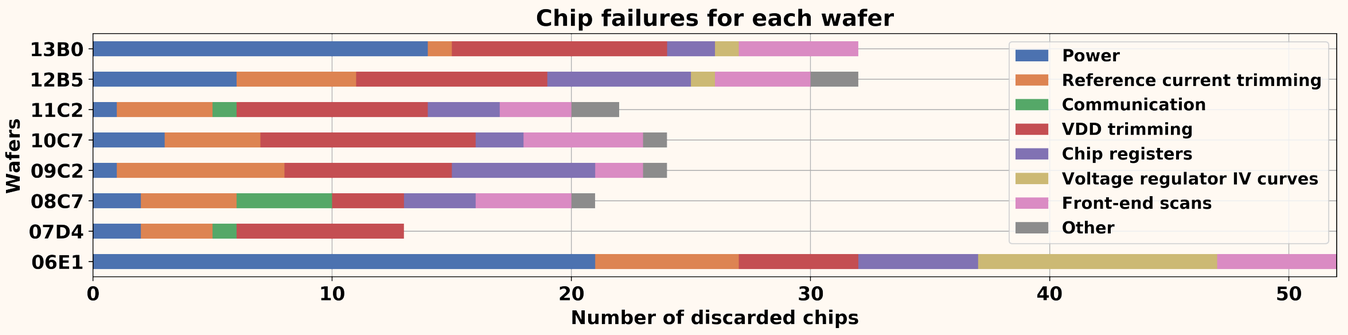
Results

- **Average yield** of the 8 tested CROCv1 wafers for hybridisation: **73 %**



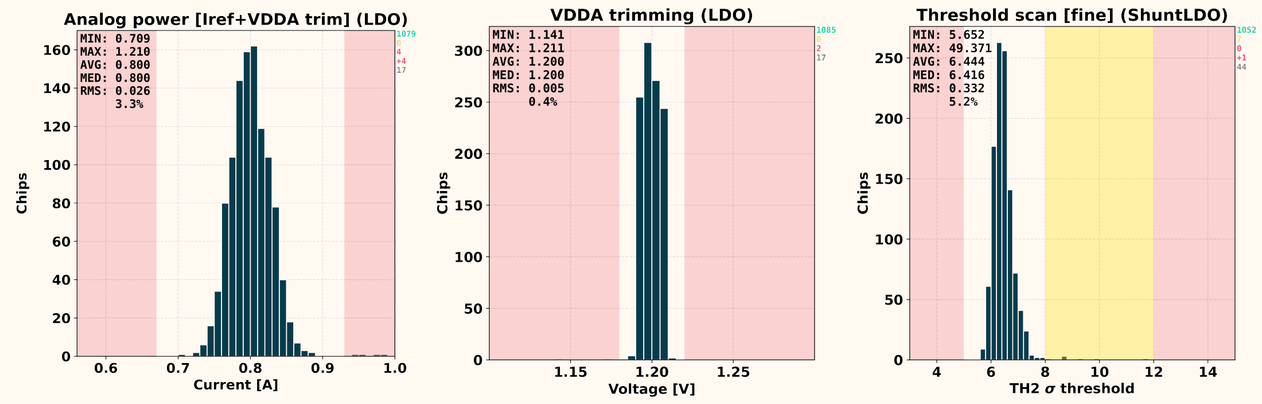
Preliminary wafer maps for the 8 tested wafers, sorted by wafer identifier

- **Rejected chips**: 220 out of 1104 (20 %) marked red and discarded
  - Most rejections due to **power anomalies** or **failed/marginal chip trimming**



Discarded chips with non-finalised wafer-level testing cuts

- **Calibration data**
  - Collected calibration data for hundreds of chips
  - Chip trimming (reference current and VDDA/D)
  - ADC, DAC, ring oscillators, temperature sensors
  - Calibration information will be stored in a CMS database
  - Data will also be used to produce and test modules
- **Characterisation data**
  - Large dataset
  - Analog current after chip calibration: (800 ± 26) mA
  - Digital current after chip calibration: (669 ± 11) mA
  - (421 ± 19) e threshold dispersion before tuning at 3100 e; after tuning: (35.2 ± 1.7) e
  - Much more



***Left, center figures**: calibrated analog current and VDDA distributions; **right figure**: threshold dispersion after tuning*

Discussion

- Wafer-level testing setup developed in Torino successfully commissioned for first waferprobing campaign on prototype readout chip for the HL-LHC CMS Inner Tracker
- Waferprobing data used to characterise the prototype chip and to get calibration information
- The tested chips will be used to produce prototype modules

Acknowledgements

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References

- *The Phase-2 Upgrade of the CMS Tracker* - CMS Collaboration (2017). Link: **cds.cern.ch/record/2272264**
- Chip reference manuals. Link: **cds.cern.ch/record/2665301**
- Wafer-level testing software repository. Link: **gitlab.cern.ch/croc_testing/croc_wlt**