Wafer-level testing of the readout chip of the CMS Inner Tracker for HL-LHC

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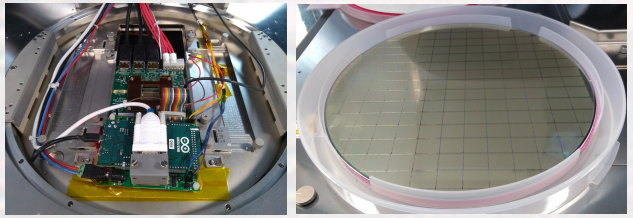
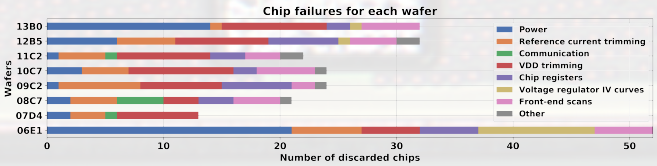
- The **CMS Inner Tracker**, in the **High-Luminosity LHC** (HL-LHC) phase, will be instrumented with more than 10^4 **CMS Readout Chips (CROCs)**
  - 65 nm readout chips developed by the joint ATLAS-CMS RD53 collaboration
  - Very complex chips with several design novelties (e.g., serial powering)
- A batch of 20 wafers of prototype CROC chips (CROCv1) has been produced
  - 8 of these wafers have recently been tested by the Turin INFN section for hybridisation
- **Wafer-level testing setup** developed at INFN Turin
  - Semi-automated probe station (Cascade Microtech CM300xi)
  - Custom electronics, such as the probe card and an auxiliary card for PC control
  - Python wafer-level testing software (**gitlab.cern.ch/croc_testing/croc_wlt**)
- **Wafer-level testing results**
  - Average yield of the 8 tested wafers is **73 %**
  - Rejected chips: 220 out of 1104 (20 %) marked red and discarded. Most rejections due to **power anomalies** or **failed/marginal chip trimming**
  - Obtained important **calibration** and **characterisation** data for hundreds of chips
- **Discussion**
  - Commissioned wafer-level testing setup at INFN Turn to test wafers from the first batch of CROC prototypes
  - Collected calibration and characterisation data useful for prototype modules production and testing



***Left figure**: wafer-level testing hardware; **right figure**: CROCv1 wafer (300 mm ⌀)*

Wafer maps examples



Discarded chips with non-finalised wafer-level testing cuts