MAPS-based tracking and vertexing for EIC

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on behalf of the EIC Silicon Consortium and the ATHENA Collaboration

Physics goals

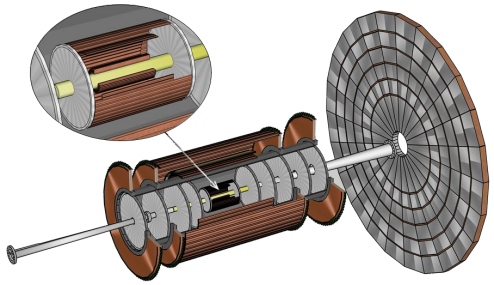
- High-precision primary vertex determination
- Secondary vertex separation capability

Detector requirements

- Spatial resolution:
  - **≤ 5 μm** in tracking layers and disks
  - **~ 3 μm** in the vertex layers
- Material budget:
  - **< 0.8 / 0.3 % X/X_0** per layer/disk
  - **< 0.1 % X/X_0** per vertex layer
- Power consumption 20 - 40 mW/cm^2
- Integration time 2 μs

Technology choice and proposed detector layout

- **65 nm MAPS** near the interaction point complemented by MPGD technologies at larger radii
  - 3 ultra-low mass bent MAPS layers for vertexing - 0.05% X/X_0
  - 2 MAPS layers for sagitta measurements - 0.55% X/X_0
  - 6 (hadron) + 5 (electron) MAPS disks - 0.24% X/X_0

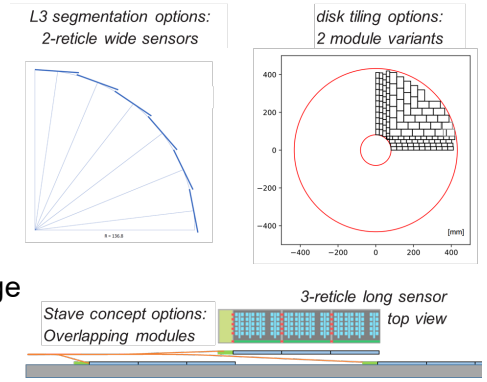


ATHENA proposal

Layers	Radius (cm)	Length (cm)
L0, L1, L2	~ 3.5 – 6.0	~ 28
L3, L4	~ 13 – 18	~ 35 – 48
Disks	**In/out R (cm)**	**z distance (cm)**
6 forward	~ 3.5 - 43	~ 25 – 165
5 backward	~ 3.5 – 43	~ 25 – 145

EIC Silicon R&D

- Vertex and tracking detector for EIC developed within the **EIC Silicon Consortium**
- Sensor development and characterization within the **ALICE ITS3** framework
- **Services reduction** via optimised powering and readout schemes *(eRD104 project)*
- **Detector development** *(eRD111 project)*
  - Module concept: adapt size and integrate in light support/bus
  - Stave and disk concepts: segmentation for high yield, low cost, max coverage
  - Mechanics and Cooling: air cooling on carbon foam



Conclusions

- EIC Vertex/Tracker proposed by ATHENA
- Based on 65 nm CMOS stitched sensor
  - Developed for the ALICE ITS3 project
  - Will be adapted to EIC needs
- R&D for Module, Stave, Disk is progressing
- Novel solutions studied for readout/powering

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