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FPGA-based techniques to improve fast track finding in the ATLAS Trigger

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This talk introduces and shows the simulated performance of two FPGA-based techniques to improve fast track finding in the ATLAS trigger. A fast track trigger is being developed in ATLAS for the High Luminosity upgrade of the Large Hadron Collider (HL-LHC), the goal of which is to provide the high-level trigger with full-scan tracking at 100 kHz in the high pile-up conditions of the HL-LHC. One option under development for achieving this include a method based on the Hough transform (whereby detector hits are mapped onto a 2D parameter space with one parameter related to the transverse momentum and one to the initial track direction) run on FPGAs.

This method can benefit from a pre-filtering step, to reduce the number of hit clusters that need to be considered and hence reduce the overall system size and/or power consumption, by examining pairs of clusters in adjacent strip detector layers (or lack thereof). This stub-filtering was first investigated by CMS but had been previously unexplored in ATLAS, and we will show the reduction in throughput enabled along with the performance impact on the Hough transform system of track finding, as well as estimates of resource usage.

One feature of the Hough transform method is that it identifies a large number of track candidates, which must be reduced before a second stage precision fit. A neural network has been developed to identify the most promising track candidates, and its promising performance will also be shown, in combination with and independent of stub filtering, along with the resources required to run it on an FPGA.

Collaboration

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