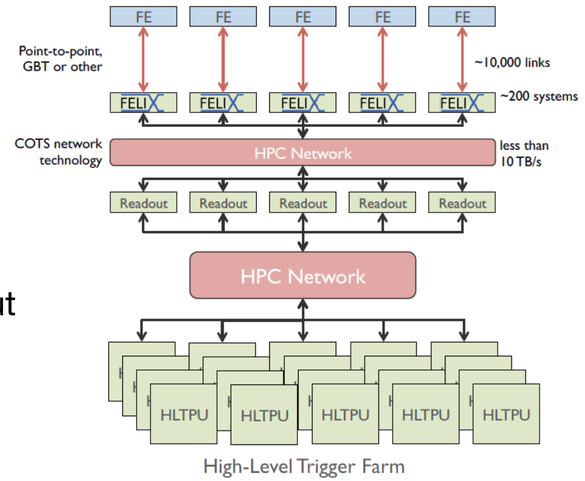
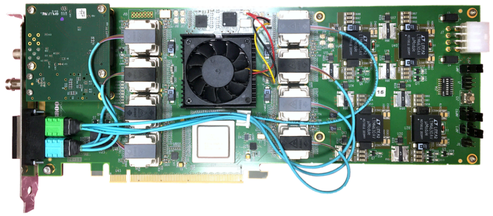
FELIX readout upgrade for the ATLAS Trigger DAQ system in HL-LHC

- HL-LHC will start data taking from 2029, the increased instant luminosity brings up new challenges to the Trigger DAQ system in various aspects
  - 10 times higher hardware trigger rate, i.e. 1MHz
  - Five times higher data readout rate (est. based on larger event size)
- In LHC Run 1 and 2, DAQ system consists a lot custom electronics that requires special crates. FELIX system largely changes this fact: one custom electronics installed on COTS servers, that communicates to software readout system through high performance ethernet network.
  - At HL-LHC, all the sub-detectors will be readout by the FELIX system
- Performance tests in HL-LHC environment carried out at the Nikhef FELIX testbeds, with specific setup:
  - 4U equivalent of standard 2U Run 3 server (i.e. same CPU)
  - Run 3 FELIX cards (FLX-712)
  - Varying number of links, packet size and other parameters
- The tested data taking modes show stable operation with trigger rate up to 1.1-1.2 MHz (required 1MHz at HL-LHC), giving confidence that the design will be able to scale to 1MHz trigger rate, given expected technology evolution over the coming years (e.g. doubled throughput with PCIe Gen4)
  - Studies and tests of techniques for maximising throughput is ongoing

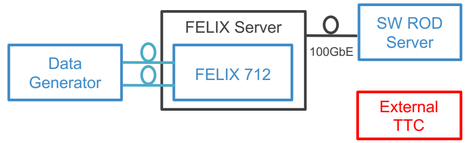
HL-LHC TDAQ system



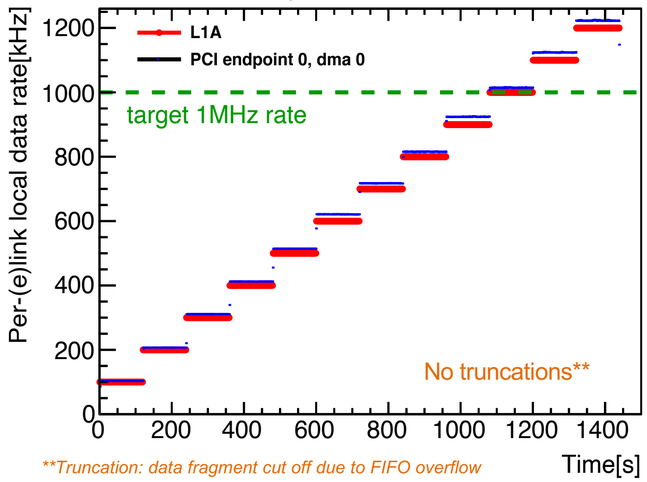
The Xilinx Kintex UltraScale FPGA based, FELIX phase I card



Performance Test Setup



364 bytes chunks, 24 links, FULL mode



**Truncation: data fragment cut off due to FIFO overflow*

Firmware FULL mode:
24 9.6 Gb/s links
- FELIX interface to other FPGA-based systems
- 24 links at 9.6 Gb/s 8b10b encoded (12 fully occupied links saturate the PCIe bandwidth)

Nikhef Radboud University
M. Wu (mengqing.wu@cern.ch), on behalf of the ATLAS TDAQ Collaboration

ATLAS EXPERIMENT