

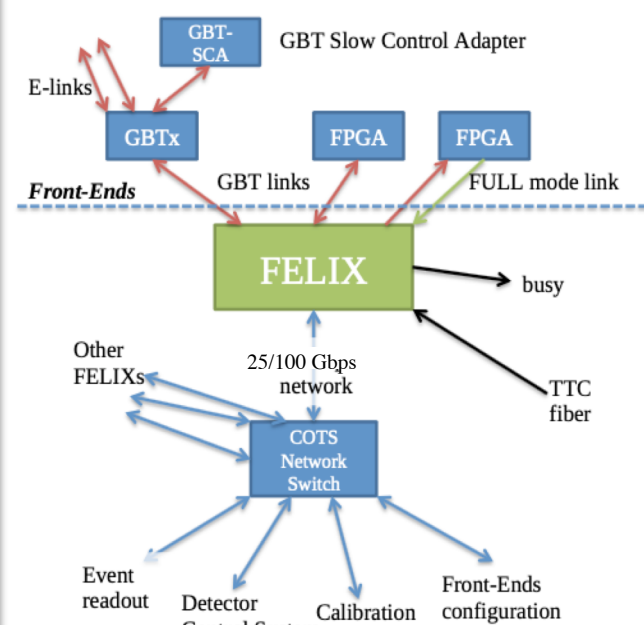
# FELIX: readout upgrade for the ATLAS Trigger DAQ system in HL-LHC

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On behalf of the ATLAS TDAQ Collaboration

## Introduction

- The Large Hadron Collider (LHC) collides proton bunches at a 40MHz rate
- ATLAS detects the collision products and the trigger systems select physics events of interest
  - The current (Run3) maximum event data rate for permanent storage is ~2 kHz
- New detector and trigger systems installed for Run 3 to improve background rejection
  - Hardware commissioning and deployment on-going
  - Three times average number of interactions per bunch crossing
  - 10 times higher hardware trigger rate
  - 5 times higher data readout rate (est. based on larger event size)
- The FELIX system functions as a router between custom serial links from front-end ASICs and FPGAs to data collection and processing components via a commodity switched network, while also forwarding Timing Trigger and Control (TTC) signals to front-end electronics [1]
- FELIX systems consist of COTS servers hosting one or two FELIX cards

## Run 3 FELIX system



## FELIX card for Run3

### Hardware

- Xilinx Kintex UltraScale FPGA
- 4/8 MiniPODs to support 24/48 bidirectional optical links
- 16-lane PCIe Gen3:
  - two 8-lane Endpoints with a switch
- Flash and Micro-controller to support firmware update
- Able to interface to multiple TTC architectures
- BUSY output

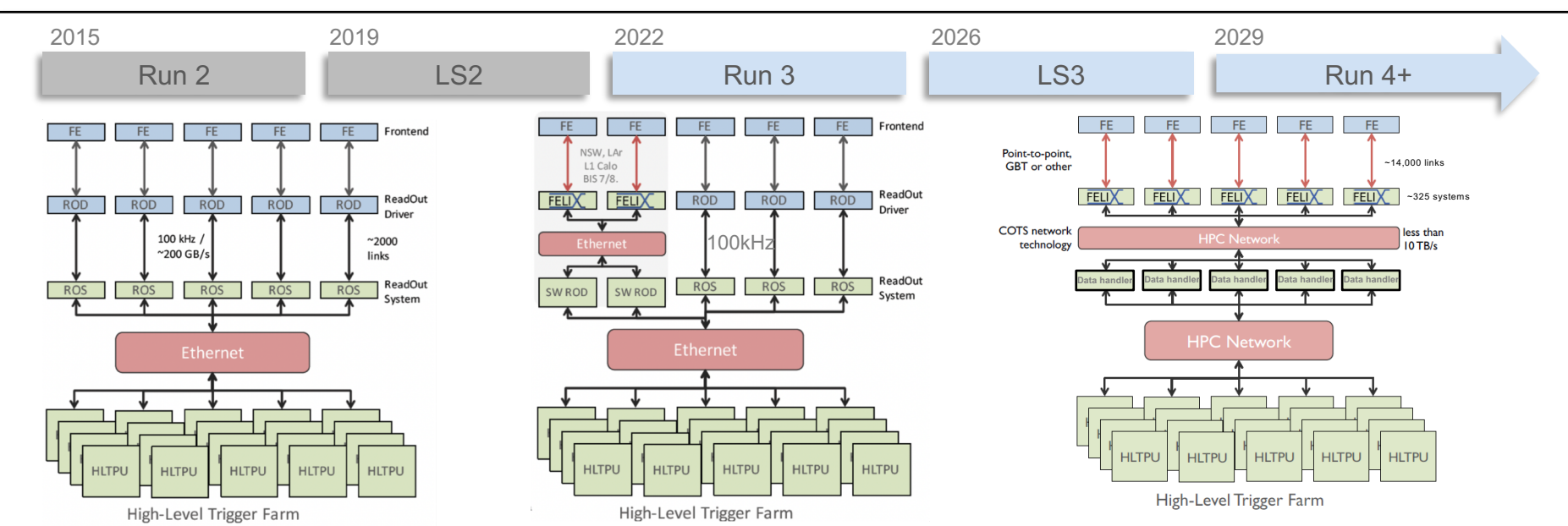
### Firmware GBT mode: 24 4.8 Gb/s links

- FELIX interface to GBTx (\*) ASICs
- Up to 24 GBT links per FLX-712
- One link (4.8 Gb/s) divided into up to 40 E-links with configurable bandwidth

### Firmware FULL mode: 24 9.6 Gb/s links

- FELIX interface to other FPGA-based systems
- 24 links at 9.6 Gb/s 8b10b encoded (12 fully occupied links saturate the PCIe bandwidth)

## A Glance at ATLAS Trigger DAQ system evolution

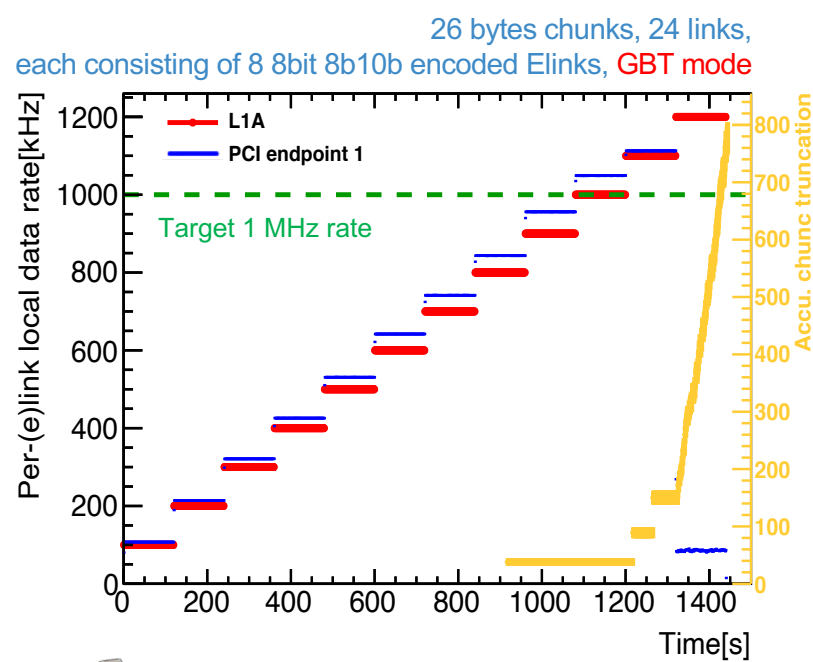
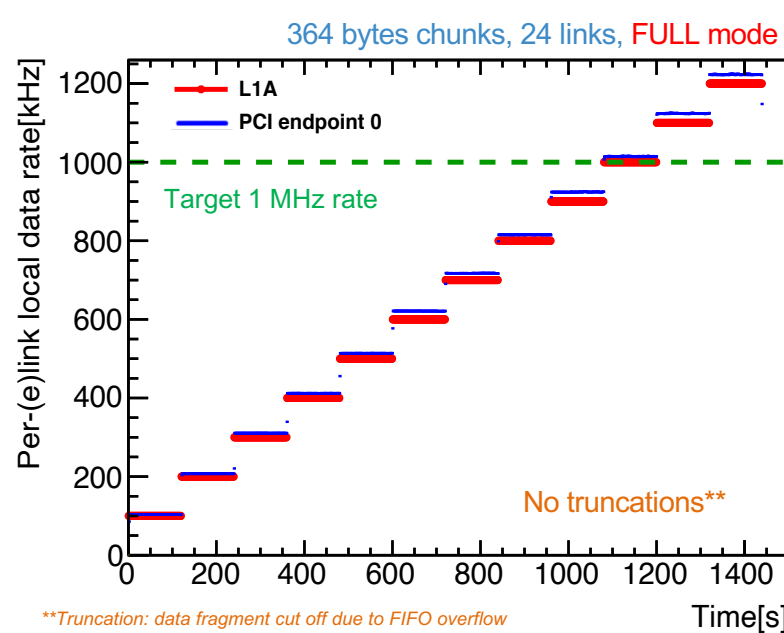
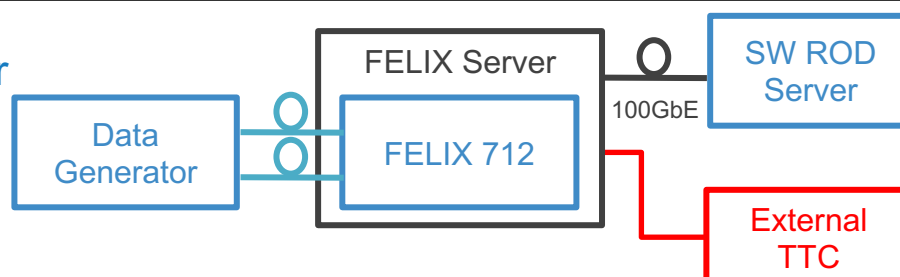


## Performance tests in HL-LHC environment

### Test with data discarded at FELIX server

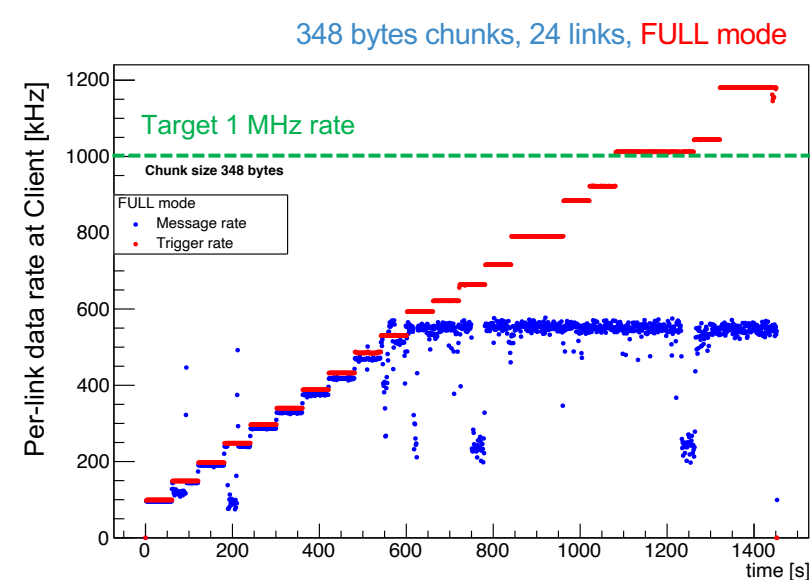
Local data processing mode shows stable operation up to 1.1 MHz for GBT mode, 1.2 MHz for FULL Mode

- required: 1 MHz



### Test with data transferred via network

Max data rate at around 0.58 MHz, limited by network backpressure that gives rise to event fragment truncation



## FELIX & Readout Software

- Uses RDMA (Remote Direct Memory Access) technology for low overhead transfers (custom 'netio-next' library)
- Low level software developed for basic configuration and monitoring.
- High level software developed for high rate data taking and channel monitoring.
- SW ROD – Run 3 software running on commercial computer, builds and aggregates events, detector-specific data processing
  - Data handler – new architecture to replace SW ROD, under development scalable for Run 4

## Conclusion and Outlook

- Tested 1 MHz Run 4 working point with specific setup:
  - 4U equivalent of standard 2U Run 3 server (i.e. same CPU)
  - Run 3 FELIX cards (FLX-712)
  - Varying number of links, packet size and other parameters
- Confidence that design will scale to 1 MHz trigger rate, given expected technology evolution over coming years
- Study and tests of techniques for maximizing throughput ongoing



(\*) GBTx = radiation hard chip aggregating FE electrical links, coupled to optical transceiver [2]  
[1] Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System, doi: 10.17181/CERN.2LBB.41AL  
[2] The GBT Project, doi: 10.5170/CERN-2009-006.342