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Operation of the SRS using the SAMPA chip: first results

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The Scalable Read-out System (SRS), developed within CERN's RD51 collaboration to assist the development and use of Micropattern Gaseous Detectors, suits applications from a small scale bench top experiments with a few hundreds of channels, up to large setups using several thousands of channels. Any ASIC collecting the charge events from the detectors can be integrated in the SRS, which will then transmit the data in the format defined by its FPGA.
In this work we present some of the most recent developments related with the integration of the SAMPA chip — developed for ALICE's TPC and Muon Chambers — in the SRS. The SAMPA chip is a 32 channel ASIC fabricated using 130nm CMOS technology, which provides a charge sensitive amplifier, a shaper and a 10-bit ADC for each channel, with a sampling rate that can reach 20 MS/s.
To test the acquisition system with charged particles, a muon telescope setup was mounted using a coincidence trigger provided by two scintillators and a small triple-GEM based TPC prototype (0.8L). The read-out is composed of 120 pads which are read by 4 SAMPA chips integrated with the SRS. In this work, we present a detailed description of the experimental setup, including detailed information on the SAMPA/SRS integration, as well as the experimental results obtained from muon tracks.

Collaboration

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