Operation of a TPC using the SAMPA chip integrated in the SRS

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Introduction

SAMPA chip [1] is an ASIC chip designed for large experiments such as the ALICE TPC and Muon Chamber, however, with a few developments of some specific electronics, it was possible to implement it as the front-end readout chip of the Scalable Readout System [2]. This work is divided into two parts. First we present the development in terms of electronics that were required to achieve this integration and later the first results and tracks of a small TPC that is using as the readout electronics the SAMPA integrated with the SRS.

The Scalable Readout System

Developed within the RD51 collaboration at CERN, the Scalable Readout System (SRS) is an multi purpose acquisition system. It is developed within the RD51 collaboration at CERN, the Scalable Readout System (SRS) is an multi purpose acquisition system. It is 100% compatible with SRS Slowcontrol protocol Compatible with main useful FEC board features 2-Clock domains. SAMPA overview:

- TSMC CMOS 110um, 1.25V technology
- 12 Channels per chip with Front-end = ADC + DSP
- Positive and negative polarities with 2 analog front-end models
- -20 or 30 µV/ï¿½C with 160 ns shaping time (Target sensor cap: 12 - 25 µF).
- -4 mV/ï¿½C with 300 ns shaping time (Target sensor cap: 40 - 80 µF).
- ADC: 10-bit resolution, up to 18.5 MSPS.

The physical dimensions are compatible with the readout plane (triggerless) acquisition is possible as well

When a trigger is received, a data frame of up to 1002 samples (per channel) is produced. Continuous (triggerless) acquisition is possible as well.

The total time window can reach 100 µs, however for our application we are using a window of approximately 200 frames (20 µs).

SAMPA simplifies and digitizes continuously while sending out data. A 192 samples buffer allows to compensate for trigger latency.

Up to 11 SELS links can be used to stream out the data.

Data traffic:

1. When a trigger is received, a data frame of up to 1002 samples (per channel) is produced. Continuous (triggerless) acquisition is possible as well.
2. In this work we set the acquisition rate to 10 MSPS (100 ns between samplings).
3. The total time window can reach 100 µs, however for our application we are using a window of approximately 200 frames (20 µs).
4. SAMPA amplifies and digitizes continuously while sending out data. A 192 samples buffer allows to compensate for trigger latency.
5. Up to 11 SELS links can be used to stream out the data.

The Front-End Card:

- FPGA Xilinx Virtex 6
- Ethernet 1Gbps
- External trigger input trigger
- 3 Clock domains

The readout of the detector is made of 120 pads, covering a total of 10 cm x 10 cm.

Two photo-multipliers, above and below the detector, were placed to create the trigger.

The detector is tilted in order to obtain longer tracks from cosmic rays.

Data processing

Set of waveforms recorded after a trigger:

1. Example 1: Small amplitude events related to noise, where the baseline occasionally crosses the 5n threshold.
2. Example 2: Artifacts yet somewhere unknown in the electronics that generated a pulse affecting many channels at the same time.
3. Example 3: Artifacts caused by the raise of the baseline after saturated pulses.

In the future we want to use the standard SRS softwares, developed by the system.

Work in progress

With that we can increase the rate and amount of the data retrieved by the system.

Solve digital communication issues that are already identified.

Optimize the hybrid component design.

Use the zero suppression and debugging features of the SAMPA chip.

The detector session: integration check the poster of our colleagues at the gaseous detector session.

References

2. The readout of the detector is made of 120 pads, covering a total of 10 cm x 10 cm.

More information

Acknowledgements and financial support

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GACR GA21-21801S (Czech Science Foundation).

Our sincere thanks to the whole GDD lab at CERN and to the SAMPA design team.

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SAMPA integration still being developed, but most of the artifacts can be solved with off-line event processing.

The developed hybrid and adapter board

SMPA chip

The SAMPA chip

Hybrid board overview:

- Four SAMPA chips operating at 300 MHz main clock
- Each hybrid provides 128 channels
- The physical dimensions are compatible with the readout plane (10 cm x 10 cm) developed by the RD51 collaboration

Adapter board overview:

- Each SAMPA chip is connected to one high speed serializer
- A single DisplayPort cable is used to connect the hybrid and the adapter board
- The adapter board has four deserializers and a PCI16 standard to connect a Front-End Card (FEC)

FPGA and Digital Results

Digital architecture blocks in our FEC’s firmware

- 16 independent serial decoder units at 300 MHz clock
- 1 Clock arbiter
- 38% Mean used of the Xilinx Virtex 6
- 100% compatible with main useful FEC board features
- Communication through USB packets
- SAMPA’s control communication through PCI

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SAMPA integration in a TPC

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SAMPA integration in a TPC

To test the SAMPA chip integrated with the SRS a small TPC prototype was built.

- 80 mm drift region.
- 3D printed PLA chamber.
- Field cage made of standard PCB strips and SMD resistors.

Detector setup:

- The triple-GEM detector is operated with a mixture of Ar/CO₂ (70/30) in open and continuous flow at a rate of 15 liters per hour at atmospheric pressure.

Data processing

Set of waveforms recorded after a trigger:

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