# Operation of a TPC using the SAMPA chip integrated in the SRS

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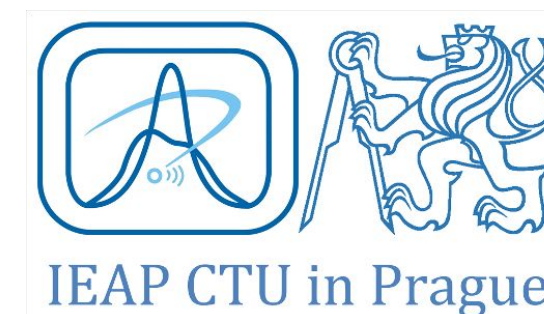
Introduction

SAMPA chip [1] is an ASIC chip designed for large experiments such as the ALICE TPC and Muon Chamber, however, with a few developments of some specific electronics, it was possible to implement it as the front-end readout chip of the Scalable Readout System [2]. This work is divided into two parts. First we present the development in terms of electronics that were required to achieve this integration and later the first results and tracks of a small TPC that is using as the readout electronics the SAMPA integrated with the SRS.

The SAMPA chip

SAMPA chip
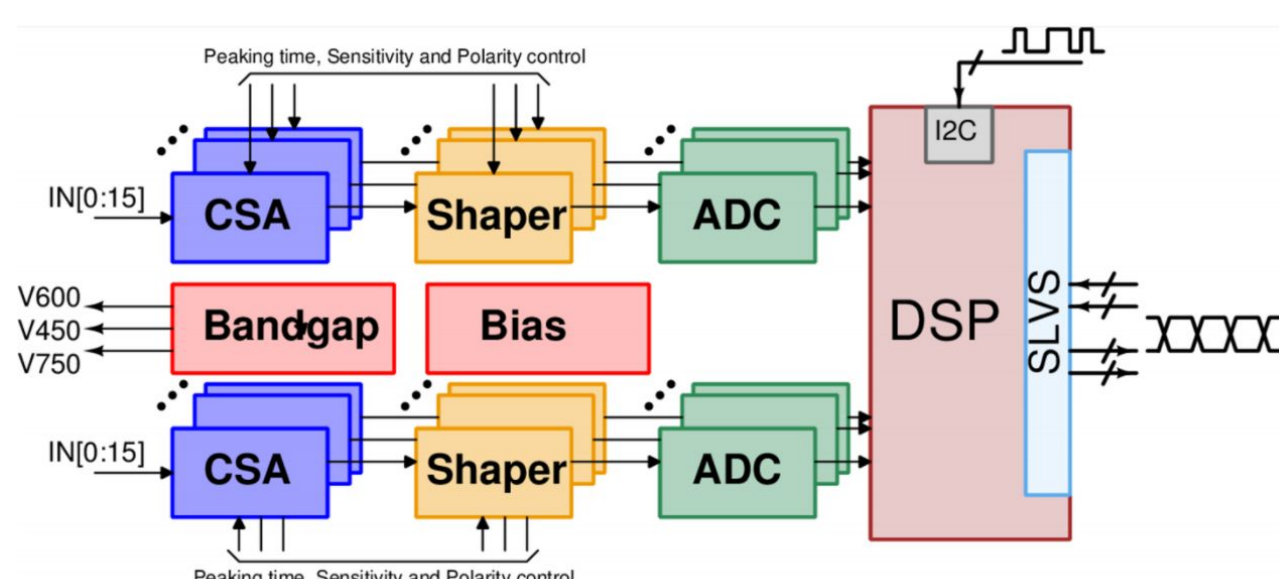
SAMPA's block diagram - image from [1]

SAMPA overview:

- TSMC CMOS 130nm, 1.25V technology.
- 32 Channels per chip with Front-end + ADC + DSP.
- Positive and negative polarities with 2 analog front-end modes:
  -20 or 30 mV/fC with 160 ns shaping time (Target sensor cap: 12 - 25 pF).
  -4 mV/fC with 300 ns shaping time (Target sensor cap: 40 - 80 pF).
- ADC: 10-bit resolution, up to 18.5 MSPS.

Data traffic:

1. When a trigger is received, a data frame of up to 1002 samples (per channel) is produced. Continuous (triggerless) acquisition is possible as well.
2. In this work we set the acquisition rate to 10 MSPS (100 ns between samplings).
3. The total time window can reach 100 µs, however for our application we are using a window of approximately 200 frames (20 µs).
4. SAMPA amplifies and digitizes continuously while sending out data. A 192 samples buffer allows to compensate for trigger latency.
5. Up to 11 SLVS links can be used to stream out the data.

The Scalable Readout System

Developed within the RD51 collaboration at CERN, the Scalable Readout System (SRS) is an multi purpose acquisition system. It is scalable in the sense that it can be used in middle size experiments with several thousands of electronic channels or small detectors such as the one used in this work, with dozens of them. The SRS can be used as common back-end electronics to support different types of detectors and its front-end electronics.
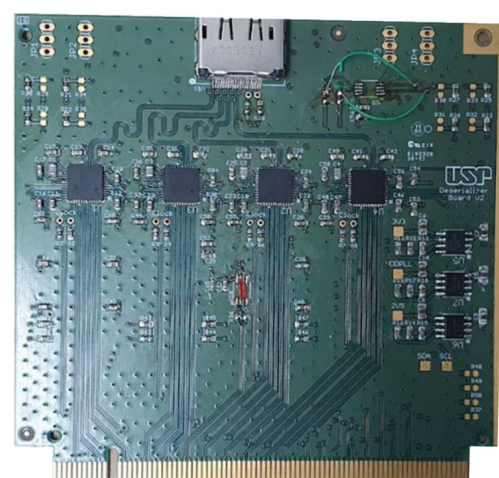

The Front-End Card:
- FPGA Xilinx Virtex 6
- Up to 20 LVDS I/O and 40 LVCMOS I/O
- Ethernet 1Gbps
- External input/output trigger
- Extensible firmware to new digital systems

The developed hybrid and adapter board


Hybrid board

Adapter board

Hybrid board overview:
- Four SAMPA chips operating at 300 MHz main clock
- Each hybrid provides 128 channels
- The physical dimensions are compatible with the readout plane (10 cm x 10 cm) developed by the RD51 collaboration

Adapter board overview:
- Each SAMPA chip is connected to one high speed serializer
- A single DisplayPort cable is used to connect the hybrid and the adapter board
- The adapter board has four deserializers and a PCIx16 standard to connect a Front-End Card (FEC).

FPGA and Digital Results
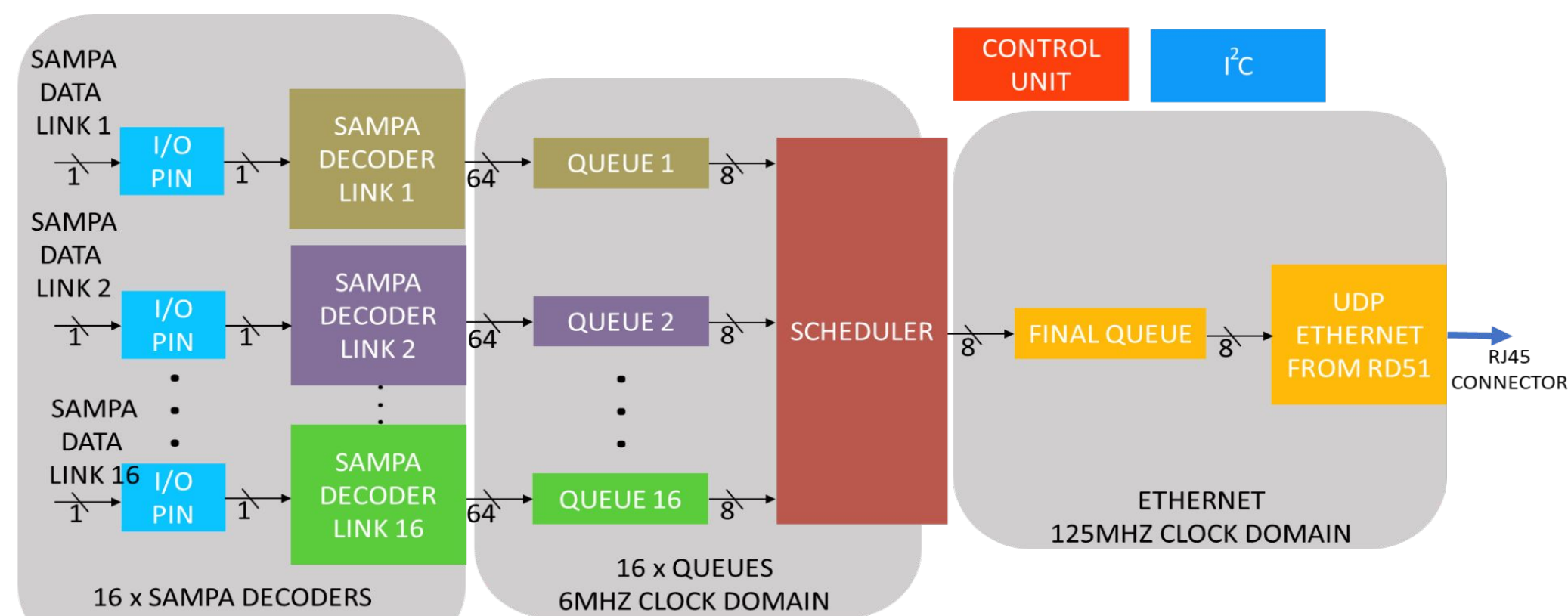
Digital architecture blocks in our FEC's firmware

- 16 Independent serial decoder units at 300 MHz clock
- 3 Clock domains
- 36% Slices used of the Xilinx Virtex 6
- Compatible with main useful FEC board features

- Communication through UDP packets
- 100% compatible with SRS Slowcontrol protocol
- SAMPA's control communication through I²C

SAMPA integration in a TPC

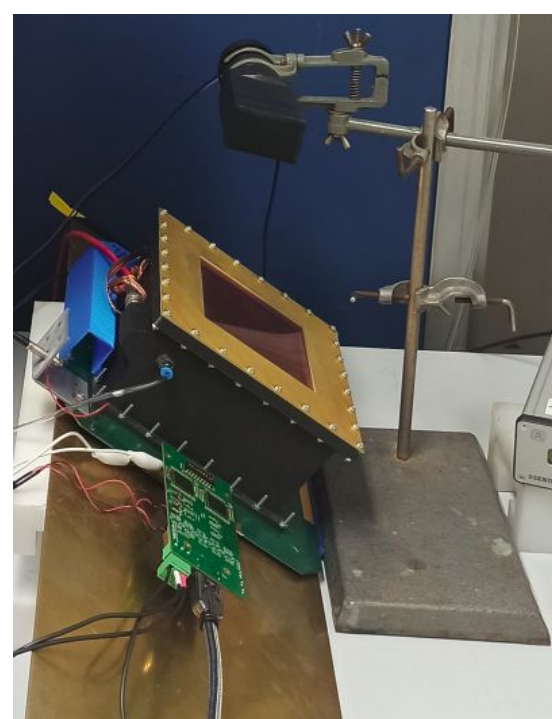To test the SAMPA chip integrated with the SRS a small TPC prototype was built.
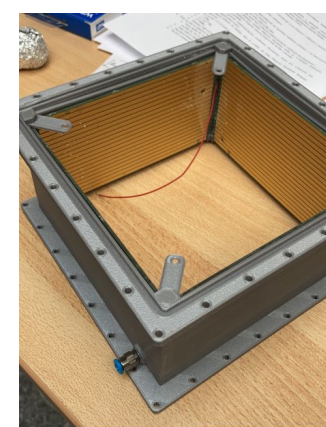
- 80 mm drift region.
- 3D printed PLA chamber.
- Field cage made of standard PCB strips and SMD resistors.
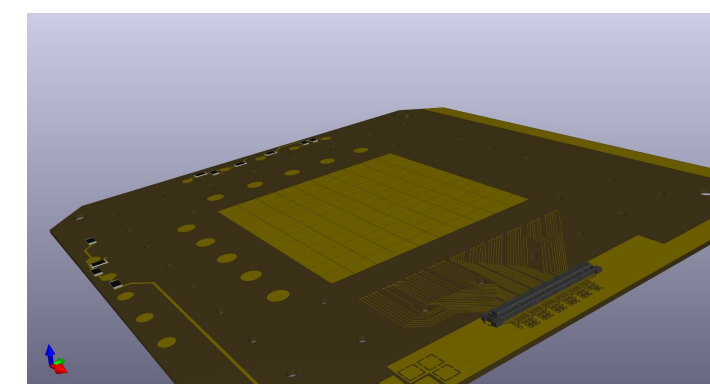
Detector setup:
- The triple-GEM detector is operated with a mixture of Ar/CO_2 (70/30) in open and continuous flow at a rate of 15 liters per hour at atmospheric pressure.

- Two photo-multipliers, above and below the detector, were placed to create the trigger.
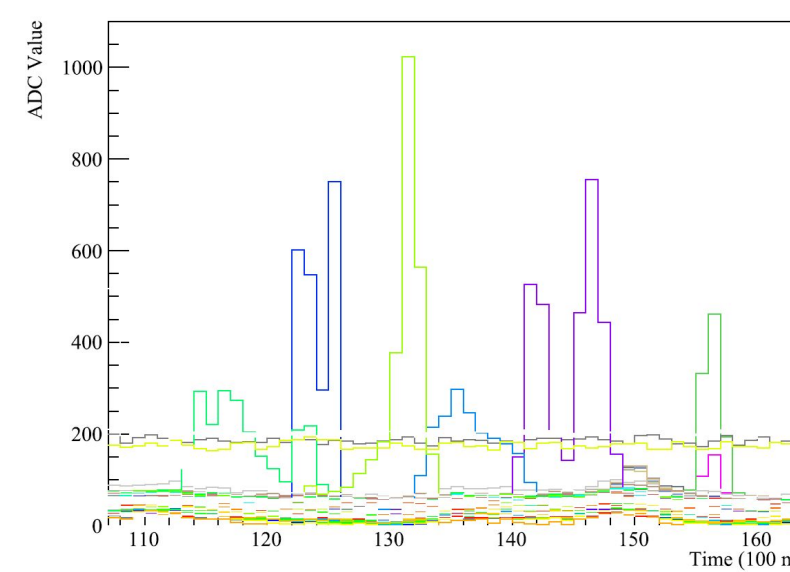- The detector is tilted in order to obtain longer tracks from cosmic rays.

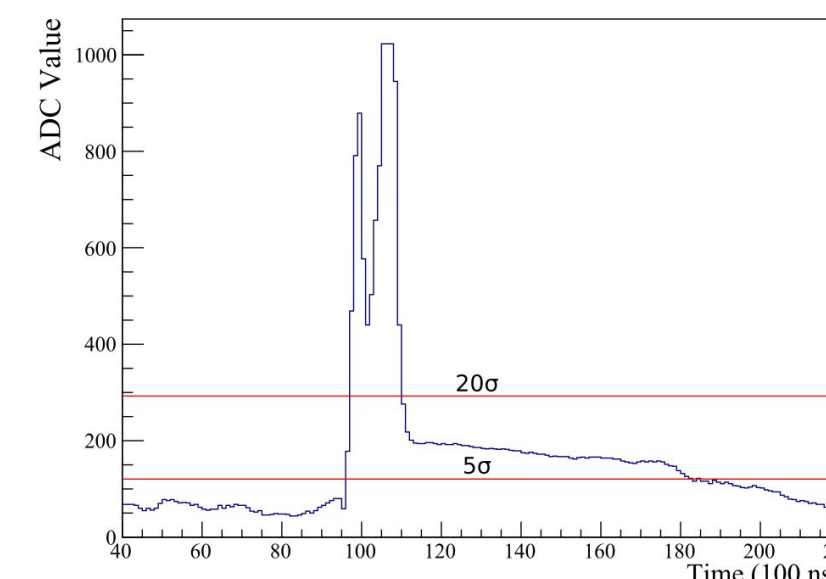- The readout of the detector is made of 120 pads, covering a total of 10 cm x 10 cm.
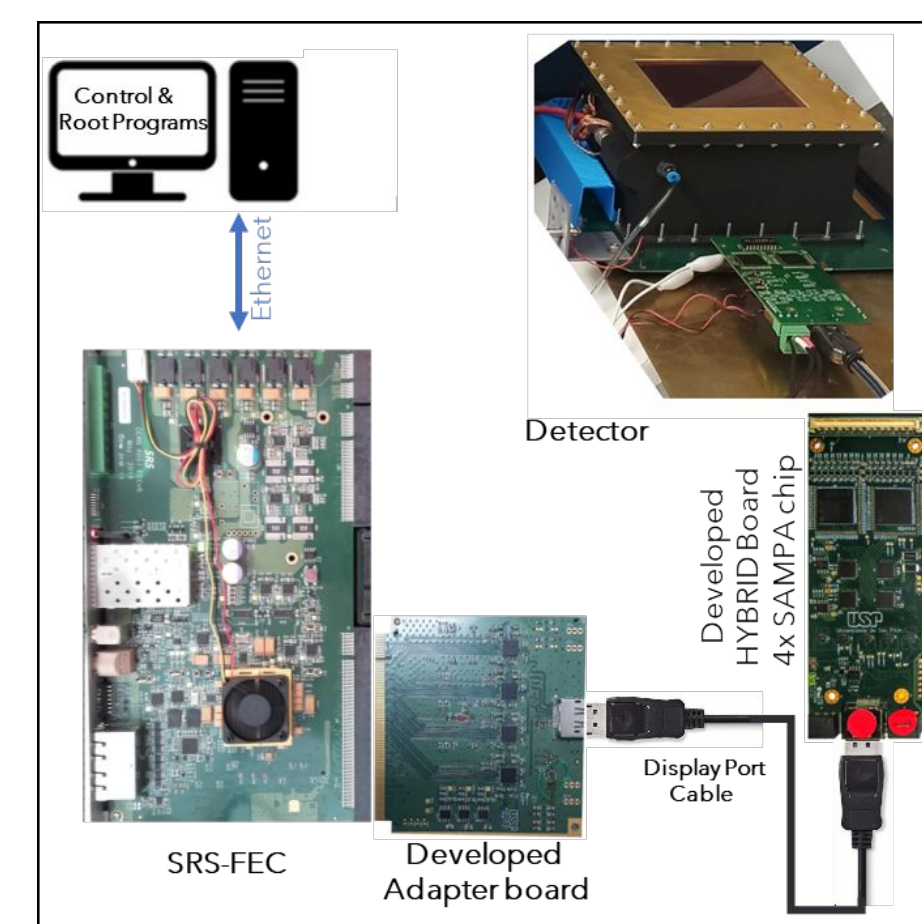
The complete setup

## Data processing

**Set of waveforms recorded after a trigger:**

Recorded event with 120 waveforms: Set of waveforms with the signal that composed the track 1 in the example below.

A saturated waveform from SAMPA: The raw signals are zero suppressed by removing the part of the pulse that is below 5σ of the baseline (which is determined from the first 80 samples of the pulse). Whenever the charge saturates the channel, the baseline increases its mean. In these cases, the zero suppression cut is changed to 20σ.

SAMPA integration still being developed, but most of the artefacts can be solved with off-line event processing
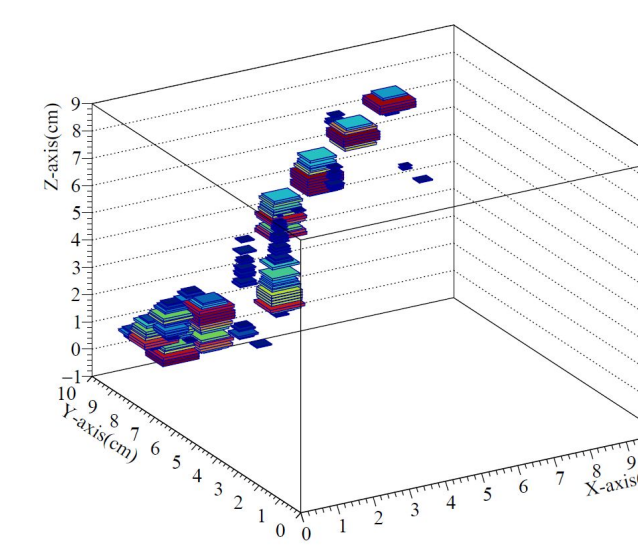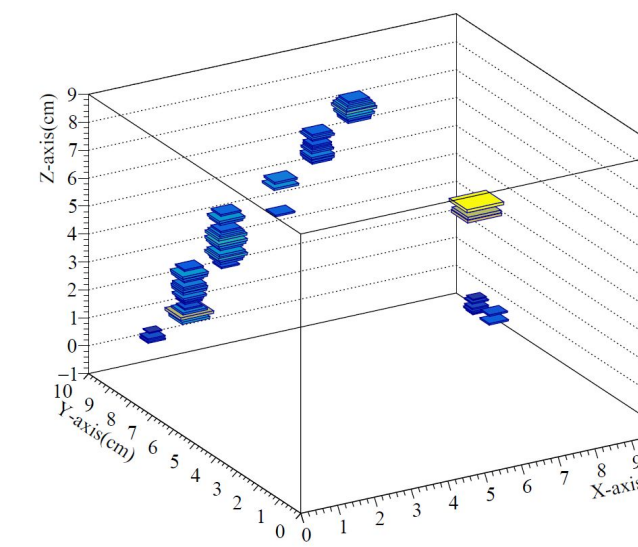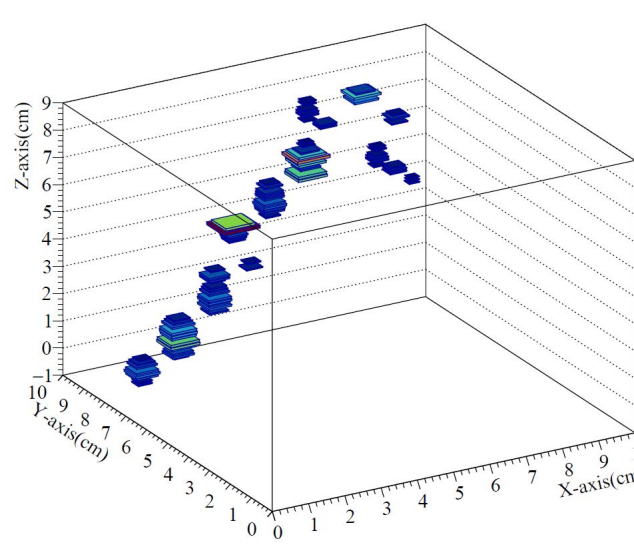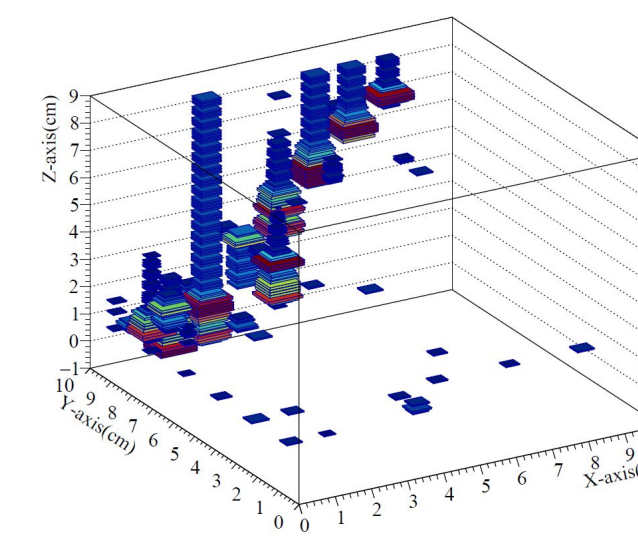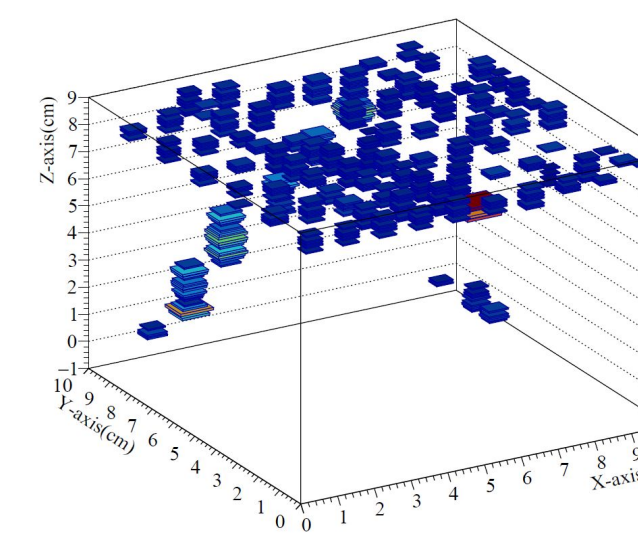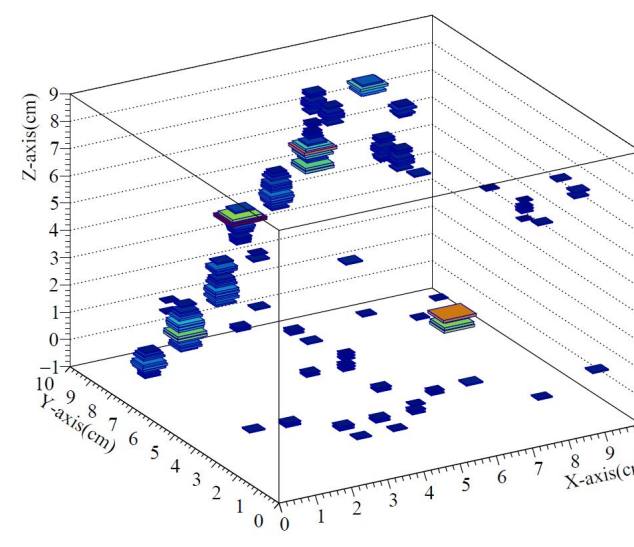
Example 1: Small amplitude events related to noise, where the baseline occasionally crosses the 5σ threshold.

Example 2: Artifacts yet somewhere unknown in the electronics that generated a pulse affecting many channels at the same time.

Example 3: Artifacts caused by the raise of the baseline after saturated pulses.

Work in progress

In the future we want to use the standard SRS softwares, developed to recover and process data produced by the SRS and the SAMPA. With that we can increase the rate and amount of the data retrieved by the system.

Solve digital communication issues that are already identified.

Optimize the hybrid component design.

Use the zero suppression and debugging features of the SAMPA chip.

More information

To know more about an experiment which is planning to use this integration check the poster of our colleagues at the gaseous detector session:

#195: Measurement of anomalies in the angular correlation of electron and positron internally produced in excited 8Be and 4He.

Acknowledgements and financial support

References

[1] - "SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades", J. Adolfsson et. al. *Journal of Instrumentation*, vol. 12, pp.

[2] - S. Martoiu, H. Muller and J. Toledo, "Front-end electronics for the Scalable Readout System of RD51," *2011 IEEE Nuclear Science Symposium Conference Record*, 2011, pp. 2036-2038, doi: 10.1109/NSSMIC.2011.6154414.C04008–C04008, Apr 2017.

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