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Progress towards readout chip for pixels with timing capabilities

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We present our developments towards a readout chip prototype for future pixel detectors with timing capabilities. The readout chip is intended for characterizing 4D pixel arrays with a pixel size of the order of 100x100 µm², where the sensors are LGADs. The long term focus is towards a possible application in the extended forward pixel system (TEPX) of the CMS experiment during the HL-LHC. The requirements for this ASIC are the incorporation of a TDC (Time to Digital Converter) in the small pixel area, low power consumption and radiation tolerance up to $5 \times 10^{15} n_{eq}/cm^2$ to withstand the radiation levels in the innermost rings of the TEPX modules during HL-LHC. Prototype structures have been designed and produced in 110 nm CMOS technology at LFoundry and UMC with different versions of TDC structures, together with a front end circuitry to interface with the sensors. The design of the front end will be discussed, with the test set-up for the measurements, and the first results comparing the performance of the different structures.

Collaboration

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