ID contributo: **240** Tipo: **Poster**

Design and tests of multi-Gbps radiation hard SERDES circuits in 65 nm CMOS technology

venerdì 27 maggio 2022 16:01 (1 minuto)

Future experiments at the LHC (beyond Phase-II upgrades) and in future colliders (like FCC) will need radiation tolerant multi-Gbps serial links for the detector readout. The most challenging components of those links are radiation tolerant (up to 1 Grad) Serializers and Deserializers (SERDES).
Current SERDES developed for the HL-LHC have limited radiation hardness (200 Mrad). We will present the status of the RD for 10-bit 3.2 Gbps SERDES with increased radiation tolerance in 65 nm CMOS technology.
Two circuits have been implemented on Silicon: a SER and a DES, with a modular architecture that makes them easily scalable, and full-custom Current Mode Logic (CML) cells (registers, clock buffers, CML/CMOS and CMOS/CML converters).
To match the desired radiation tolerance dedicated design techniques are requested, as the use of Enclosed Layout Transistors, n-MOS devices only and of "long"MOS devices. In addition we introduced (and later patented) an innovative compensation technique based on a tunable bias voltage in CML cells. Irradiation tests have shown that this technique is able to recover most of the performance degradation due to TID effects.
Two prototypes have been produced in the past couple of years. Test and characterization of the first prototypes led to design improvements in the SERDES design that allowed a significant reduction of the power dissipation. Thorough tests and characterization results of both devices will be presented.

Collaboration

Autori principali: PALLA, Fabrizio (Istituto Nazionale di Fisica Nucleare); MAGAZZU', Guido (Istituto Nazionale di Fisica Nucleare); CIARPI, Gabriele (DII); SAPONARA, Sergio (DII)

Relatore: PALLA, Fabrizio (Istituto Nazionale di Fisica Nucleare)

Classifica Sessioni: Front End, Trigger, DAQ and Data Mangement - Poster session