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Implementation of the Cluster Counting and Timing technique on FPGA for the reduction of transferred data and stored information.

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Ultra-low mass and high granularity Drift Chambers fulfill the requirements of tracking systems for modern High Energy Physics experiments at future high luminosity accelerators (FCC or CEPC). For this purpose, it is required the ability of reaching the expected resolutions and rate performance. The application of the Cluster Counting/Timing technique adds a valuable PID capabilities with resolutions outperforming the usual dE/dx technique. By measuring the arrival times of each individual ionization cluster to the sense wire and by using suitable statistical tools it is possible to perform a bias free estimate of the impact parameter and a precise PID in drift chamber operating in a Helium based gas mixtures The Cluster Counting/Timing technique consisting in isolating pulses due to different ionization clusters, therefore it is necessary to have a read-out interface capable of processing such high speed signals. This requires a data acquisition chain, able to manage the low amplitude signals from the sense wires (a ∼few mV) with a high bandwidth (∼1~GHz). The signals are first converted from analog to digital by a fast ADC. Requirements on the drift chamber performance impose conversions at sampling frequencies of at least 1~GS/s with 14-bit resolution.
These constraints, together with maximum drift times and many readout channels, impose some sizable data reduction strategy, while preserving all relevant information. Measuring both the amplitude and the arrival time of each peak in the signal associated to each ionization cluster is the minimum requirement on the data transfer for storage to prevent any data loss. An electronic board including a Fast ADC and an FPGA for real-time processing of the signals coming from a drift chamber is presented. Moreover, various algorithms implementation for peaks finding are compared.

Collaboration

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