Implementation of the Cluster Counting and Timing technique on FPGA for the reduction of transferred data and stored information.

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Abstract

Ultra-low mass and high granularity Drift Chambers fulfill the requirements of tracking systems for modern High Energy Physics experiments at future high luminosity accelerators (FCC or CEPC). The application of the Cluster Counting technique adds a valuable PID capabilities with resolutions outperforming the usual dE/dx technique. Moreover, by measuring the arrival times of each individual ionization cluster to the sense wire (Cluster Timing) and by using suitable statistical tools, it is possible to perform a bias free estimate of the impact parameter in drift chambers operated with a Helium based gas mixtures. The Cluster Counting/Timing techniques consist in isolating pulses due to different ionization clusters, therefore it is necessary to have a read-out interface capable of processing such high speed signals and to manage the low amplitude signals from the sense wires. An electronic board including a fast ADC and an FPGA for real-time processing is presented. Additionally, various algorithm implementations for peaks finding are compared.

Cluster counting/timing operation

In a conventional drift chamber, only the time of the first cluster is used to estimate the track impact parameter, thus providing a biased systematic overestimate. Cluster timing technique uses statistical tools to reduce the biased estimate by exploiting the information of all clusters detected with a cluster counting/timing algorithm implemented on a FPGA. The algorithm (in VHDL/Verilg languages) identifies, in the digitized signals, in real time, the peaks due to the single ionization electrons, records their times and amplitudes and sends the data stored to an external device when a specific trigger signals occurs.Initially, to evaluate the performance of the algorithm, simulated signals through an AWG have been used and the obtained results on the number of real and false peaks found have been compared to assess whether eventual errors were due to the algorithm itself or to approximations in the VHDL implementation and successively its efficiency calculated the percentage of fake peaks versus the number of real peaks.

Solution

The solution consists in transferring, for each hit drift cell, instead of the full spectrum of the signal, only the minimal information relevant to the application of the cluster timing/counting techniques, i.e. the amplitude and the arrival time of each peak associated with each individual ionization electron.

Hardware Setup

KIT EVAL ULTRASCALE FPGA KCU105

- UltraScale™ XCKU040-2FFVA1156E
- Transceiver 20 GTH
- 2 moduli SFP+ da 10Gbps

ADC32RF45EVM

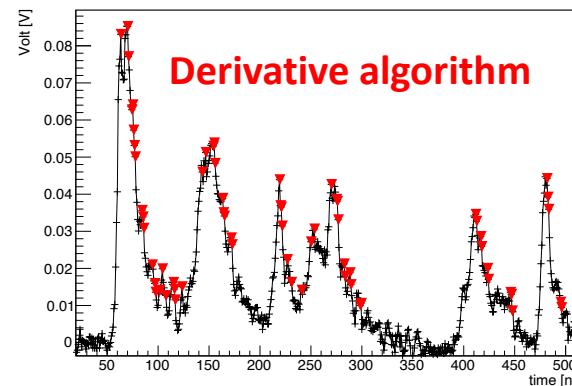- 14-bit
- Dual channel
- 3GSPS

Implementation of the algorithm

The CluTim algorithm (implemented on a FPGA, interfaced with a ADC), identifies in real-time the peaks corresponding to the different ionization cluster, stores each peak amplitude and time in an internal memory and sends the stored data to an external device when a specific trigger signal occurs. Such a quasi-on-line procedure results in data reduction factors of almost two orders of magnitude with respect to the raw digitized data.
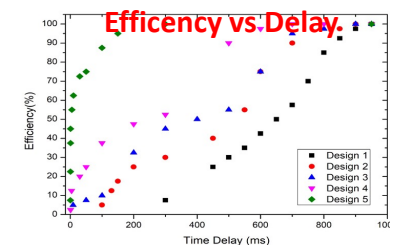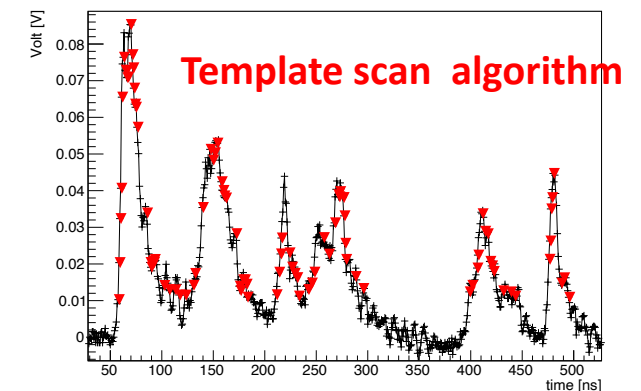
Cluster Finder Approach

Test on several possible algorithms. A simple peak finder algorithm, based on the first and second. The red arrows indicate the peaks identified by the algorithm

2 cm drift tube Track angle 45°
Derivative algorithm

2 cm drift tube Track angle 45°
Template scan algorithm

Efficiency vs Delay