Design and characterization of the electronics of a fully functional FoCal-E prototype

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The poster focuses on the development of the read-out electronics for a fully functional demonstrator model of the FoCal-E detector.

The concept of the detector and its main goals are introduced and illustrated. It is aiming to provide unique capabilities to constrain small-x gluon distributions via the measurement of the prompt photon production. It represents an upgrade to the ALICE experiment, and will be installed during LS3 (2026– 2028) for data taking at the LHC in 2028-2031.

This prototype is presented. It is composed of 18 single E-pad boards and 2 MAPS layers. They are all connected via an interface board to an aggregator system. Each single E-pad contains 72 Si-pixel sensors and a front-end ASIC (HGCROC). This ASIC ensures that the response of each sensor is read out using an integrated charge sensitive amplifier-shaper and an analog to digital conversion system (2-4 fC up to 10 pC) enabling the transmission of data. This board also contains probes to monitor the temperature, the power consumption and a local power converter to provide clean power supplies. The aggregator board is used to gather the data and trigger information from the detector at a data rate of 1,28 Gb/s. It is based on an FPGA allowing the extraction of data via multiple supports (Ethernet, CRU).

Results from a first SPS beam test are presented and the encountered issues are studied and resolved. The main issue is related to the connection of the bottom of the Si detector with the GND, because of that the single E-pad could not be tested next to the tungsten plate. Currently, a solution was implemented and tested in Lab conditions.

The integration of all the front-end electronics with the aggregator system is shown. This prototype is expected to be firstly tested under beam in PS in June 2022 then an SPS beam in the fall of 2022.

The next step is to build a full model based on the performance of this prototype for the end of 2023