ARCADIA FD-MAPS: simulation, characterization and perspectives for high resolution timing applications

ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

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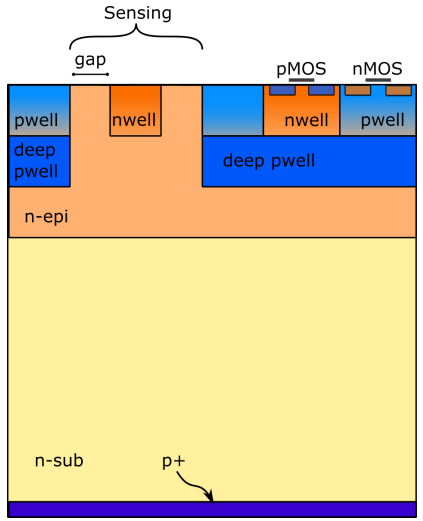
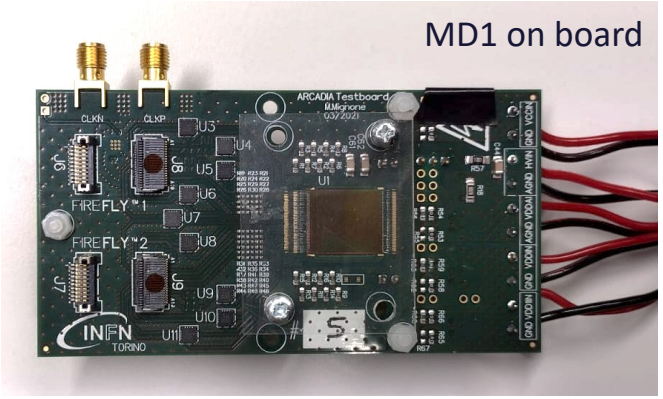
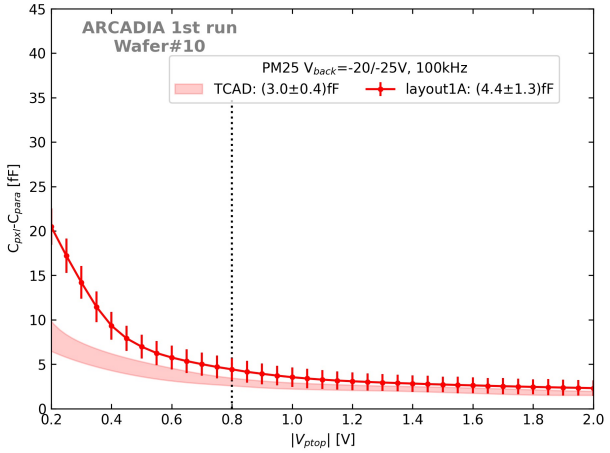


Fully depleted substrate at low front bias → charge collection via drift

- n-in-n device
- pn-junction on backside
- depletion voltage applied through backside, only low bias voltage from top
- low-resistive epi layer delays the onset punch-through currents
- backside processing (diode + GR) for thick sensors (> 100μm)



Main demonstrator (MD1) chip of (1.2×1.2)cm² with 512×512 fully depleted monolithic pixels with 25μm pitch.

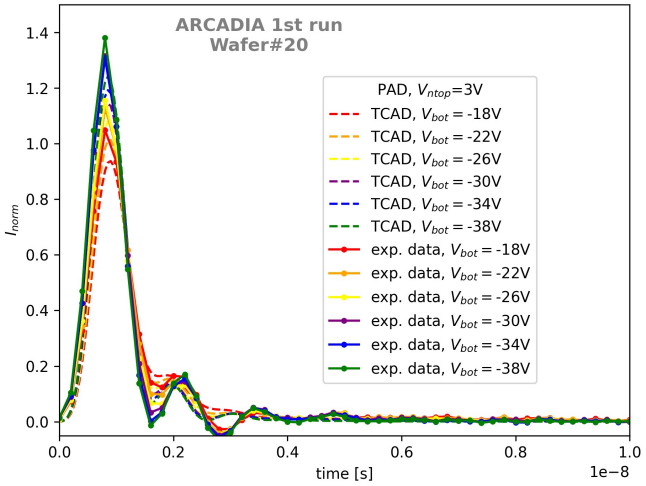


Focused IR laser, 1GHz bandwidth oscilloscope on (500×500)μm² pad

- Strong impact of 1GHz oscilloscope, well reproduced in simulation with digital low pass filter
- 95% charge collection in < 1.4ns in d_{Si}=50μm

Variety of passive pixel matrices

- Tests of pixels with (10/25/50)μm pitch from different wafers in different thicknesses (50/100/200)μm
- Capacitance of single pixel of MD1 found < 5fF



Ongoing development of MAPS for timing:

- Pad-like MAPs in 50µm pitch for chip implemented in 2nd run
  - *new large pixels including a charge multiplication layer*